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DATASHEET

Intel® Enpirion® Power Solutions

EM2140P01QI 40A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor, Featuring Digital Control with PMBus™ v1.2 Compliant Interface

Description

The EM2140 is a fully integrated 40A PowerSoC synchronous buck converter. It features an advanced digital controller, gate drivers, synchronous MOSFET switches, and a high performance inductor. Only input and output filter capacitors and a few small signal components are required for a complete solution. A PMBus version 1.2 compliant interface provides setup, control, and telemetry.

Differential remote sensing and ±0.5% set-point accuracy provides precise regulation over line, load and temperature variation. Very low ripple further reduces accuracy uncertainty to provide best in class static regulation for today's FPGAs, ASICs, processors, and DDR memory devices.

The EM2140 may be used in standalone mode or utilizing the PMBus interface for a high degree of flexibility and programmability. Advanced digital control techniques ensure stability and excellent dynamic performance, and eliminate the need for external compensation components. The PC-based Intel Enpirion Digital Power Configurator provides a user-friendly and easy-to-use interface to the device for communication and configuration.

The EM2140 features high conversion efficiency and superior thermal performance to minimize thermal de-rating limitations, which is key to product reliability and longevity.

Features

- Integrated inductor, FETs, and digital controller
- Wide 4.5V to 16V V_{IN} range
- 0.5V to 1.325V V_{OUT} range
- 40A continuous current with no thermal de-rating
- High efficiency in 11mm x 17mm x 6.76mm QFN package
  - 90% efficiency at V_{IN} = 12V, V_{OUT} = 1.2V
- Optimized total solution size of only 365 mm^2
- Meets all high performance FPGA requirements
  - Digital loop for best in class transient response
  - 0.5% set-point over line, load, and temperature
  - Output ripple as low as 10 mV peak-peak
  - Differential remote sensing
  - Monotonic startup into pre-bias output
  - Optimized FPGA configs stored in NVM
- Programmable through PMBus™
  - V_{OUT} margining, startup and shutdown delays
  - Programmable warnings, faults and response
- Ability to operate without PMBus™
  - RVSET resistor for programmable V_{OUT}
  - RTUNE resistor for single resistor compensation
- Tracking pin for complex sequencing
- RoHS compliant, MSL level 3, 260°C reflow

Applications

- High performance FPGA supply rails
- ASIC and processor supply rails
- High density double data rate (DDR) memory VDDQ rails

Ordering Information

Table 1

Part Number	Supported V_{OUT} Range	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
EM2140P01QI	0.5V to 1.325V	M2140	-40 to +85	17 mm x 11 mm x 6.76 mm QFN104 provided in 112 units per tray
EVB-EM2140P01	0.5V to 1.325V	Evaluation board; 40A single phase		
EVI-EM2COMIF	GUI interface dongle			

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments

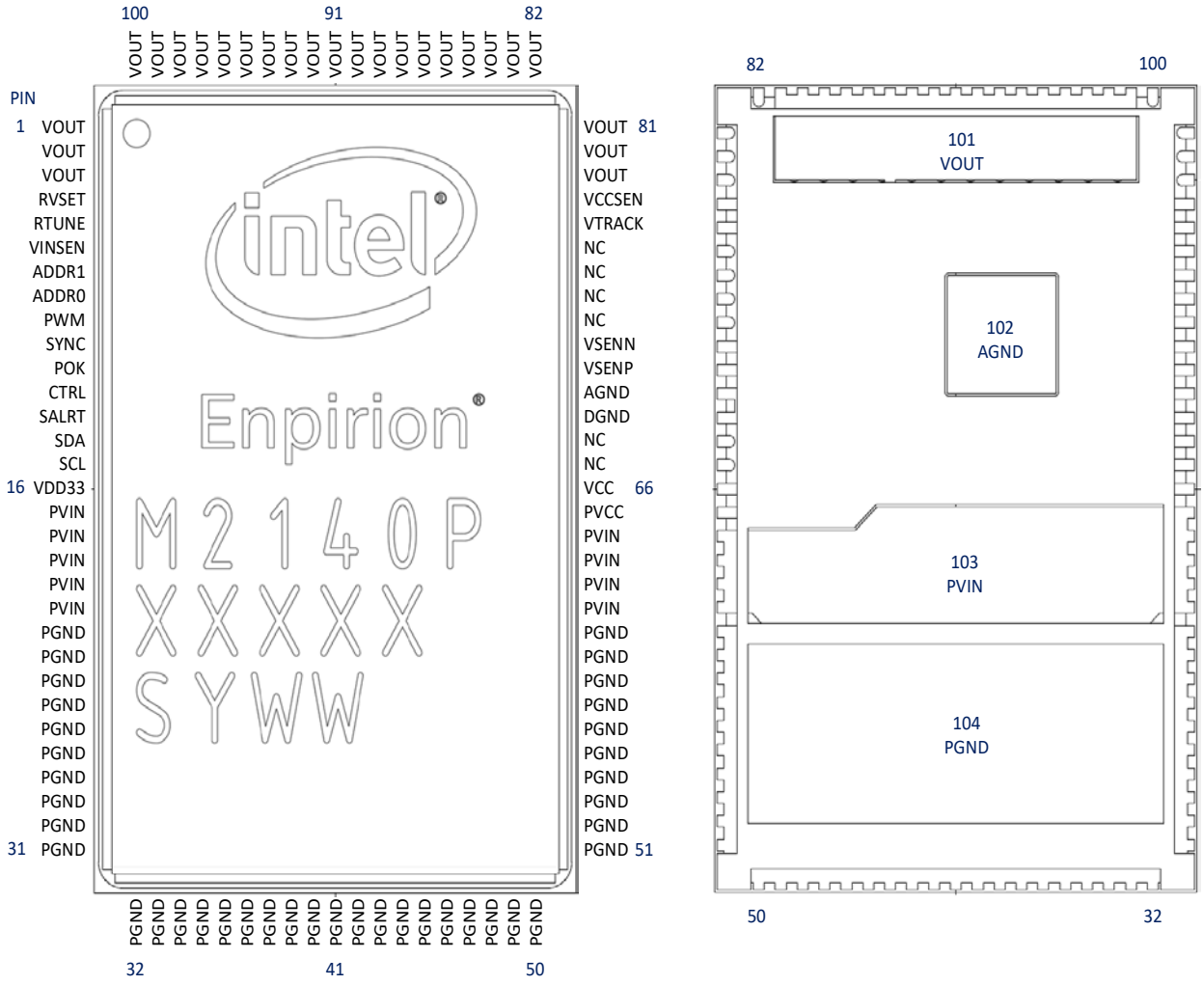


Figure 1: Pin Out Diagram

Pin Description

Table 2

PIN	NAME	I/O	FUNCTION
1,2,3, 79-101	VOUT	Regulated Output	Regulated output voltage. Decouple to PGND with appropriate filter capacitors
4	RVSET	Analog I/O	A resistor from RVSET to AGND; and can be used to program the V_{OUT} set-point. Using 1% tolerance or better resistor. See Table 8 for more information.
5	RTUNE	Analog I/O	A resistor from RTUNE to AGND; and can be used to tune the transient compensator for the amount of output capacitance. Using 1% tolerance or better resistor. See Table 9 for more information.
6	VINSEN	Analog Input	Single-ended input voltage sense (relative to AGND).
7	ADDR1	Analog I/O	A resistor from ADDR1 to AGND; and can be used to set the PMBus™ address. Use a 1% tolerance or better resistor.
8	ADDR0	Analog I/O	A resistor from ADDR0 to AGND; and can be used to set the PMBus™ address. Use a 1% tolerance or better resistor.
9	PWM	PWM	PWM signal test pin.
10	SYNC	Digital I/O	PWM synchronization signal
11	POK	Digital I/O	Power OK is selectable as a push-pull output or an open drain transistor for power system state indication. See the Power OK description for details
12	CTRL	Digital Input	PMBus-compatible control pin with programmable functionality. CTRL should never be left floating if enabled in Configuration. The default configuration is for V_{OUT} to be on with CTRL high (positive edge)
13	SALRT	Digital Output	PMBus™ alert line.
14	SDA	Digital I/O	PMBus™ serial data I/O.
15	SCL	Digital Input	PMBus™ serial clock input.
16	VDD33	Output	3.3V output of the internal LDO. May be used as pull-up supply for PMBus™ pins and CTRL pin.
17-21, 61-64, 103	PVIN	Input Supply	Input supply for MOSFET switches. Decouple to PGND with appropriate filter capacitors. Refer to Recommended Application Circuit section for more details.
22-60, 104	PGND	Ground	Power ground. Ground for MOSFET switches.
65	PVCC	Input Supply	5.0V supply voltage for driver circuitry. Decouple to PGND using a 2.2µF MLCC high quality ceramic capacitor.
66	VCC	Input Supply	5.0V supply voltage for analog circuitry.
67,68, 73-76	NC	NC	No connect. Do not connect to any signal, supply, or ground.
69	DGND	Ground	Digital ground. Connect to AGND pin directly.

PIN	NAME	I/O	FUNCTION
70, 102	AGND	Ground	Analog ground. Connect to system ground plane. Refer to layout section for more details on grounding.
71	VSENP	Analog Input	Differential output voltage sense input (positive).
72	VSENN	Analog Input	Differential output voltage sense input (negative).
77	VTRACK	Analog Input	Voltage tracking reference input if EM2140 is configured for voltage tracking mode. May remain floating if not used**. If enabled but not used, connect to VDD33 using a 10kΩ resistor**. VTRACK is not enabled in the default configuration.
78	VCCSEN	Analog Input	Single-ended VCC voltage sense (relative to AGND)

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Voltage measurements are referenced to AGND.

Absolute Maximum Pin Ratings

Table 3

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply voltage PVIN	PVIN	-0.3	18	V
Supply voltage VCC	VCC	-0.3	5.5	V
VCC ramp time	VCC		20	ms
VDD33	VDD33	-0.3	3.6	V
Digital ground	DGND	-0.3	0.1	V
Power ground	PGND	-0.3	0.3	V
Digital I/O pins	SALRT, POK, SYNC,	-0.3	5.5	V
Digital I/O pins	SCL, SDA, CTRL	-0.3	3.6	V
Analog I/O pins	VINSEN, VCCSEN, ADDR1, ADDR2, RVSET, RTUNE, VTRACK	-0.3	2.0	V
Voltage feedback	VSENP, VSENN	-0.3	2.0	V
PWM pin	PWM	-0.3	5.5	V
Output voltage pins	VOUT	-0.3	1.44	V
DC current on VOUT	VOUT		43	A

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Operating junction temperature			+125	°C
Storage temperature range		-65	+150	°C
Reflow peak body temperature	(10 Sec) MSL3		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBD	All pins; Except VINSEN 1000 V Max	2000		V
CDM; all pins		500		V

Recommended Operating Conditions

Table 4

PARAMETER	PINS	MIN	MAX	UNITS
PVIN supply voltage range	PVIN	4.5	16	V
Supply voltage V_{CC} & PV_{CC}	VCC, PVCC	4.75	5.25	V
Continuous load current	V_{OUT}		40	A

Thermal Characteristics

Table 5

PARAMETER	PINS	TYPICAL	UNITS
Thermal shutdown [programmable]	T_{SD}	120	°C
Thermal shutdown Hysteresis	T_{SDH}	18	°C
Thermal resistance: junction to ambient (0 LFM) *(Note1)*	θ_{JA}	8	°C/W
Thermal resistance: junction to case bottom (0 LFM)	θ_{JC}	1.5	°C/W

Note1: Based on 2 oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51 standards for high thermal conductivity boards. No top side cooling required.

Electrical Characteristics

PV_{IN} = 12V and V_{CC} = 5.0V. The minimum and maximum values are over the operating ambient temperature range (-40°C to 85°C) unless otherwise noted. Typical values are at T_A = 25°C.

Table 6

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CHARACTERISTICS						
PVIN supply voltage range	PVIN		4.5		16	V
PVIN supply quiescent current		Device switching; no load; f_{sw} = 800 kHz; V_{OUT} = 1.0V		40		mA
		Device not switching		1		
VCC supply voltage range	VCC		4.75	5.0	5.25	V
VCC UVLO rising				4.4		V
VCC UVLO falling				4.2		V
PVCC & VCC supply current		Normal operation; no load; f_{sw} = 800 kHz		80		mA
		Idle; communication and telemetry only; no switching		30		mA
		Disabled (V_{CC} ≤ 2.8V)		900		µA
INTERNALLY GENERATED SUPPLY VOLTAGE						
VDD33 voltage range	VDD33		3.0	3.3	3.6	
VDD33 output current					2	mA
DIGITAL I/O PINS (POK, SYNC)						
Input high voltage			2.0		5.5	V
Input low voltage			0		0.8	V
Output high voltage			2.4		VDD33	V
Output low voltage					0.4	V
Input leakage current					±1	µA
Output current - source					2.0	mA
Output current - sink					2.0	mA
DIGITAL I/O PIN (CTRL)						
Input high voltage			2.0		3.6	V
Input low voltage			-0.3		0.8	V
CTRL response delay (stop)		Configurable polarity; extra turn-off delay configurable (assumes 0 s turn-off delay)		150		µs

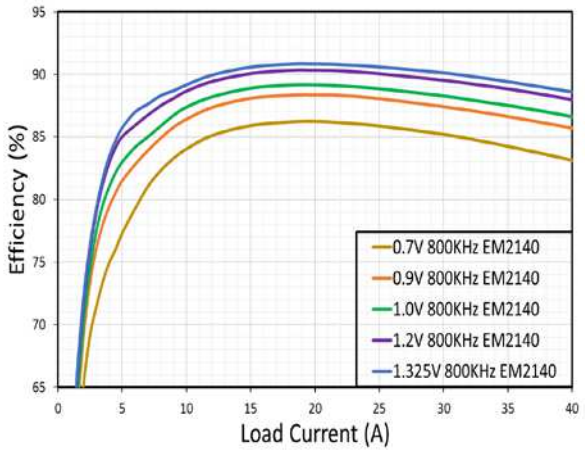
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CTRL response delay (start)		Configurable polarity; extra turn-on delay configurable (assumes 0 s turn-on delay)		250		µs
HKADC INPUT PINS (VINSEN, VCCSEN, ADDR0 AND ADDR1)						
Input voltage			0		1.44	V
PWM AND SYNCHRONIZATION						
PWM output voltage - high			2.4			V
PWM output voltage - low					0.4	V
PWM tristate leakage					±1	µA
PWM pulse width			30			ns
Resolution				163		ps
Switching frequency – EM2140	f_{SW}	With internal oscillator		800		kHz
SYNC frequency range		Percent of nominal switching frequency			±12.5	%
SYNC pulse width			25			ns
OUTPUT VOLTAGE SENSE, REPORTING, AND MANAGEMENT						
Output voltage adjustment range	EM2140		0.5		1.325	V
Output voltage set-point accuracy	EM2140	$0^{\circ}C < T_A < 85^{\circ}C$	-0.5		+0.5	%
	EM2140	$-40^{\circ}C < T_A < 85^{\circ}C$	-1		+1	%
Output set-point resolution	EM2140			1.5		mV
Line regulation				0.007		mV/V
Load regulation				0.07		mV/A
Output voltage startup delay		From V_{CC} valid, to start of output voltage ramp, if configured to regulate from power on reset, and TON_DELAY is set to 0.		5		ms
Output voltage ramp delay (TON_DELAY & TOFF_DELAY)		Configurable, no V_{OUT} pre-bias condition.	0		500	ms
Vout slew rate				0.5		V/ms
VTRACK ramp rate					2.0	V/ms
VTRACK range		Without resistor divider	0		1.4	V
VTRACK offset voltage				±100		mV

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CURRENT SENSE, REPORTING, AND MANAGEMENT						
Current sense reporting accuracy		$25°C \leq T_A < 85°C$		±1.5		A
		$I_{OUT} > 5A, T_A = 25°C$		±1		A
TEMPERATURE SENSE, REPORTING, AND MANAGEMENT						
Temperature reporting accuracy				±5		°C
Resolution				0.22		°C
FAULT MANAGEMENT PROTECTION FEATURES						
PV_{IN} UV threshold				3.96		V
PVIN OV threshold				16.5		V
V_{OUT} OV threshold		Percentage of output voltage		115		%
V_{OUT} UV threshold		Percentage of output voltage		85		%
I_{OUT} OCP		With 65A OCP setting	60		70	A
OTP threshold				120		°C
OTP hysteresis		Fixed.		85		%
POK threshold		On level		95		%
POK threshold		Off level		90		%
Watchdog Timer Interval					3	ms
SERIAL COMMUNICATION PMBUS DC CHARACTERISTICS						
Input voltage – high (VIH)		SCL and SDA	1.11			V
Input voltage – low (VIL)		SCL and SDA			0.8	V
Rise & Fall Time		SCL and SDA >0.8V<1.1V			2	ms
Input leakage current		SCL, SDA, SALRT, and CTRL.	-10		10	µA
Output voltage – low (VOL)		SDA and SALRT at rated pull-up current of 20mA.			0.4	V
Nominal bus voltage		SCL, SDA, and SALRT termination voltage.			3.6	V

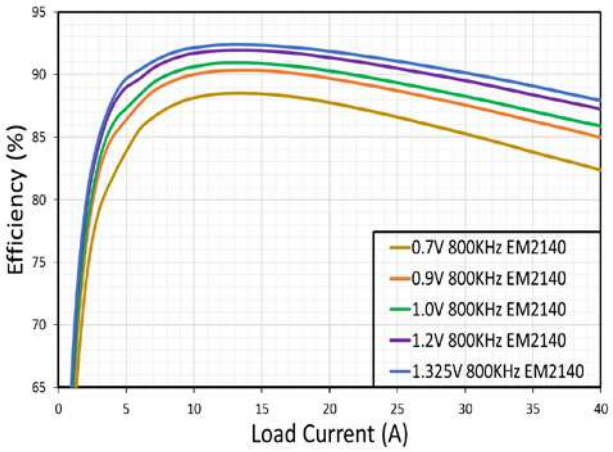
Typical Performance Characteristics

All the performance curves are measured with EM2140 evaluation board at 25°C ambient temperature unless otherwise noted. The output capacitors configuration for the evaluation board is 2 x 470 µF (3 mΩ ESR) + 4 x 100 µF (Ceramic) + 4 x 47 µF (Ceramic).

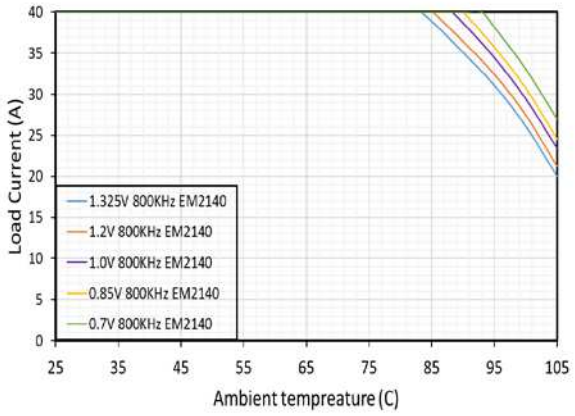
Efficiency, V_{IN} = 12V



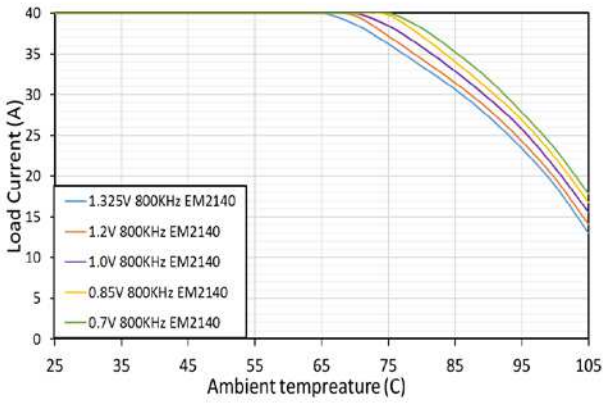
Efficiency, V_{IN} = 5V



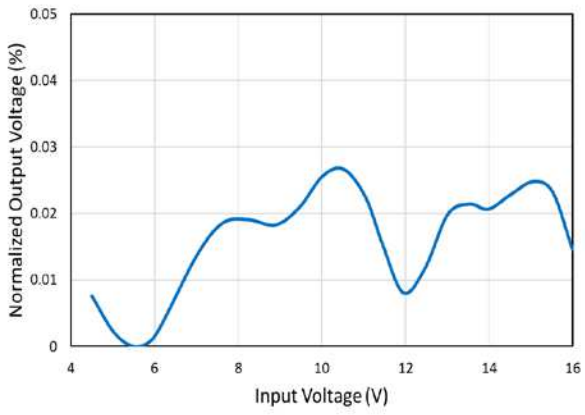
Thermal Derating, With Airflow 400 LFM



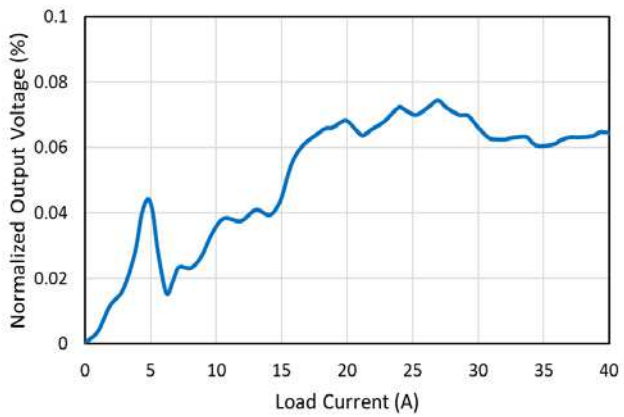
Thermal Derating, No Airflow



EM2140 Line Regulation, V_{OUT} = 0.9V

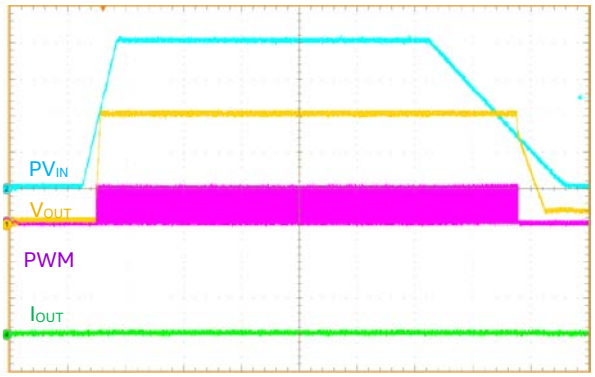


EM2140 Load Regulation, V_{OUT} = 0.9V



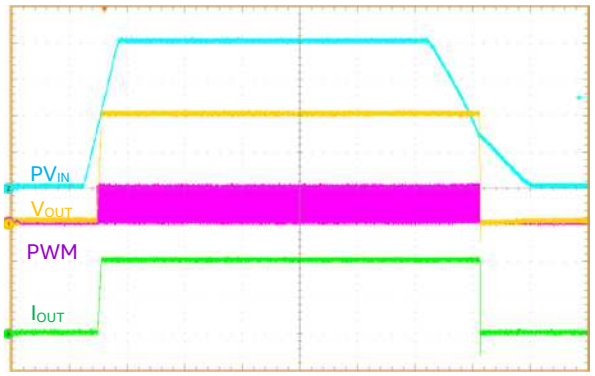
Typical Performance Characteristics (Continued)

Start-up/Shutdown, PVIN At No Load, 20 ms/div



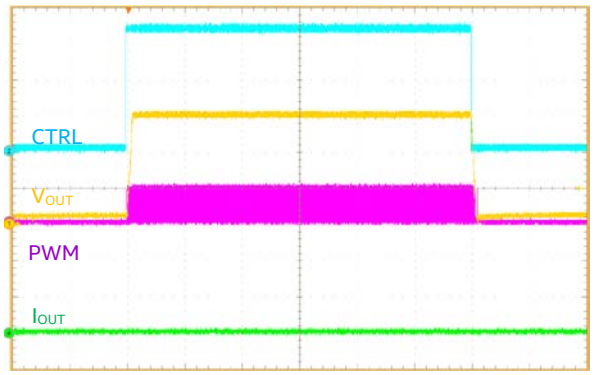
PV_{IN} and PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, PVIN At 20A Load, 20 ms/div



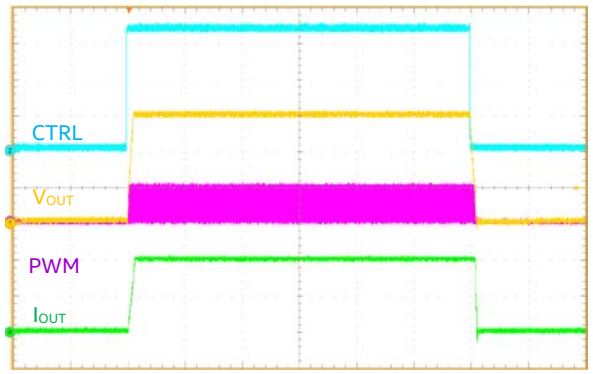
PV_{IN} and PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, CTRL At No Load, 10 ms/div



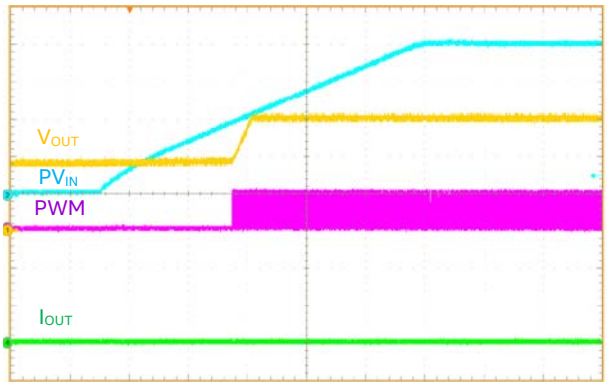
CTRL: 1 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, CTRL At 20A Load, 10 ms/div



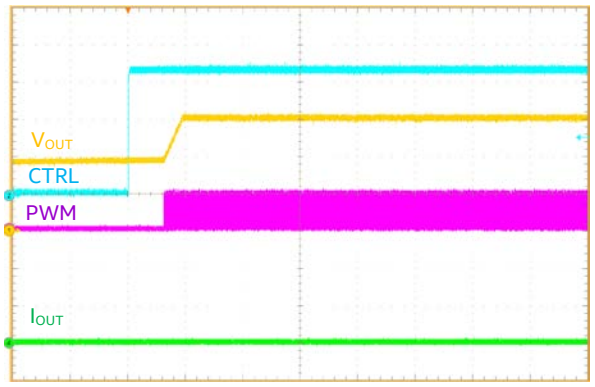
CTRL: 1 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up Into 0.6V Pre-Bias With PVIN, 2 ms/div



PV_{IN}: 3 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

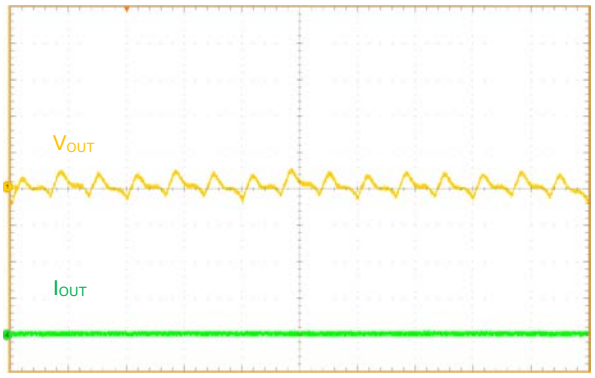
Start-up Into 0.6V Pre-Bias With CTRL, 2 ms/div



CTRL: 1 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

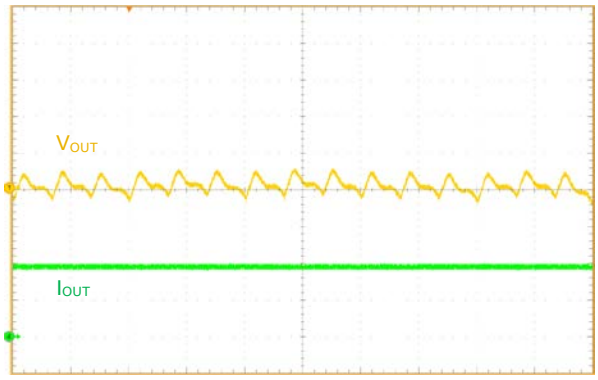
Typical Performance Characteristics (Continued)

Output Voltage Ripple, No Load



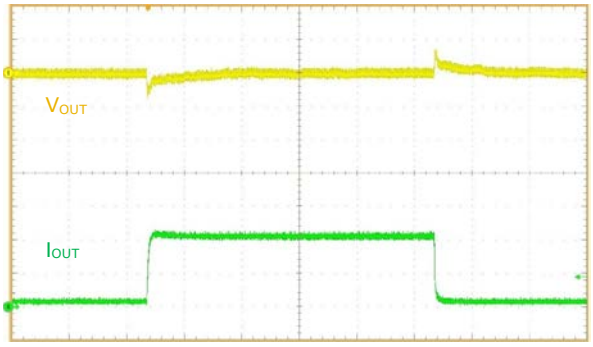
V_{IN} = 12V, V_{OUT} = 0.9V
2 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Ripple, 40A Load



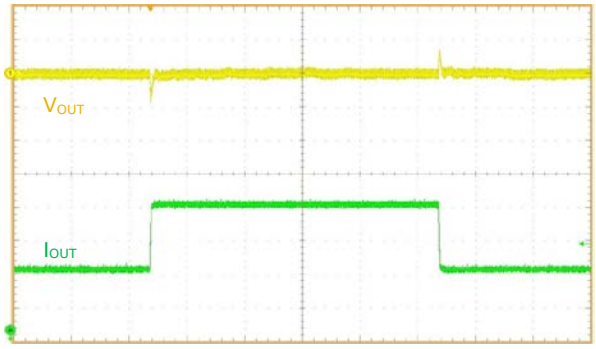
V_{IN} = 12V, V_{OUT} = 0.9V
2 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Transient Response, Load Step From 0A To 20A



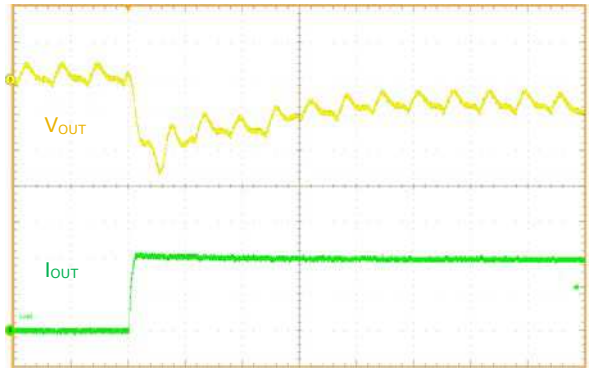
V_{IN} = 12V, V_{OUT} = 0.9V, 100µs/div
V_{OUT}: 30mV/div, I_{OUT}: 10A/div, 10A/µs

Output Voltage Transient Response, Load Step From 20A To 40A



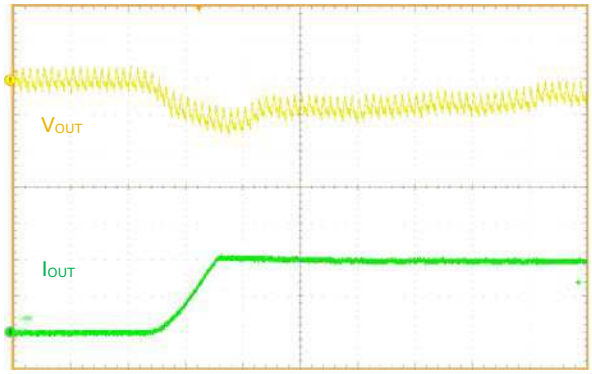
V_{IN} = 12V, V_{OUT} = 0.9V, 100µs/div
V_{OUT}: 30mV/div, I_{OUT}: 10A/div, 10A/µs

Output Voltage Transient Response, Load Step From 0A To 20A



V_{IN} = 12V, V_{OUT} = 0.9V, 2µs/div
V_{OUT}: 10mV/div, I_{OUT}: 10A/div, 10A/µs

Output Voltage Transient Response, Load Step From 0A To 20A



V_{IN} = 12V, V_{OUT} = 0.9V, 10µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 10A/div, 1A/µs

Functional Block Diagram

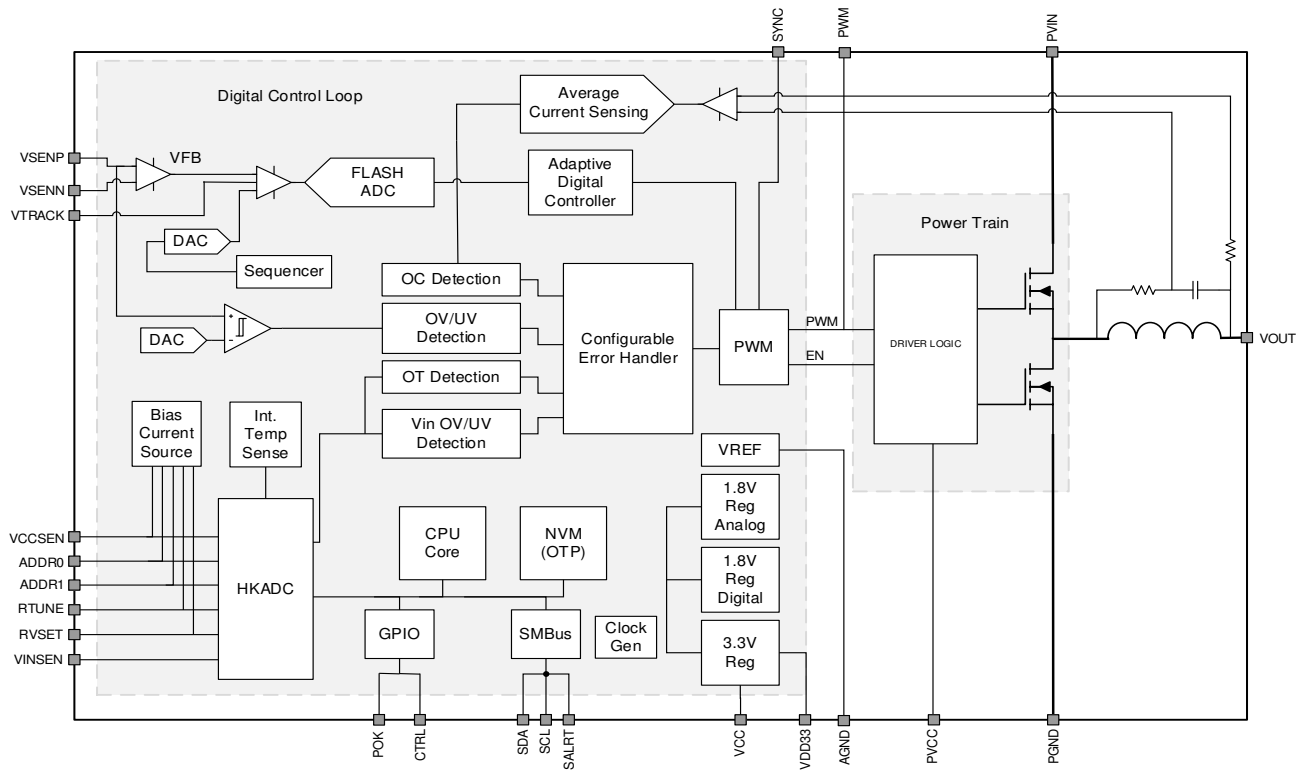


Figure 2: Functional Block Diagram

Functional Description

FUNCTIONAL DESCRIPTION: DEFAULT CONFIGURATION

The EM2140 is a single output digital PowerSoC synchronous step-down converter with advanced digital control techniques, capable of supplying up to 40A of continuous output current. The PowerSoC includes integrated power MOSFETs, a high-performance inductor and a digital controller which offers a PMBus version 1.2 compliant interface to support an extensive suite of telemetry, configuration and control commands.

In the default configuration, the EM2140 requires only two resistors total to set the output voltage and set the digital compensator for the most optimized performance. This easy-to-use default configuration allows the user to tune the EM2140 to meet the most demanding accuracy and load transient requirements without requiring any programming or digital interface. The following sections describe the default configuration. Refer to the Advanced Configuration section for details on the many ways the EM2140 may be customized and configured through the PMBus interface.

In order to optimize size versus efficiency over a wide range of operating conditions, there are two module variants – a low output voltage variant EM2140 (0.7V ≤ V_{OUT} ≤ 1.325V) which operates at 800KHz.

The advanced digital control loop works as a voltage-mode controller using a PID-type compensation. The basic structure of the controller is shown in Figure 3. The EM2140 controller features two PID compensators for steady-state operation and fast transient operation. Fast, reliable switching between the different

compensation modes ensures good transient performance and quiet steady state performance. The EM2140 has been pre-programmed with a range of default compensation coefficients which lets the user select the best compensation for the best transient response and stability for the output capacitance of the system.

The EM2140 uses two additional technologies to improve transient performance. First, the EM2140 uses over-sampling techniques to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any changes in output voltage. Second, a non-linear gain adjustment is applied during large load transients to boost the loop gain and reduce the settling time.

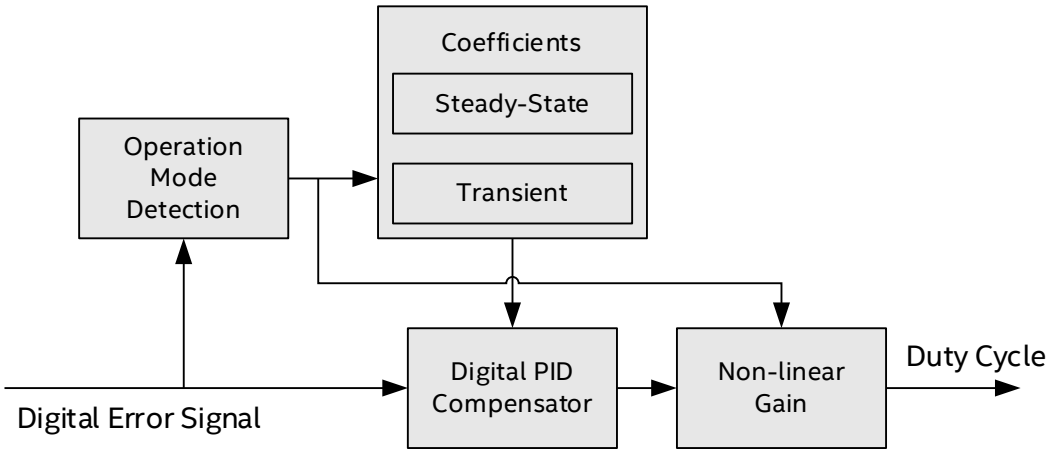


Figure 3: Simplified Block Diagram Of The Digital Compensation

In the default configuration, the EM2140 offers a complete suite of fault warnings and protections. Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored. A dedicated ADC is used to provide fast and accurate current information over the switching period allowing for fast Over-Current Protection (OCP) response. Over Temperature Protection (OTP) is accomplished by direct monitoring of the device's internal temperature.

POWER ON RESET

The EM2140 employs an internal power-on-reset (POR) circuit to ensure proper start-up and shut down with a changing supply voltage. Once the VCC supply voltage increases above the POR threshold voltage, the EM2140 begins the internal start-up process. Upon its completion, the device is ready for operation.

Two separate input voltage supplies are necessary to operate, PVIN (4.5V to 16V) and V_{CC} (4.75V to 5.25V). Both of these voltage rails must be monitored for proper power-up and to protect the power MOSFETs under various input power fault conditions. A voltage divider on each input voltage supply connected to VINSEN for the power rail (PVIN) and VCCSEN for the supply rail (VC) is used for digital monitoring of the supplies.

As illustrated in Figure 4, the values of resistors R1, R2, R3 and R4 are chosen so the internal monitor ADC does not saturate within the appropriate ranges. This allows the EM2140 telemetry to report when the recommended operation voltage has been exceeded.

It is mandatory that the listed resistors values are used in order to ensure proper operation with the EM2140 default configuration. The resistors used must be R1=11 kΩ, R2=1 kΩ, R3=10 kΩ and R4=3.3 kΩ, using 1%

tolerance or better resistors. If these values are not used then the EM2140 will read incorrect values for both PVIN and VCC.

Digital filtering is provided inside the EM2140 but if additional filtering is needed due to high noise on either rail, a capacitor can be connected between each pin (VINSEN & VCCSEN) and ground to maintain high accuracy.

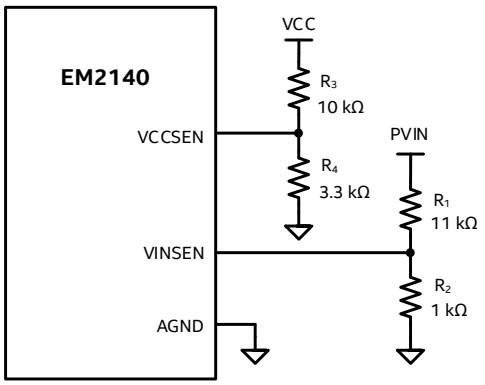


Figure 4: VINSEN And VCCSEN Input Resistor Dividers

The EM2140 also uses the PVIN monitor for input voltage feed-forward, which eliminates variations in the output voltage due to sudden changes in the input voltage supply. It does this by immediately changing the duty cycle to compensate for the input supply variation by normalizing the DC gain of the loop.

SETTING THE OUTPUT VOLTAGE

Differential remote sensing provides for precise regulation at the point of load. One of thirty output voltages may be selected in the default configuration, based on a resistor connected to the RVSET pin. At power-up, an internal current source biases the resistor and the voltage is measured by an ADC to decode the Vout selection. Use the RVSET tables (Table 8) for the details of VOUT selection and RVSET values.

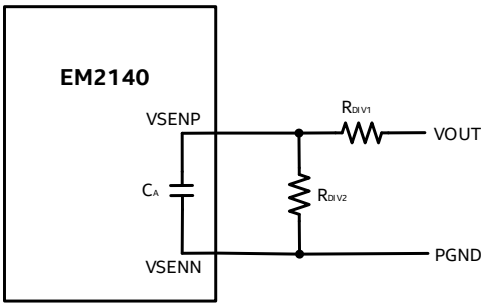


Figure 5: Output Voltage Sense Circuitry

The digital control loop ADC of the low voltage EM2140 supports direct output voltage feedback connection over the entire V_{OUT} range. For the low output voltage EM2140, a feedback divider is required as shown in Figure 5. The resistor values in Table 7 are required as a function of the output voltage selection. It is mandatory that the listed resistor values are used, use of other values may result in poor regulation performance as these values are expected in the EM2140 default configuration. Resistors with tight tolerances are recommended to maintain output voltage accuracy.

The resistors in the feedback path also form a low-pass filter with the internal capacitor, C_A, for removing high-frequency disturbances from the sense signals. Place these components as close as possible to the EM2140 for best filtering performance.

Table 7: Output Voltage Feedback Component

Module	V_{OUT}	R_{DIV1}	R_{DIV2}
EM2140	$0.7V \le V_{OUT} \le 1.325V$	2 kΩ	Open

Table 8: Supported Configuration Voltage Values For EM2140 Output Voltage

RVSET Resistor	V_{OUT}	External Resistor Divider
0kΩ	0.5V	R_{1DIV} = 2kΩ, R_{2DIV} = open
0.392kΩ	0.55V	R_{1DIV} = 2kΩ, R_{2DIV} = open
0.576kΩ	Reserved	R_{1DIV} = 2kΩ, R_{2DIV} = open
0.787kΩ	Reserved	R_{1DIV} = 2kΩ, R_{2DIV} = open
1.000kΩ	1.325V	R_{1DIV} = 2kΩ, R_{2DIV} = open
1.240kΩ	1.3V	R_{1DIV} = 2kΩ, R_{2DIV} = open
1.500kΩ	1.275V	R_{1DIV} = 2kΩ, R_{2DIV} = open
1.780kΩ	1.25V	R_{1DIV} = 2kΩ, R_{2DIV} = open
2.100kΩ	1.225V	R_{1DIV} = 2kΩ, R_{2DIV} = open
2.430kΩ	1.2V	R_{1DIV} = 2kΩ, R_{2DIV} = open
2.800kΩ	1.175V	R_{1DIV} = 2kΩ, R_{2DIV} = open
3.240kΩ	1.15V	R_{1DIV} = 2kΩ, R_{2DIV} = open
3.740kΩ	1.12V	R_{1DIV} = 2kΩ, R_{2DIV} = open
4.220kΩ	1.1V	R_{1DIV} = 2kΩ, R_{2DIV} = open
4.750kΩ	1.075V	R_{1DIV} = 2kΩ, R_{2DIV} = open
5.360kΩ	1.05V	R_{1DIV} = 2kΩ, R_{2DIV} = open
6.040kΩ	1.03V	R_{1DIV} = 2kΩ, R_{2DIV} = open
6.810kΩ	1.0V	R_{1DIV} = 2kΩ, R_{2DIV} = open
7.680kΩ	0.975V	R_{1DIV} = 2kΩ, R_{2DIV} = open
8.660kΩ	0.95V	R_{1DIV} = 2kΩ, R_{2DIV} = open
9.530kΩ	0.925V	R_{1DIV} = 2kΩ, R_{2DIV} = open
10.500kΩ	0.9V	R_{1DIV} = 2kΩ, R_{2DIV} = open
11.800kΩ	0.875V	R_{1DIV} = 2kΩ, R_{2DIV} = open
13.000kΩ	0.85V	R_{1DIV} = 2kΩ, R_{2DIV} = open
14.300kΩ	0.825V	R_{1DIV} = 2kΩ, R_{2DIV} = open
15.800kΩ	0.8V	R_{1DIV} = 2kΩ, R_{2DIV} = open
17.400kΩ	0.775V	R_{1DIV} = 2kΩ, R_{2DIV} = open
19.100kΩ	0.75V	R_{1DIV} = 2kΩ, R_{2DIV} = open

RVSET Resistor	V_{OUT}	External Resistor Divider
21.000kΩ	0.725V	R_{1DIV} = 2kΩ, R_{2DIV} = open
23.200kΩ	0.7V	R_{1DIV} = 2kΩ, R_{2DIV} = open

ENABLE And OUTPUT START-UP BEHAVIOR

The control pin (CTRL) provides a means to enable normal operation or to shut down the device. When the CTRL pin asserted (high) the device will undergo a normal soft-start. A logic low on this pin will power the device down in a controlled manner. Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this period.

The typical power sequencing, including ramp up/down and delays is shown in Figure 6.

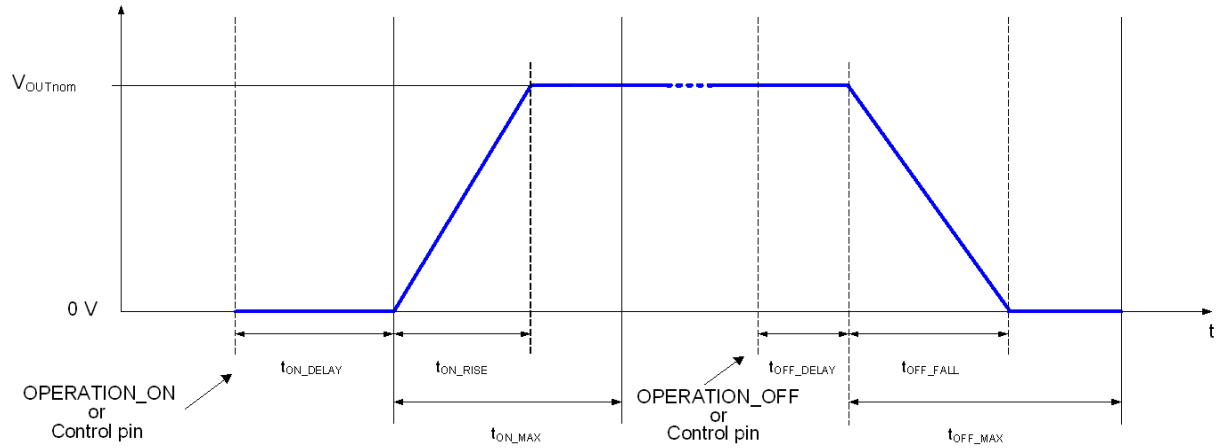


Figure 6: Power Sequencing

POWER OK

The EM2140 has a power good indicator at its output pin, POK. When de-asserted, POK indicates that the output voltage is below the threshold value, 90% of the programmed output voltage in the default configuration. When asserted, POK indicates that the output is in regulation, and no major faults are present. As a result, POK de-asserts during any serious fault condition where power conversion stops and re-asserts when the output voltage recovers.

The POK indication can be either push-pull or open-drain, selected based upon the PMBus™ address. For addresses in the range 0x01 to 0x40, the POK signal is a push-pull output and no pull-up resistor is required. For addresses in the range 0x41 to 0x7F, the POK signal is open-drain and may be wire-OR's with other open drain signals with an appropriate pull-up resistor. The Pull-Up resistor may be connected to the VDD33 pin but it is not recommended to use the 5VCC supply. Table 13 describes the resistor values which are used to set the PMBus address.

In a noisy application, it is strongly recommended that a 100nf decoupling capacitor be placed between the POK pin and GND to act as a filter to unwanted external noise . When configured as a Push-Pull output, a 10kΩ pull-down resistor to Gnd may be used instead to prevent any spurious noise spikes appearing on POK upon power being applied to the module.

COMPENSATING THE DIGITAL CONTROL LOOP

To improve the transient performance for a typical point-of-load design, it is common to add output capacitance to the converter. This moves the output LC resonant frequency lower as capacitance increases which results in lower bandwidth, lower phase margin, and longer settling times unless the control loop is compensated for added capacitance.

However, with EM2140 the user does not need to be concerned with, or even understand, the details of control loop compensation techniques. The default configuration allows users to select from preconfigured PID control loop settings (known as compensators) through the use of pin-strapping. A single resistor from the RTUNE pin to AGND informs the EM2140 of the compensator selection.

The selection of the compensator is driven first by the type of output capacitors used, as the ESL and ESR of different capacitor types demands different PID coefficients to optimize transient deviation and recovery characteristics. An all ceramic output capacitor design requires a different compensator than a design with a combination of ceramic and polymer capacitors, i.e. POSCAP. Table 10 shows several output capacitor part number recommendations.

The five different compensators can then be subdivided into groups of six each whereby the initial capacitance value in the appropriate compensator can be scaled upwards by multiplication factor M to match the additional capacitance.

Table 9 :RTUNE configuration table for EM2140

Compensator Description	C_{OUT}	RTUNE Resistor	Multiplication factor (M)	Typical Deviation With 20A Load Step
Polymer Aluminum (SP-CAP) and Ceramic MLCC Output Capacitors Base capacitance = 1 x 470µF (Polymer) + 2 x 100µF (Ceramic) + 2 x 47µF (Ceramic)	Base	0kΩ	1	± 5%
	2 x Base	0.392kΩ	2	± 3%
	3 x Base	0.576kΩ	3	
	4 x Base	0.787kΩ	4	± 1.5%
	5 x Base	1.000kΩ	5	
	6 x Base	1.240kΩ	6	
All MLCC Ceramic Output Capacitors Base capacitance = 8 x 100µF	Base	1.500kΩ	1	± 5%
	1.5 x Base	1.780kΩ	1.5	
	2 x Base	2.100kΩ	2	± 3%
	3 x Base	2.430kΩ	3	
	4 x Base	2.800kΩ	4	
	4.5 x Base	3.240kΩ	4.5	± 1.5%
POSCAP and Ceramic MLCC Output Capacitors Base capacitance = 4 x 330 µF (POSCAP) + 2 x 100 µF (Ceramic)	Base	3.740kΩ	1	± 5%
	1.5 x Base	4.220kΩ	1.5	
	2 x Base	4.750kΩ	2	± 3%
	2.5 x Base	5.360kΩ	2.5	
	3 x Base	6.040kΩ	3	± 1.5%
	3.5 x Base	6.810kΩ	3.5	
Reserved for User Programmed Compensation Values		7.680kΩ		
		8.660kΩ		
		9.530kΩ		
		10.500kΩ		
		11.800kΩ		
		13.000kΩ		
		14.300kΩ		
		15.800kΩ		
		17.400kΩ		
		19.100kΩ		
		21.000 kΩ		
		23.200 kΩ		

Table **10: Recommended Output Capacitors**

Description	Manufacturer	P/N
470µF, 2.5V, ESR 3mΩ SP-CAP	Panasonic	EEFGX0E471R
330µF, 6.3V, ESR 9 mΩ POSCAP	Panasonic	6TPF330M9L
330µF, 2.5V, ESR 9 mΩ POSCAP	Kemet	T520B337M2R5ATE009
100µF, 6.3V, X5R, 1206 Ceramic	Kemet	C1206C107M9PACTU
47µF, 6.3V, X5R 1206 Ceramic	Murata	GRM31CR60J476ME19L

OUTPUT CAPACITOR RECOMMENDATION

EM2140 is designed for fast transient response and low output ripple noise. The output capacitors should be low ESR polymer, tantalum or ceramic capacitor. **Error! Reference source not found.** shows different output capacitor combinations to optimize the load transient deviation performance. With the Rtune feature, the user can simply scale up the total output capacitance to meet further stringent transient requirement.

Please consult the documentation for your particular FPGA, ASIC, processor, or memory block for the transient and the bulk decoupling capacitor requirements.

INPUT CAPACITOR RECOMMENDATION

The EM2140 input should be decoupled with at least three 22µF 1206 case size and one 10µF 0805 case size MLCC ceramic capacitor's or four 22µF MLCC 1206 case size ceramic capacitors. More bulk capacitor may be needed only if there are long inductive traces at the input source or there is not enough source capacitance.

These input decoupling ceramic capacitors can be mounted on the PCB back-side to reduce the solution size. These input filter capacitors should have the appropriate voltage rating for the input voltage on PVIN, and use a X5R, X7R, or equivalent dielectric rating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

The PVCC pin provides power to the gate drive of the internal high/low side power MOSFETs. The VCC pin provides power to the internal digital controller. These two power inputs share the same supply voltage (5V nominal), and should be bypassed with a single 2.2µF MLCC capacitor. To avoid switching noise injection from PVCC to VCC, it is recommended a ferrite bead is inserted between PVCC and VCC pins as shown Figure 14.

PROTECTION FEATURES

The EM2140 offers a complete suite of programmable fault warnings and protections. Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored. A dedicated ADC is used to provide fast and accurate current information during the entire switching period to provide fast Over-Current Protection (OCP) response.

To prevent damage to the load, the EM2140 utilizes an output over-voltage protection circuit. The voltage at VSENP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, a fault response is generated and the PWM output is turned off.

The output voltage is also sampled, filtered, and compared with an output over-voltage warning threshold. If the output voltage exceeds this threshold, a warning is generated and the preconfigured actions are triggered. The EM2140 also monitors the output voltage with two lower thresholds. If the output voltage is below the under-voltage warning level and above the under-voltage fault level, an output voltage under-voltage warning is triggered. If the output voltage falls below the fault level, a fault event is generated.

Similar to output over and under voltage protection, the EM2140 monitors the input voltage at VINSEN continuously with a configurable threshold. If the input voltage exceeds the over voltage threshold or is below the under voltage threshold, the default response is generated.

Over Temperature Protection (OTP) is based on direct monitoring of the device's internal temperature. If the temperature exceeds the OTP threshold, the device will enter a soft-stop mode slowly ramping the output voltage down until the temperature falls below the default recovery temperature.

The default fault response is zero delay and latch off for most fault conditions. The CTRL pin may be cycled to clear the latch. Table **11** summarizes the default configurations that have been pre-programmed to the device.

Table 11: Fault Configuration OverviewTable

Signal	Fault Level	Default Response Type	Delay (ms)	Retries
Output Over-Voltage	Warning		0	None
	Fault	High-impedance		
Output Under-Voltage	Warning		0	None
	Fault	High-impedance		
Input Over-Voltage	Warning		0	None
	Fault	High-impedance		
Input Under-Voltage	Warning		0	Infinity
	Fault	High-impedance		
Over-Current	Warning		0	None
	Fault	High-impedance		
Internal Over-Temperature	Warning		0	Infinity
	Fault	Soft Off		

FUNCTIONAL DESCRIPTION: ADVANCED CONFIGURATION

All EM2140 modules are delivered with a pre-programmed default configuration, allowing the module to be powered up without a need to configure the device or even the need for the GUI to be connected. However, a PMBus version 1.2 compliant interface allows access to an extensive suite of digital communication and control commands. This includes configuring the EM2140 for optimum performance, setting various parameters such as output voltage, and monitoring and reporting device behavior including output voltage, output current, and fault responses.

The device may be reconfigured multiple times without storing the configuration into the non-volatile memory (NVM). Any configuration changes will be lost upon power-on reset unless specifically stored into NVM using either STORE_DEFAULT_ALL or STORE_DEFAULT_CODE PMBus commands. Please see Table 14 for more details.

For RVSET and RTUNE configurations, there is no reprogramming permitted.

After writing a new configuration to NVM, the user may still make changes to the device configuration through the PMBus interface; however, now upon power cycling the device, the stored NVM configuration will be recalled upon power-up rather than the factory default configuration of the EM2140.

The NVM configuration can be stored three times in its entirety. However, the consumption of the available NVM is dynamic, based on the configuration parameters that have actually changed. The unused NVM information is given in the GUI or through the manufacture specific command MFR_STORE_PARAMS_REMAINING.

INTEL DIGITAL POWER CONFIGURATOR

The Intel Enpirion Digital Power Configurator is a Graphical User Interface (GUI) software which allows the EM2140 to be controlled via a USB interface to a host computer.

The user can view the power supply's status, I/O voltages, output current and fault conditions detected by the device, program settings to the converter, and issue PMBus commands using the GUI. Most of the parameters (for example, VOUT turn on/off time, protection and fault limits) can be configured and adjusted within the GUI environment. These parameters can also be configured outside of the GUI environment using the relevant PMBus™ commands.

The GUI also allows the user to easily create, modify, test and save a configuration file which may then be used to permanently burn the configuration into NVM within a production test environment.

ALTERNATIVE OUTPUT VOLTAGE CONTROL METHODS

In the default configuration, output voltage selection is determined at power-up by the pin-strapped resistor RVSET. This functionality can be disabled using the PMBus command MFR_PIN_CONFIG. When RVSET is disabled, the output voltage will be determined by the nominal output voltage setting in the user configuration. The EM2140 supports a subset of the output voltage commands outlined in the PMBus specification. For example, the output voltage can be dynamically changed using the PMBus command VOUT_COMMAND. When the output is being changed by the PMBus command, power good (POK) remains at a logic high.

POWER SEQUENCING AND THE CONTROL (CTRL) PIN

Three different configuration options are supported to enable the output voltage. The device can be configured to turn on after an OPERATION_ON command, via the assertion of the CTRL pin or a combination of both per the PMBus convention. The EM2140 supports power sequencing features including programmable ramp up/down and delays. The typical sequence of events is shown in Figure 6 and follows the PMBus standard. The individual timing values shown in Figure 6 and Figure 7 can be configured using the appropriate configuration setting in Intel Digital Power Configurator GUI.

PRE-BIASED START-UP AND SOFT-STOP

In systems with complex power architectures, there may be leakage paths from one supply domain which may charge capacitors in another supply domain leading to a pre-biased condition on one or more power supplies. This condition is not ideal and can be avoided through careful design, but is generally not harmful. Attempting to discharge the pre-bias is not advised as it may force high current though the leakage path. The EM2140 includes features to enable and disable into pre-biased output capacitors.

If the output capacitors are pre-biased when the EM2140 is enabled, start-up logic in the EM2140 ensures that the output does not pull down the pre-biased voltage and the t_{ON_RISE} timing is preserved. Closed-loop stability is ensured during the entire start-up sequence under all pre-bias conditions.

The EM2140 also supports pre-biased off, in which the output voltage ramp down to a user-defined level (V_{OFF_nom}) rather than to zero. After receiving the disable command, via PMBus command or the CTRL pin, the EM2140 ramps down the output voltage to the predefined value. Once the value is reached, the output driver goes into a tristate mode to avoid excessive currents through the leakage path.

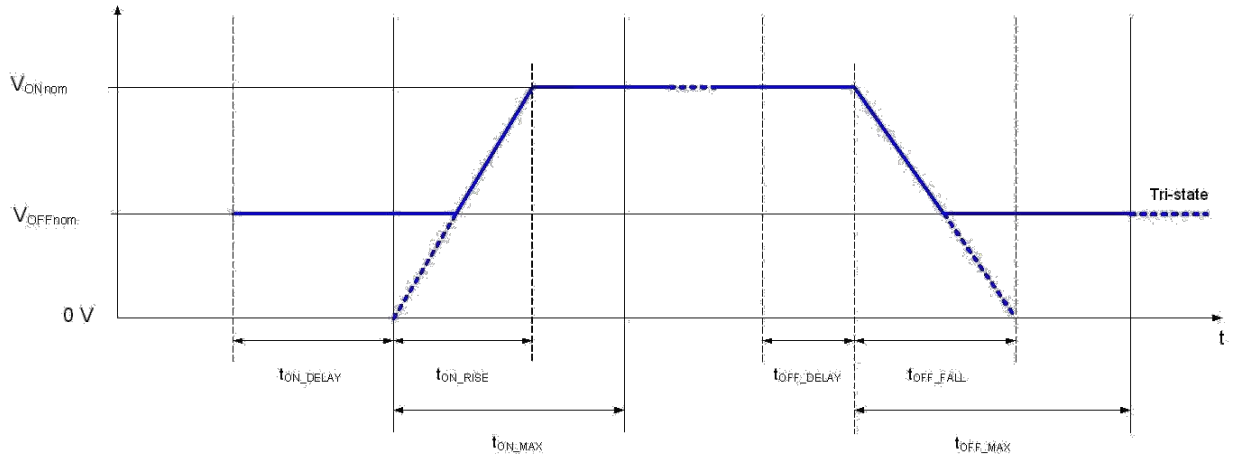


Figure 7: Power Sequencing With Non-Zero Off Voltage

VOLTAGE TRACKING

The EM2140 can control the output voltage based on the external voltage applied to the VTRACK pin, thus allowing sequencing of the output voltage from an external source. Pre-bias situations are also supported. The VTRACK pin voltage is a single-ended input referenced to analog ground. Tracking mode is disabled by default, but it can be enabled using the GUI software or via the manufacturer-specific PMBus command, MFR_FEATURES_CTRL see Table 14.

If VTRACK is not intended to be used, tie the VTRACK pin low or leave it floating.

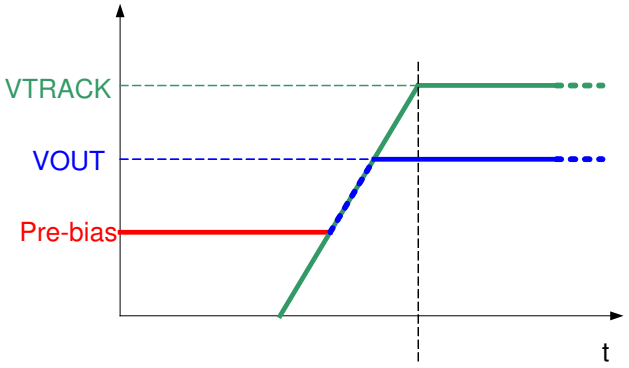


Figure 8: Power Sequencing Using VTRACK With Bias Voltage On VOUT

The set point voltage for the EM2140 is defined by the lower value of the V_{OUT} setting or an external voltage applied to the VTRACK pin. If the VTRACK voltage rises above the V_{OUT} set point voltage, then the final output voltage will be limited by the V_{OUT} setting. If the tracking feature is enabled, but the VTRACK pin is tied low or floating, then the output will never start as the VTRACK pin input is always the lower value and will always be in control. Conversely, if tracking is enabled, but VTRACK is tied high, the output will start but will follow the V_{OUT} set point, not the VTRACK pin.

If tracking is used for sequencing, it is recommended that the VTRACK signal be kept greater than the V_{OUT} voltage. This ensures that the internal V_{OUT} set point is used as the final steady-state output voltage and accuracy is not a function of the externally applied VTRACK voltage. The tracking function will override a programmed pre-bias off level (V_{OFF_nom}).

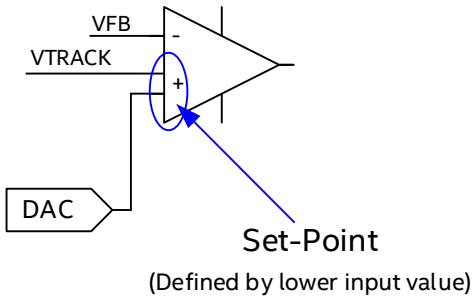


Figure 9: VTRACK Circuitry

The following figures demonstrate ratio-metric and simultaneous sequencing of the output voltage, which can be accomplished by applying an appropriate external voltage on the VTRACK pin. When using the VTRACK feature, the sequencing will be ratio-metric as shown in Figure 12 if an external resistor network is used at the VTRACK pin as shown Figure 10. If no external resistors are used, the output sequence is simultaneous as shown in Figure 13.

In the event that a feedback divider is not required, (such as when VOUT ≤ 1.4V) but the tracking voltage applied to VTRACK is greater than 1.4V, then a 2kΩ resistor is required in series with the VTRACK pin to minimize leakage current as shown in Figure 11.

In applications where a voltage divider is required on the output voltage, a voltage divider consisting of the same values is also required for the VTRACK pin.