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## Features

- 32-bit ARM® Cortex -M3 processor
- 2.4 GHz IEEE 802.15.4-2003 transceiver & lower MAC
- 128 or 192 kB flash, with optional read protection
- 12 kB RAM memory
- AES128 encryption accelerator
- Flexible ADC, UART/SPI/TWI serial communications, and general purpose timers
- 24 highly configurable GPIOs with Schmitt trigger inputs

## Industry-leading ARM® Cortex -M3 processor

- Leading 32-bit processing performance
- Highly efficient Thumb-2 instruction set
- Operation at 6, 12, or 24 MHz
- Flexible Nested Vectored Interrupt Controller

## Low power consumption, advanced management

- RX Current (w/ CPU): 26 mA
- TX Current (w/ CPU, +3 dBm TX): 31 mA
- Low deep sleep current, with retained RAM and GPIO: 400 nA without/800 nA with sleep timer
- Low-frequency internal RC oscillator for low-power sleep timing
- High-frequency internal RC oscillator for fast (110 μs) processor start-up from sleep

## Exceptional RF Performance

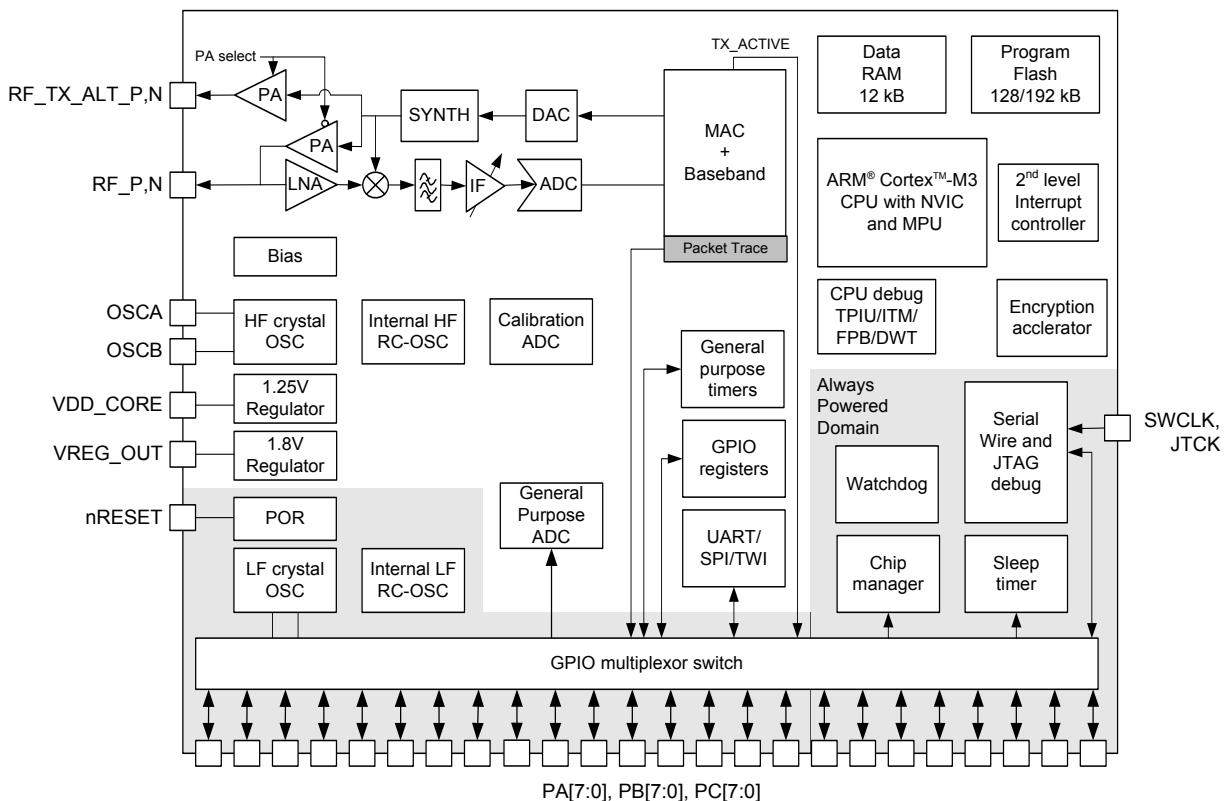
- Normal mode link budget up to 103 dB; configurable up to 110 dB
- -100 dBm normal RX sensitivity; configurable to -102 dBm (1% PER, 20 byte packet)
- +3 dB normal mode output power; configurable up to +8 dBm
- Robust Wi-Fi and Bluetooth coexistence

## Innovative network and processor debug

- Packet Trace Port for non-intrusive packet trace with Ember development tools
- Serial Wire/JTAG interface
- Standard ARM debug capabilities: Flash Patch & Breakpoint; Data Watchpoint & Trace; Instrumentation Trace Macrocell

## Application Flexibility

- Single voltage operation: 2.1–3.6 V with internal 1.8 and 1.25 V regulators
- Optional 32.768 kHz crystal for higher timer accuracy
- Low external component count with single 24 MHz crystal
- Support for external power amplifier
- Small 7x7 mm 48-pin QFN package



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## 1. Typical Application

Figure 1.1 illustrates the typical application circuit, and Table 1.1 contains an example bill of materials (BOM) for the off-chip components required by the EM35x.

**Note:** The circuit shown in Figure 1.1 is for example purposes only, and the BOM is for budgetary quotes only. For a complete reference design, please download one of the latest Ember Hardware Reference Designs from the Silicon Labs website ([www.silabs.com/zigbee-support](http://www.silabs.com/zigbee-support)).

The Balun provides an impedance transformation from the antenna to the EM35x for both TX and RX modes.

L1 tunes the impedance presented to the RF port for maximum transmit power and receive sensitivity.

The harmonic filter (L2, L3, C5, C6 and C9) provides additional suppression of the second harmonic, which increases the margin over the FCC limit.

The 24 MHz crystal Y1 with loading capacitors is required and provides the high-frequency crystal oscillator source for the EM35x's main system clock. The 32.768 kHz crystal with loading capacitors generates a highly accurate low-frequency crystal oscillator for use with peripherals, but it is not mandatory as the low-frequency internal RC oscillator can be used.

Loading capacitance and ESR (C1 and R3) provides stability for the internal 1.8 V regulator.

Loading capacitance C2 provides stability for the internal 1.25 V regulator, no ESR is required because it is contained within the chip.

Resistor R1 reduces the operating voltage of the flash memory, this reduces current consumption and improves sensitivity by 1 dB when compared to not using it.

Various decoupling capacitors are required, these should be placed as close to their corresponding pins as possible. For values and locations see one of the latest reference designs.

An antenna matched to 50  $\Omega$  is required.

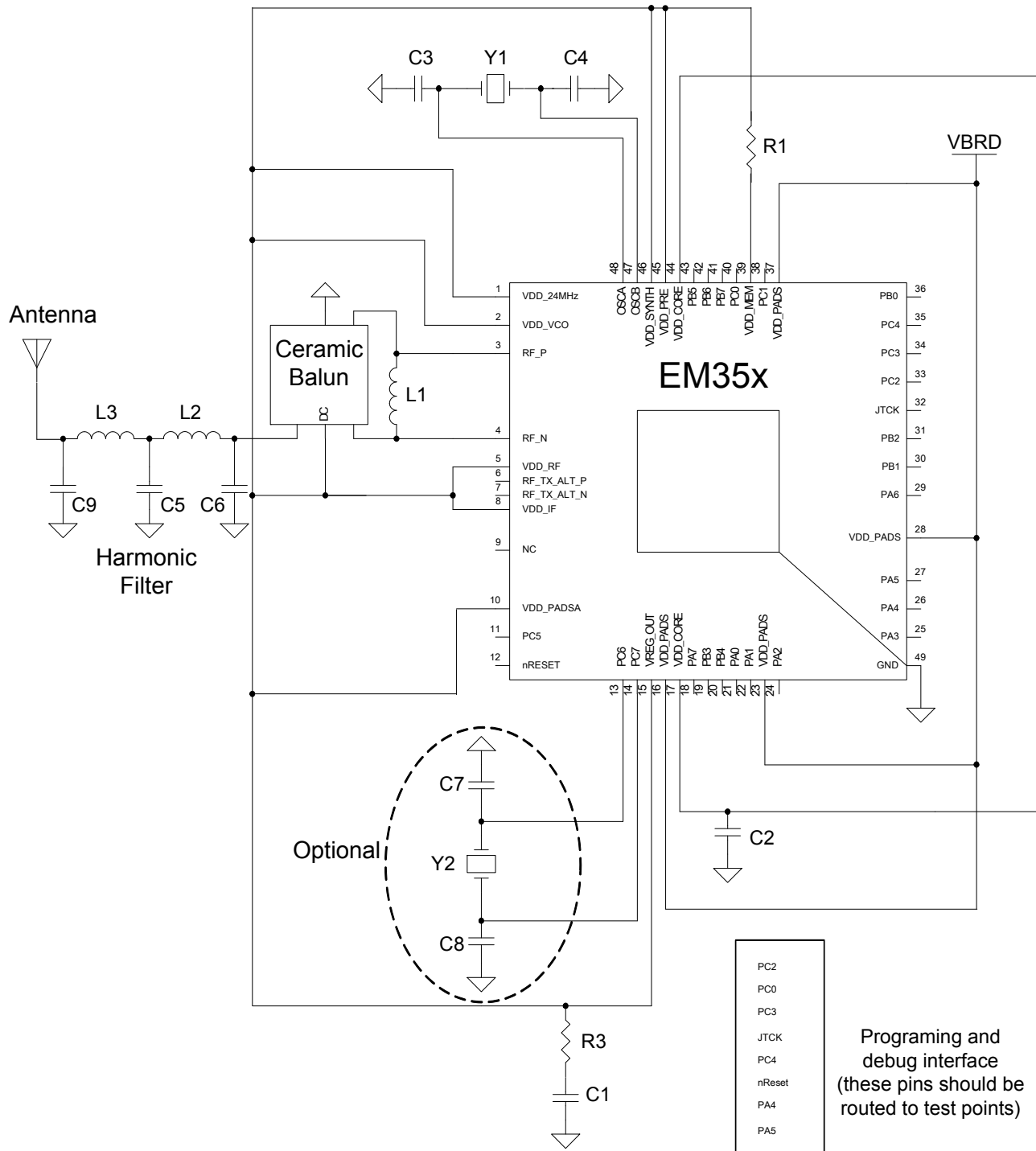


Figure 1.1. Typical Application Circuit

Table 1.1 contains a typical Bill of Materials for the application circuit shown in Figure 1.1. The information within this table should be used for a rough cost analysis. For a more detailed BOM, please refer to one of Ember EM35x-based reference designs at the Silicon Labs website ([www.silabs.com/zigbee-support](http://www.silabs.com/zigbee-support)).

**Table 1.1. Bill of Materials for Typical Application Circuit**

Item	Qty	Reference	Description	Manufacturer
1	1	C2	CAPACITOR, 1 $\mu$ F, 6.3 V, X5R, 10%, 0402	<not specified>
2	1	C1	CAPACITOR, 2.2 $\mu$ F, 10 V, X5R, 10%, 0603	<not specified>
3	1	C7	CAPACITOR, 22 pF, $\pm$ 5%, 50 V, NPO, 0402	<not specified>
4	2	C3,C4	CAPACITOR, 18 pF, $\pm$ 5%, 50 V, NPO, 0402	<not specified>
5	1	C8	CAPACITOR, 33 pF, $\pm$ 5%, 50 V, NPO, 0402	<not specified>
6	2	C5, C9	CAPACITOR, 1 pF, $\pm$ 0.25 pF, 50 V, 0402, NPO	<not specified>
7	1	C6	CAPACITOR, 1.8 pF, $\pm$ 0.25 pF, 50 V, 0402, NPO	
8	1	L1	INDUCTOR, 5.1 nH, $\pm$ 0.3 nH, 0402 MULTILAYER	Murata LQG15HS5N1
9	2	L2, L3	INDUCTOR, 2.7 nH, $\pm$ 0.3 nH, 0402, MULTILAYER	Murata LQG15HS2N7
10	1	R1	RESISTOR, 10 $\Omega$ , 5%, 0402	<not specified>
11	1	R3	RESISTOR, 1 $\Omega$ , 5%, 0402	<not specified>
12	1	U1	EM35x SINGLE-CHIP ZIGBEE/802.15.4-2003 SOLUTION	Ember EM35x
13	1	Y1	CRYSTAL, 24.000 MHz, $\pm$ 25 ppm STABILITY OVER $-40$ to $+85$ $^{\circ}$ C, 18 pF	ILSI, Abracon, KDS, Epson
14	1	Y2 (Optional)	CRYSTAL, 32.768 kHz, $\pm$ 20 ppm INITIAL TOLERANCE AT $+25^{\circ}$ C, 12.5 pF	Abracon, KDS, Epson
15	1	BLN1	BALUN, CERAMIC 50/200 $\Omega$	Würth 748421245 Johanson 2450BL15B100E Murata LDB212G4010C
16	1	ANT1	ANTENNA	Johanson 2450AT18B100E



## 2. Electrical Specifications

### 2.1. Absolute Maximum Ratings

Table 2.1 lists the absolute maximum ratings for the EM35x.

**Table 2.1. Absolute Maximum Ratings**

Parameter	Test Condition	Min	Max	Unit
Regulator input voltage (VDD_PADS)		-0.3	+3.6	V
Analog, Memory and Core voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_MEM, VDD_PRE, VDD_SYNTH, VDD_CORE)		-0.3	+2.0	V
Voltage on RF_P,N; RF_TX_ALT_P,N		-0.3	+3.6	V
RF Input Power (for max level for correct packet reception see Table 2.7)	RX signal into a lossless balun	—	+15	dBm
Voltage on any GPIO (PA[7:0], PB[7:0], PC[7:0]), SWCLK, nRESET, VREG_OUT		-0.3	VDD_PAD S +0.3	V
Voltage on any GPIO pin (PA4, PA5, PB5, PB6, PB7, PC1), when used as an input to the general purpose ADC		-0.3	2.0	V
Voltage on OSCA, OSCB, NC		-0.3	VDD_PAD SA +0.3	V
Storage temperature		-40	+140	°C

**Note:** Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 2.2. Recommended Operating Conditions

Table 2.2 lists the rated operating conditions of the EM35x.

**Table 2.2. Operating Conditions**

Parameter	Test Condition	Min	Typ	Max	Unit
Regulator input voltage (VDD_PADS)		2.1	—	3.6	V
Analog and memory input voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_MEM, VDD_PRE, VDD_SYNTH)		1.7	1.8	1.9	V
Core input voltage when supplied from internal regulator (VDD_CORE)		1.18	1.25	1.32	V
Core input voltage when supplied externally (VDD_CORE)		1.18	—	1.9	V
Operating temperature range, T <sub>A</sub>		-40	—	+85	°C

**Note:** Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 2.3. Environmental Characteristics

Table 2.3 lists the rated environmental characteristics of the EM35x.

**Table 2.3. Environmental Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ESD (human body model)		On any pin	—	—	±2	kV
ESD (charged device model)		Non-RF pins	—	—	±400	V
ESD (charged device model)		RF pins	—	—	±225	V
Package Thermal Resistance*	$\theta_{JA}$		27.1			°C/W

\*Note: Thermal resistance assumes multi-layer PCB with exposed pad soldered to a PCB board.

## 2.4. DC Electrical Characteristics

Table 2.4 lists the dc electrical characteristics of the EM35x.

**Table 2.4. DC Characteristics**

Measured on Silicon Labs' EM357 reference design with  $T_A = 25\text{ °C}$  and  $V_{DD} = 3\text{ V}$ , unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
Regulator input voltage (VDD_PADS)		2.1	—	3.6	V
Power supply range (VDD_MEM)	Regulator output or external input	1.7	1.8	1.9	V
Power supply range (VDD_CORE)	Regulator output	1.18	1.25	1.32	V
<b>Deep Sleep Current</b>					
Quiescent current, internal RC oscillator disabled	−40 °C, VDD_PADS=3.6 V	—	0.4	—	μA
	+25 °C, VDD_PADS=3.6 V	—	0.4	—	μA
	+85 °C, VDD_PADS=3.6 V	—	0.7	—	μA
Quiescent current, including internal RC oscillator	−40 °C, VDD_PADS=3.6 V	—	0.7	—	μA
	+25 °C, VDD_PADS=3.6 V	—	0.7	—	μA
	+85 °C, VDD_PADS=3.6 V	—	1.1	—	μA
Quiescent current, including 32.768 kHz oscillator	−40 °C, VDD_PADS=3.6 V	—	0.8	—	μA
	+25 °C, VDD_PADS=3.6 V	—	1.0	—	μA
	+85 °C, VDD_PADS=3.6 V	—	1.5	—	μA
Quiescent current, including internal RC oscillator and 32.768 kHz oscillator	−40 °C, VDD_PADS=3.6 V	—	1.1	—	μA
	+25 °C, VDD_PADS=3.6 V	—	1.3	—	μA
	+85 °C, VDD_PADS=3.6 V	—	1.8	—	μA
Simulated deep sleep (debug mode) current	With no debugger activity	—	300	—	μA

**Table 2.4. DC Characteristics (Continued)**Measured on Silicon Labs' EM357 reference design with  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ , unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
<b>Reset Current</b>					
Quiescent current, nRESET asserted	Typ at 25 °C/3.0 V Max at 85 °C/3.6 V	—	1.2	2.0	mA
<b>Processor and Peripheral Currents</b>					
ARM® Cortex™-M3, RAM, and flash memory	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 running at 12 MHz from crystal oscillator Radio and all peripherals off	—	6.5	—	mA
ARM® Cortex™-M3, RAM, and flash memory	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 running at 24 MHz from crystal oscillator Radio and all peripherals off	—	7.5	—	mA
ARM® Cortex™-M3, RAM, and flash memory sleep current	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz from the crystal oscillator Radio and all peripherals off	—	3.0	—	mA
ARM® Cortex™-M3, RAM, and flash memory sleep current	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 6 MHz from the high frequency RC oscillator Radio and all peripherals off	—	2.0	—	mA
Serial controller current	For each controller at maximum data rate	—	0.2	—	mA
General purpose timer current	For each timer at maximum clock rate	—	0.25	—	mA
General purpose ADC current	At maximum sample rate, DMA enabled	—	1.1	—	mA
<b>RX Current</b>					
Radio receiver, MAC, and base-band	ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz	—	22.0	—	mA
Total RX current ( = $I_{\text{Radio receiver, MAC and baseband, CPU + IRAM, and Flash memory}}$ )	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 12 MHz	—	25.5	—	mA
	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 24 MHz	—	26.5	—	mA
Boost mode total RX current ( = $I_{\text{Radio receiver, MAC and base-band, CPU+ IRAM, and flash memory}}$ )	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 12 MHz	—	27.5	—	mA
	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 24 MHz	—	28.5	—	mA

**Table 2.4. DC Characteristics (Continued)**Measured on Silicon Labs' EM357 reference design with  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ , unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
<b>TX Current</b>					
Radio transmitter, MAC, and baseband	25 °C and 1.8 V core; max. power out (+3 dBm typical) ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz	—	26.0	—	mA
Total TX current (= $I_{\text{Radio transmitter, MAC and baseband, CPU + IRAM, and flash memory}}$ )	25 °C, VDD_PADS=3.0 V; maximum power setting (+8 dBm); ARM® Cortex™-M3 running at 12 MHz	—	42.5	—	mA
	25 °C, VDD_PADS=3.0 V; +3 dBm power setting; ARM® Cortex™-M3 running at 12 MHz	—	30.0	—	mA
	25 °C, VDD_PADS=3.0 V; 0 dBm power setting; ARM® Cortex™-M3 running at 12 MHz	—	27.5	—	mA
	25 °C, VDD_PADS=3.0 V; minimum power setting; ARM® Cortex™-M3 running at 12 MHz	—	21.5	—	mA
	25 °C, VDD_PADS=3.0 V; maximum power setting (+8 dBm); ARM® Cortex™-M3 running at 24 MHz	—	43.5	—	mA
	25 °C, VDD_PADS=3.0 V; +3 dBm power setting; ARM® Cortex™-M3 running at 24 MHz	—	31.0	—	mA
	25 °C, VDD_PADS=3.0 V; 0 dBm power setting; ARM® Cortex™-M3 running at 24 MHz	—	28.5	—	mA
	25 °C, VDD_PADS=3.0 V; minimum power setting; ARM® Cortex™-M3 running at 24 MHz	—	22.5	—	mA

Figure 2.1 shows the variation of current in transmit mode (with the ARM® Cortex™-M3 running at 12 MHz).

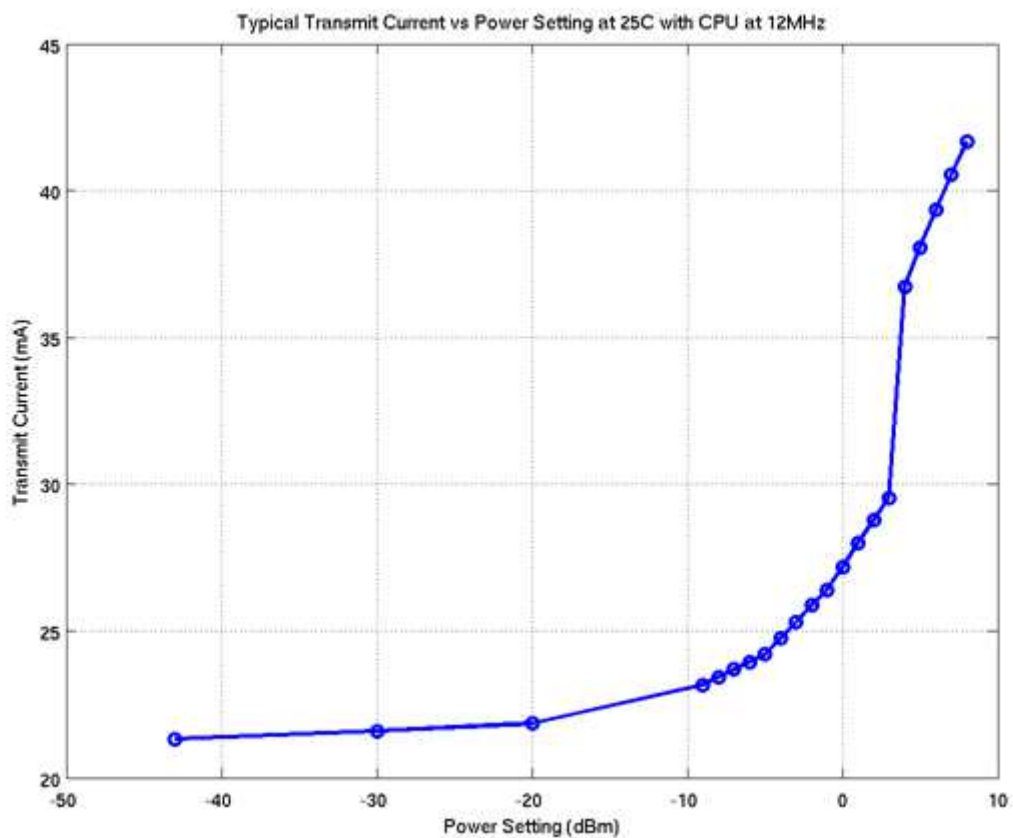


Figure 2.1. Transmit Power Consumption

Figure 2.2 shows typical output power against power setting on the Silicon Labs reference design.

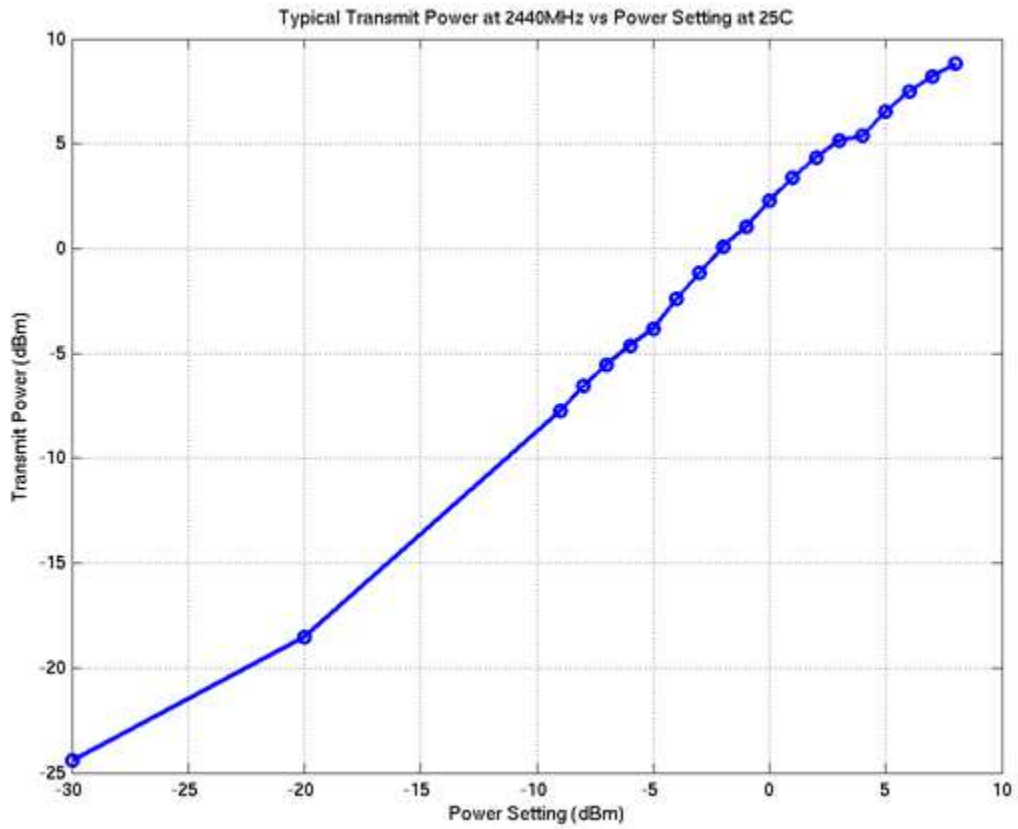


Figure 2.2. Transmit Output Power

## 2.5. Digital I/O Specifications

Table 2.5 lists the digital I/O specifications for the EM35x. The digital I/O power (named VDD\_PADS) comes from three dedicated pins (pins 23, 28 and 37). The voltage applied to these pins sets the I/O voltage.

**Table 2.5. Digital I/O Specifications**

Parameter	Test Condition	Min	Typ	Max	Unit
Voltage supply (regulator input voltage)		2.1	—	3.6	V
Low Schmitt switching threshold	$V_{SWIL}$ Schmitt input threshold going from high to low	0.42 x VDD_PADS	—	0.50 x VDD_PADS	V
High Schmitt switching threshold	$V_{SWIH}$ Schmitt input threshold going from low to high	0.62 x VDD_PADS	—	0.80 x VDD_PADS	V
Input current for logic 0	$I_{IL}$	—	—	-0.5	$\mu$ A
Input current for logic 1	$I_{IH}$	—	—	+0.5	$\mu$ A
Input pull-up resistor value	$R_{IPU}$	24	29	34	k $\Omega$
Input pull-down resistor value	$R_{IPD}$	24	29	34	k $\Omega$
Output voltage for logic 0	$V_{OL}$ ( $I_{OL} = 4$ mA for standard pads, 8 mA for high current pads)	0	—	0.18 x VDD_PADS	V
Output voltage for logic 1	$V_{OH}$ ( $I_{OH} = 4$ mA for standard pads, 8 mA for high current pads)	0.82 x VDD_PADS	—	VDD_PADS	V
Output source current (standard current pad)	$I_{OHS}$	—	—	4	mA
Output sink current (standard current pad)	$I_{OLS}$	—	—	4	mA
Output source current high current pad: PA6, PA7, PB6, PB7, PC0	$I_{OHH}$	—	—	8	mA
Output sink current high current pad: PA6, PA7, PB6, PB7, PC0	$I_{OLH}$	—	—	8	mA
Total output current (for I/O Pads)	$I_{OH} + I_{OL}$	—	—	40	mA

Table 2.6 lists the nRESET pin specifications for the EM35x. The digital I/O power (named VDD\_PADS) comes from three dedicated pins (pins 23, 28 and 37). The voltage applied to these pins sets the I/O voltage.

**Table 2.6. nReset Pin Specifications**

Parameter	Test Condition	Min	Typ	Max	Unit
Low Schmitt switching threshold	$V_{SWIL}$ Schmitt input threshold going from high to low	0.42 x VDD_PADS	—	0.50 x VDD_PADS	V
High Schmitt switching threshold	$V_{SWIH}$ Schmitt input threshold going from low to high	0.62 x VDD_PADS	—	0.80 x VDD_PADS	V
Input current for logic 0	$I_{IL}$	—	—	-0.5	$\mu$ A
Input current for logic 1	$I_{IH}$	—	—	+0.5	$\mu$ A
Input pull-up resistor value	$R_{IPU}$ Pull-up value while the chip is not reset	24	29	34	k $\Omega$
Input pull-up resistor value	$R_{IPURESET}$ Pull-up value while the chip is reset	12	14.5	17	k $\Omega$

## 2.6. Non-RF System Electrical Characteristics

Table 2.7 lists the non-RF system level characteristics for the EM35x.

**Table 2.7. Non-RF System Electrical Characteristics**

Measured on Silicon Labs' EM357 reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ , unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
System wake time from deep sleep	From wakeup event to first ARM <sup>®</sup> Cortex <sup>™</sup> -M3 instruction running from 6 MHz internal RC clock Includes supply ramp time and oscillator startup time	—	110	—	$\mu$ s
Shutdown time going into deep sleep	From last ARM <sup>®</sup> Cortex <sup>™</sup> -M3 instruction to deep sleep mode	—	5	—	$\mu$ s



## 2.7. RF Electrical Characteristics

### 2.7.1. Receive

Table 2.8 lists the key parameters of the integrated IEEE 802.15.4-2003 receiver on the EM35x.

Receive measurements were collected with the Silicon Labs EM35x Ceramic Balun Reference Design (Version A0) at 2440 MHz. The typical number indicates one standard deviation above the mean, measured at room temperature (25 °C). The min and max numbers were measured over process corners at room temperature.

**Table 2.8. Receive Characteristics**

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	—	2500	MHz
Sensitivity (boost mode)	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	—	-102	-96	dBm
Sensitivity	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	—	-100	-94	dBm
High-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	35	—	dB
Low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	35	—	dB
2 <sup>nd</sup> high-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	46	—	dB
2 <sup>nd</sup> low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	46	—	dB
High-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	39	—	dB
Low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	47	—	dB
2 <sup>nd</sup> high-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	49	—	dB
2 <sup>nd</sup> low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	49	—	dB
High-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	44	—	dB
Low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	47	—	dB

**Table 2.8. Receive Characteristics (Continued)**

Parameter	Test Condition	Min	Typ	Max	Unit
2 <sup>nd</sup> high-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	59	—	dB
2 <sup>nd</sup> low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	59	—	dB
Channel rejection for all other channels	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	40	—	dB
802.11g rejection centered at +12 MHz or -13 MHz	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	36	—	dB
Maximum input signal level for correct operation		0	—	—	dBm
Co-channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	—	-6	—	dBc
Relative frequency error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		-120	—	+120	ppm
Relative timing error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		-120	—	+120	ppm
Linear RSSI range	As defined by IEEE 802.15.4-2003	40	—	—	dB
RSSI Range		-90	—	-40	dBm

Figure 2.3 shows the variation of receive sensitivity with temperature for boost mode and normal mode for a typical chip.

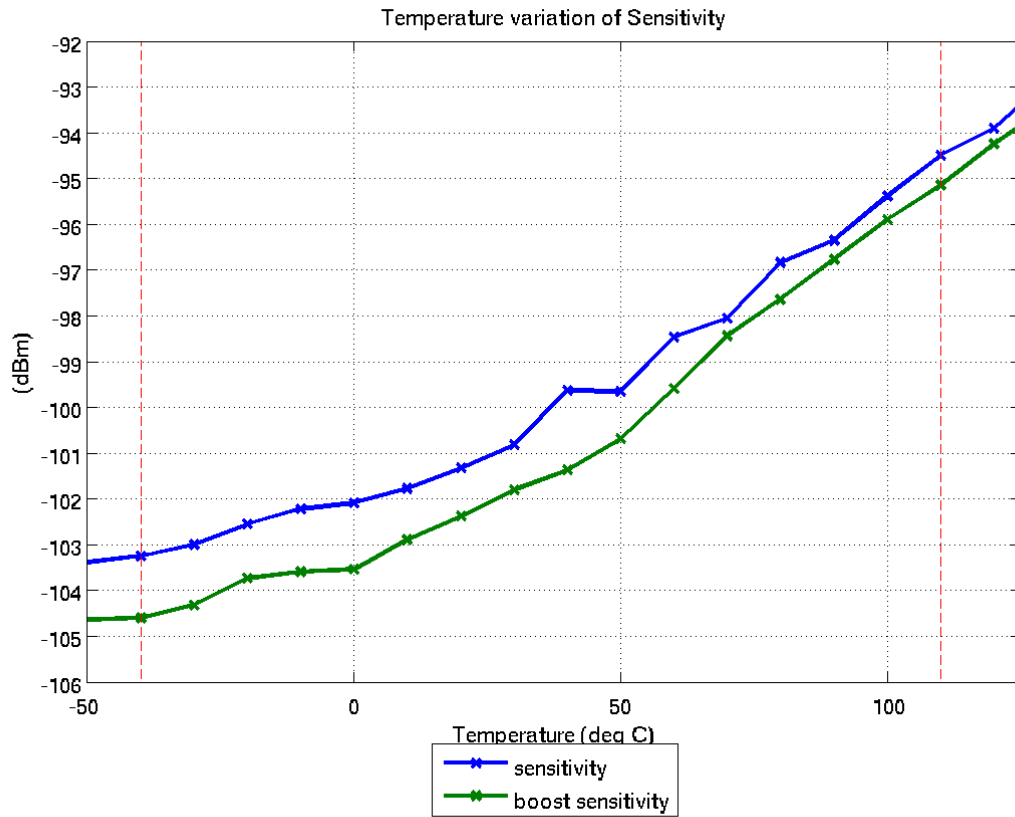


Figure 2.3. Receive Sensitivity vs. Temperature

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## 2.7.2. Transmit

Table 2.9 lists the key parameters of the integrated IEEE 802.15.4-2003 transmitter on the EM35x.

Transmit measurements were collected with the Silicon Labs EM35x Ceramic Balun Reference Design (Version A0) at 2440 MHz. The Typical number indicates one standard deviation below the mean, measured at room temperature (25 °C). The Min and Max numbers were measured over process corners at room temperature. In terms of impedance, this reference design presents a 3n3 inductor in parallel with a 100:50  $\Omega$  balun to the RF pins.

**Table 2.9. Transmit Characteristics**

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power (boost mode)	At highest boost mode power setting (+8)	—	8	—	dBm
Maximum output power	At highest normal mode power setting (+3)	1	5	—	dBm
Minimum output power	At lowest power setting	—	-55	—	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	—	5	15	%
Carrier frequency error		-40	—	+40	ppm
PSD mask relative	3.5 MHz away	-20	—	—	dB
PSD mask absolute	3.5 MHz away	-30	—	—	dBm

Figure 2.4 shows the variation of transmit power with temperature for maximum boost mode power, and normal mode for a typical chip.

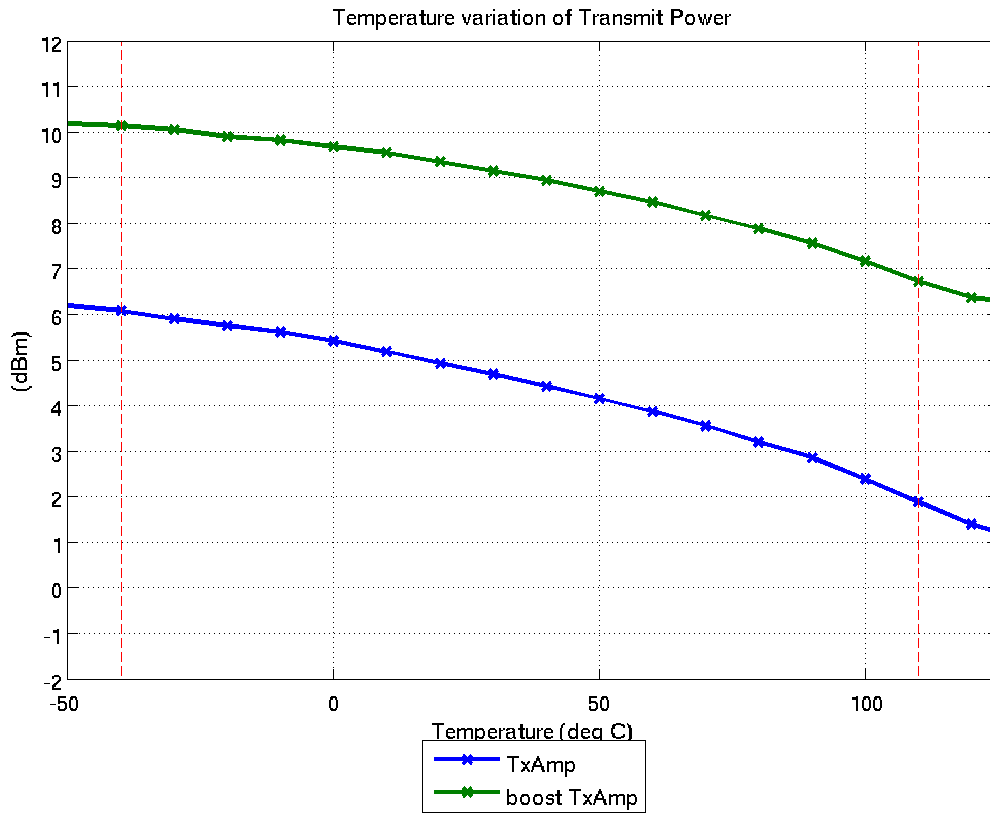


Figure 2.4. Transmit Power vs. Temperature

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### 2.7.3. Synthesizer

Table 2.10 lists the key parameters of the integrated synthesizer on the EM35x.

**Table 2.10. Synthesizer Characteristics**

Measured on Silicon Labs' EM357 reference design with  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ , unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	—	2500	MHz
Frequency resolution		—	11.7	—	kHz
Lock time	From off	—	—	100	$\mu\text{s}$
Relock time	Channel change or RX/TX turnaround (IEEE 802.15.4-2003 defines 192 $\mu\text{s}$ turnaround time)	—	—	100	$\mu\text{s}$
Phase noise at 100 kHz offset		—	-75	—	dBc/Hz
Phase noise at 1 MHz offset		—	-100	—	dBc/Hz
Phase noise at 4 MHz offset		—	-108	—	dBc/Hz
Phase noise at 10 MHz offset		—	-114	—	dBc/Hz

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### 3. Functional Description

The EM351 and EM357 are fully integrated system-on-chips that integrate a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM<sup>®</sup> Cortex-M3 microprocessor, flash and RAM memory, and peripherals of use to designers of ZigBee-based systems.

The transceiver uses an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15 dB. The integrated receive channel filtering allows for robust co-existence with other communication standards in the 2.4 GHz spectrum, such as IEEE 802.11-2007 and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high performance radio mode (boost mode) is software-selectable to boost dynamic range.

The integrated 32-bit ARM<sup>®</sup> Cortex™-M3 microprocessor is highly optimized for high performance, low power consumption, and efficient memory utilization. Including an integrated MPU, it supports two different modes of operation—privileged mode and user mode. This architecture could allow for separation of the networking stack from the application code, and prevents unwanted modification of restricted areas of memory and registers resulting in increased stability and reliability of deployed solutions.

The EM351 has 128 kB of embedded flash memory and the EM357 has 192 kB of embedded flash memory. Both chips have 12 kB of integrated RAM for data and program storage. The Ember software for the EM35x employs an effective wear-leveling algorithm that optimizes the lifetime of the embedded flash.

To maintain the strict timing requirements imposed by the ZigBee and IEEE 802.15.4-2003 standards, the EM35x integrates a number of MAC functions, AES128 encryption accelerator, and automatic CRC handling into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic backoff delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. The Ember Packet Trace Interface is also integrated with the MAC, allowing complete, non-intrusive capture of all packets to and from the EM35x with Ember development tools.

The EM35x offers a number of advanced power management features that enable long battery life. A high-frequency internal RC oscillator allows the processor core to begin code execution quickly upon waking. Various deep sleep modes are available with less than 1  $\mu$ A power consumption while retaining RAM contents. To support user-defined applications, on-chip peripherals include UART, SPI, TWI, ADC, and general-purpose timers, as well as up to 24 GPIOs. Additionally, an integrated voltage regulator, power-on-reset circuit, and sleep timer are available.

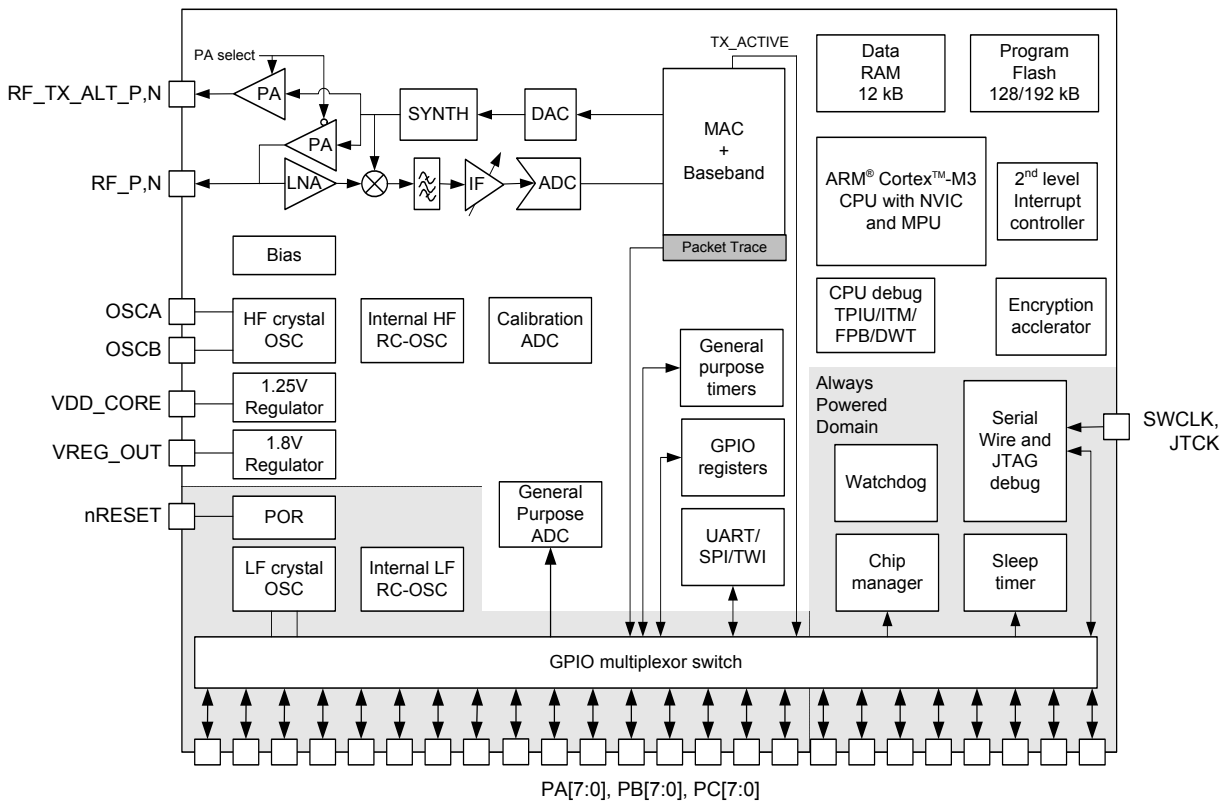
Finally, the EM35x utilizes standard Serial Wire and JTAG interfaces for powerful software debugging and programming of the ARM Cortex™-M3 core. The EM35x integrates the standard ARM system debug components: Flash Patch and Breakpoint (FPB), Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (ITM).

Target applications for the EM35x include the following:

- Smart Energy
- Building automation and control
- Home automation and control
- Security and monitoring
- General ZigBee wireless sensor networking

The technical data sheet details the EM35x features available to customers using it with Ember software.

Figure 3.1 shows a detailed block diagram of the EM35x.



**Figure 3.1. EM35x Block Diagram**

The EM35x radio receiver is a low-IF, super-heterodyne receiver. The architecture has been chosen to optimize co-existence with other devices in the 2.4 GHz band (namely Wi-Fi and Bluetooth), and to minimize power consumption. The receiver uses differential signal paths to reduce sensitivity to noise interference. Following RF amplification, the signal is downconverted by an image-rejecting mixer, filtered, and then digitized by an ADC.

The digital section of the receiver uses a coherent demodulator to generate symbols for the hardware-based MAC. The digital receiver also contains the analog radio calibration routines, and controls the gain within the receiver path.

The radio transmitter uses an efficient architecture in which the data stream directly modulates the VCO frequency. An integrated PA provides the output power. Digital logic controls TX path and output power calibration. If the EM35x is to be used with an external PA, use the TX\_ACTIVE or nTX\_ACTIVE signal to control the timing of the external switching logic.

The integrated 4.8 GHz VCO and loop filter minimize off-chip circuitry. Only a 24 MHz crystal with its loading capacitors is required to establish the PLL local oscillator signal.

The MAC interfaces the on-chip RAM to the RX and TX baseband modules. The MAC provides hardware-based IEEE 802.15.4-2003 packet-level filtering. It supplies an accurate symbol time base that minimizes the synchronization effort of the Ember software and meets the protocol timing requirements. In addition, it provides timer and synchronization assistance for the IEEE 802.15.4-2003 CSMA-CA algorithm.

The EM35x integrates hardware support for a packet trace module, which allows robust packet-based debug. This element is a critical component of Ember Desktop, the Ember development environment, and provides advanced network debug capability when used with the Ember Debug Adapter (ISA3).

The EM35x integrates an ARM® Cortex™-M3 microprocessor, revision r1p1. This industry-leading core provides 32-bit performance and is very power-efficient. It has excellent code density using the ARM® Thumb-2 instruction set. The processor can be operated at 12 or 24 MHz when using the high-frequency crystal oscillator, or at 6 MHz



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or 12 MHz when using the high-frequency internal RC oscillator.

The EM351 has 128 kB of flash memory and the EM357 has 192 kB of flash memory. Both chips have 12 kB of RAM on-chip, and the ARM configurable memory protection unit (MPU).

The EM35x implements both the ARM Serial Wire and JTAG debug interfaces. These interfaces provide real time, non-intrusive programming and debugging capabilities. Serial Wire and JTAG provide the same functionality, but are mutually exclusive. The Serial Wire interface uses two pins; the JTAG interface uses five. Serial Wire is preferred, since it uses fewer pins.

The EM35x contains 24 GPIO pins shared with other peripheral or alternate functions. Because of flexible routing within the EM35x, external devices can use the alternate functions on a variety of different GPIOs. The integrated serial controller SC1 can be configured for SPI (master or slave), TWI (master-only), or UART operation, and the serial controller SC2 can be configured for SPI (master or slave) or TWI (master-only) operation.

The EM35x has a general purpose ADC which can sample analog signals from six GPIO pins in single-ended or differential modes. It can also sample the 1.8 V regulated supply VDD\_PADSA, the voltage reference VREF, and GND. The ADC has one voltage range: 0 to 1.2 V (normal). The ADC has a DMA mode to capture samples and automatically transfer them into RAM. The integrated voltage reference for the ADC, VREF, can be made available to external circuitry. An external voltage reference can also be driven into the ADC. The regulator input voltage, VDD\_PADS, cannot be measured using the general purpose ADC, but it can be measured through Ember software.

The EM35x contains four oscillators: a high-frequency 24 MHz external crystal oscillator, a high-frequency 12 MHz internal RC oscillator, an optional low-frequency 32.768 kHz external crystal oscillator, and a low-frequency 10 kHz internal RC oscillator.

The EM35x has an ultra low power, deep sleep state with a choice of clocking modes. The sleep timer can be clocked with either the external 32.768 kHz crystal oscillator or with a 1 kHz clock derived from the internal 10 kHz RC oscillator. Alternatively, all clocks can be disabled for the lowest power mode. In the lowest power mode, only external events on GPIO pins will wake up the chip. The EM35x has a fast startup time (typically 110  $\mu$ s) from deep sleep to the execution of the first ARM<sup>®</sup> Cortex<sup>™</sup>-M3 instruction.

The EM35x contains three power domains. The always-on high voltage supply powers the GPIO pads and critical chip functions. Regulated low voltage supplies power the rest of the chip. The low voltage supplies are disabled during deep sleep to reduce power consumption. Integrated voltage regulators generate regulated 1.25 V and 1.8 V voltages from an unregulated supply voltage. The 1.8 V regulator output is decoupled and routed externally to supply analog blocks, RAM, and flash memories. The 1.25 V regulator output is decoupled externally and supplies the core logic.

**Note:** The EM35x is not pin-compatible with the previous generation chip, the EM250, except for the RF section of the chip. Pins 1-11 and 45-48 are compatible, to ease migration to the EM35x.

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## 4. Radio Module

The radio module consists of an analog front end and digital baseband as shown in Figure 3.1 on page 23.

### 4.1. Receive (RX) Path

The RX path uses a low-IF, super-heterodyne receiver that rejects the image frequency using complex mixing and polyphase filtering. In the analog domain, the input RF signal from the antenna is first amplified and mixed down to a 4 MHz IF frequency. The mixers' output is filtered, combined, and amplified before being sampled by a 12 MSPS ADC. The digitized signal is then demodulated in the digital baseband. The filtering within the RX path improves the EM35x's co-existence with other 2.4 GHz transceivers such as Zigbee/ 802.15.4-2003, IEEE 802.11-2007, and Bluetooth radios. The digital baseband also provides gain control of the RX path, both to enable the reception of small and large wanted signals and to tolerate large interferers.

#### 4.1.1. RX Baseband

The EM35x RX digital baseband implements a coherent demodulator for optimal performance. The baseband demodulates the O-QPSK signal at the chip level and synchronizes with the IEEE 802.15.4-2003-defined preamble. An automatic gain control (AGC) module adjusts the analog gain continuously every  $\frac{1}{4}$  symbol until the preamble is detected. Once detected, the gain is fixed for the remainder of the packet. The baseband despreads the demodulated data into 4-bit symbols. These symbols are buffered and passed to the hardware-based MAC module for packet assembly and filtering.

In addition, the RX baseband provides the calibration and control interface to the analog RX modules, including the LNA, RX baseband filter, and modulation modules. The Ember software includes calibration algorithms that use this interface to reduce the effects of silicon process and temperature variation.

#### 4.1.2. RSSI and CCA

The EM35x calculates the RSSI over every 8-symbol period as well as at the end of a received packet. The linear range of RSSI is specified to be at least 40 dB over temperature. At room temperature, the linear range is approximately 60 dB (–90 dBm to –30 dBm input signal).

The EM35x RX baseband provides support for the IEEE 802.15.4-2003 RSSI CCA method. Clear channel reports busy medium if RSSI exceeds its threshold.

### 4.2. Transmit (TX) Path

The EM35x TX path produces an O-QPSK-modulated signal using the analog front end and digital baseband. The area- and power-efficient TX architecture uses a two-point modulation scheme to modulate the RF signal generated by the synthesizer. The modulated RF signal is fed to the integrated PA and then out of the EM35x.

#### 4.2.1. TX Baseband

The EM35x TX baseband in the digital domain spreads the 4-bit symbol into its IEEE 802.15.4-2003-defined 32-chip sequence. It also provides the interface for the Ember software to calibrate the TX module to reduce silicon process, temperature, and voltage variations.

#### 4.2.2. TX\_ACTIVE and nTX\_ACTIVE Signals

For applications requiring an external PA, two signals are provided called TX\_ACTIVE and nTX\_ACTIVE. These signals are the inverse of each other. They can be used for external PA power management and RF switching logic. In transmit mode the TX baseband drives TX\_ACTIVE high, as described in Table 7.5 on page 57. In receive mode the TX\_ACTIVE signal is low. TX\_ACTIVE is the alternate function of PC5, and nTX\_ACTIVE is the alternate function of PC6. See "7. GPIO (General Purpose Input/Output)" on page 50 for details of the alternate GPIO functions. The digital I/O that provide these signals have a 4 mA output sink and source capability.

### 4.3. Calibration

The Ember software calibrates the radio using dedicated hardware resources.