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Complete System-on-Chip
- 32-bit ARM® Cortex -M3 processor
- 2.4 GHz IEEE 802.15.4-2003 transceiver & lower MAC
- 256 or 512 kB flash, with optional read protection
- 32 or 64 kB RAM memory
- AES128 encryption accelerator
- Flexible ADC, UART/SPI/TWI serial communications, and general purpose timers
- Optional USB serial communications
- 24 highly configurable GPIOs with Schmitt trigger inputs

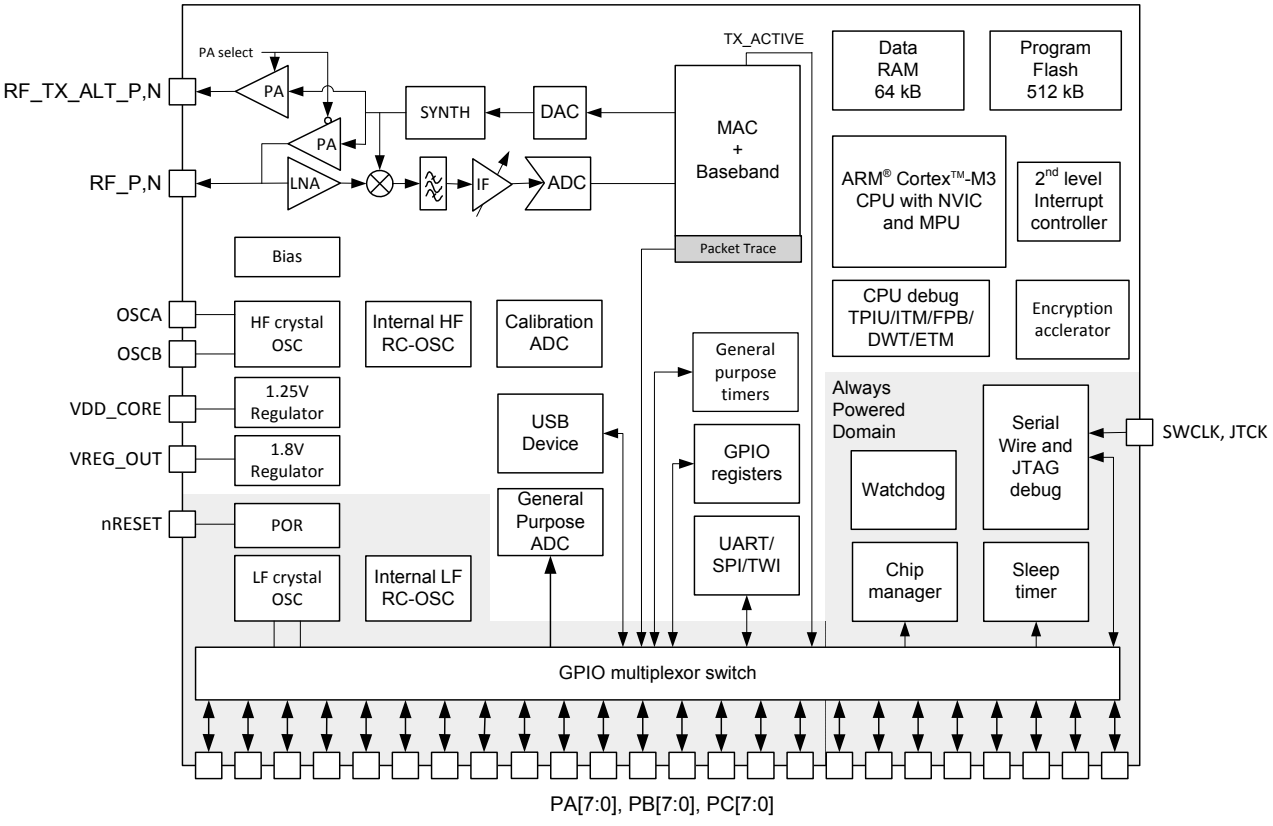
Industry-leading ARM® Cortex -M3 processor
- Leading 32-bit processing performance
- Highly efficient Thumb-2 instruction set
- Operation at 6, 12, or 24 MHz
- Flexible Nested Vectored Interrupt Controller

Low power consumption, advanced management
- RX Current (w/ CPU): 27 mA
- TX Current (w/ CPU, +3 dBm TX): 31 mA
- Low deep sleep current, with retained RAM and GPIO: 1.0 µA without/1.25 µA with sleep timer
- Low-frequency internal RC oscillator for low-power sleep timing
- High-frequency internal RC oscillator for fast (110 µs) processor start-up from sleep

Exceptional RF Performance
- Normal mode link budget up to 103 dB; configurable up to 110 dB
- –100 dBm normal RX sensitivity; configurable to –102 dBm (1% PER, 20 byte packet)
- +3 dB normal mode output power; configurable up to +8 dBm
- Robust Wi-Fi and Bluetooth coexistence

Innovative network and processor debug
- Packet Trace Port for non-intrusive packet trace with Ember development tools
- Serial Wire/JTAG interface
- Standard ARM debug capabilities: Flash Patch & Breakpoint; Data Watchpoint & Trace; Instrumentation Trace Macrocell

Application Flexibility
- Single voltage operation: 2.1–3.6 V with internal 1.8 and 1.25 V regulators
- Optional 32.768 kHz crystal for higher timer accuracy
- Low external component count with single 24 MHz crystal
- Support for external power amplifier
- Small 7x7 mm 48-pin QFN package



General Description

The Ember EM358x is a fully integrated System-on-Chip that integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM® Cortex™-M3 microprocessor, flash and RAM memory, and peripherals of use to designers of ZigBee-based systems.

The transceiver uses an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15 dB. The integrated receive channel filtering allows for robust co-existence with other communication standards in the 2.4 GHz spectrum, such as IEEE 802.11-2007 and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high performance radio mode (boost mode) is software-selectable to boost dynamic range.

The integrated 32-bit ARM® Cortex™-M3 microprocessor is highly optimized for high performance, low power consumption, and efficient memory utilization. Including an integrated MPU, it supports two different modes of operation—privileged mode and user mode. This architecture could allow for separation of the networking stack from the application code, and prevents unwanted modification of restricted areas of memory and registers resulting in increased stability and reliability of deployed solutions.

The EM358x has either 256 or 512 kB of embedded flash memory and either 32 or 64 kB of integrated RAM for data and program storage. The Ember software for the EM358x employs an effective wear-leveling algorithm that optimizes the lifetime of the embedded flash.

To maintain the strict timing requirements imposed by the ZigBee and IEEE 802.15.4-2003 standards, the EM358x integrates a number of MAC functions, AES128 encryption accelerator, and automatic CRC handling into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic backoff delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. The Ember Packet Trace Interface is also integrated with the MAC, allowing complete, non-intrusive capture of all packets to and from the EM358x with Ember development tools.

The EM358x offers a number of advanced power management features that enable long battery life. A high-frequency internal RC oscillator allows the processor core to begin code execution quickly upon waking. Various deep sleep modes are available with less than 2 µA power consumption while retaining RAM contents. To support user-defined applications, on-chip peripherals include optional USB, UART, SPI, TWI, ADC, and general-purpose timers, as well as up to 24 GPIOs. Additionally, an integrated voltage regulator, power-on-reset circuit, and sleep timer are available.

Finally, the EM358x utilizes standard Serial Wire and JTAG interfaces for powerful software debugging and programming of the ARM Cortex™-M3 core. The EM358x integrates the standard ARM® system debug components: Flash Patch and Breakpoint (FPB), Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (ITM) as well as the advanced Embedded Trace Macrocell (ETM).

Target applications for the EM358x include:

- Smart Energy
- Building automation and control
- Home automation and control
- Security and monitoring
- General ZigBee wireless sensor networking

This technical data sheet details the EM358x features available to customers using it with Ember software.

Table of Contents

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the Ember EM358x devices.

1.1.1. Ember EM358x Reference Manual

The Silicon Laboratories Ember EM358x Reference Manual provides the detailed description for each peripheral on the EM358x devices.

1.1.2. ZigBee Specification

The core ZigBee specification (Document 053474) defines ZigBee's smart, cost-effective and energy-efficient mesh network. It can be downloaded from the ZigBee website (www.zigbee.org). ZigBee Alliance membership is required.

1.1.3. ZigBee PRO Stack Profile

The ZigBee PRO Stack Profile specification (Document 074855) is optimized for low power consumption and to support large networks with thousands of devices. It can be downloaded from the ZigBee website (111.zigbee.org). ZigBee Alliance membership is required.

1.1.4. ZigBee Stack Profile

The ZigBee Stack Profile specification (Document 064321) is designed to support smaller networks with hundreds of devices in a single network. It can be downloaded from the ZigBee website (111.zigbee.org). ZigBee Alliance membership is required.

1.1.5. Bluetooth Core Specification

The Bluetooth specification is the global short-range wireless standard enabling connectivity for a broad range of electronic devices. Version 2.1 + EDR (Enhanced Data Rate) can be found here:

http://www.bluetooth.org/docman/handlers/downloaddoc.ashx?doc_id=241363

1.1.6. EEE 802.15.4-2003

This standard defines the protocol and compatible interconnection for data communication devices using low data rate, low power and low complexity, short-range radio frequency (RF) transmissions in a wireless personal area network (WPAN). It can be found here:

IEEE 802.15.4-2003 (http://standards.ieee.org/getieee802/download/802.15.4-2003.pdf)

1.1.7. EEE 802.11g

This version provides changes and additions to support the further higher data rate extension for operation in the 2.4 GHz band. It can be found here:

http://standards.ieee.org/getieee802/download/802.11g-2003.pdf

1.1.8. USB 2.0 Specification

The Universal Serial Bus Revision 2.0 specification provides the technical details to understand USB requirements and design USB compatible products. The main specification (usb_20.pdf) is part of the zipfile found here:

http://www.usb.org/developers/docs/usb_20_101111.zip

1.1.9. ARM® Cortex™-M3 Reference Manual

ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM® Cortex™-M3 reference documentation. The online reference manual can be found here:

http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm.m3/index.html#cortexm3

1.2. Conventions

Abbreviations and acronyms used in this data sheet are explained in

Table 1.1. Acronyms and Abbreviations

Acronym/Abbreviation	Meaning
ACK	Acknowledgement
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AHB	Advanced High Speed Bus
APB	Advanced Peripheral Bus
CBC-MAC	Cipher Block Chaining—Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter with CBC-MAC Mode for AES encryption
CCM*	Improved Counter with CBC-MAC Mode for AES encryption
CIB	Customer Information Block
CLK1K	1 kHz Clock
CLK32K	32.768 kHz Crystal Clock
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSMA-CA	Carrier Sense Multiple Access-Collision Avoidance
CTR	Counter Mode
CTS	Clear to Send
DNL	Differential Non-Linearity
DMA	Direct Memory Access
DWT	Data Watchpoint and Trace
EEPROM	Electrically Erasable Programmable Read Only Memory
EM	Event Manager
ENOB	effective number of bits
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
ETR	External Trigger Input
FCLK	ARM® Cortex™-M3 CPU Clock
FIB	Fixed Information Block
FIFO	First-in, First-out

Table 1.1. Acronyms and Abbreviations

FPB	Flash Patch and Breakpoint
GPIO	General Purpose I/O (pins)
HF	High Frequency
I^2C	Inter-Integrated Circuit
IDE	Integrated Development Environment
IF	Intermediate Frequency
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Non-linearity
ITM	Instrumentation Trace Macrocell
JTAG	Joint Test Action Group
LF	Low Frequency
LNA	Low Noise Amplifier
LQI	Link Quality Indicator
LSB	Least significant bit
MAC	Medium Access Control
MFB	Main Flash Block
MISO	Master in, slave out
MOS	Metal Oxide Semiconductor (P-channel or N-channel)
MOSI	Master out, slave in
MPU	Memory Protection Unit
MSB	Most significant bit
MSL	Moisture Sensitivity Level
NACK	Negative Acknowledge
NIST	National Institute of Standards and Technology
NMI	Non-Maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
OPM	One-Pulse Mode
O-QPSK	Offset-Quadrature Phase Shift Keying
OSC24M	High Frequency Crystal Oscillator
OSC32K	Low-Frequency 32.768 kHz Oscillator
OSCHF	High-Frequency Internal RC Oscillator
OSCRC	Low-Frequency RC Oscillator
PA	Power Amplifier

Table 1.1. Acronyms and Abbreviations

PCLK	Peripheral clock
PER	Packet Error Rate
PHY	Physical Layer
PLL	Phase-Locked Loop
POR	Power-On-Reset
PRNG	Pseudo Random Number Generator
PSD	Power Spectral Density
PTI	Packet Trace Interface
PWM	Pulse Width Modulation
QFN	Quad Flat Pack
RAM	Random Access Memory
RC	Resistive/Capacitive
RF	Radio Frequency
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances
RSSI	Receive Signal Strength Indicator
RTS	Request to Send
Rx	Receive
SYSCLK	System clock
SDFR	Spurious Free Dynamic Range
SFD	Start Frame Delimiter
SINAD	Signal-to-noise and distortion ratio
SPI	Serial Peripheral Interface
SWJ	Serial Wire and JTAG Interface
THD	Total Harmonic Distortion
TRNG	True random number generator
TWI	Two Wire serial interface
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UEV	Update event
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator

2. Typical Connection Diagrams

Figure 2.1 illustrates the typical application circuit.

Note: The circuit shown in Figure 2.1 is for example purposes only. For a complete reference design, please download one of the latest Ember Hardware Reference Designs from the Silicon Labs website (www.silabs.com/zigbee-support).

The Balun provides an impedance transformation from the antenna to the EM358x for both TX and RX modes.

L4, along with the PCB trace parasitics and the ceramic balun impedence, provide the optimal RF path for maximum transmit power and receive sensitivity for the EM358x system.

The harmonic filter (L5, L6, C7, C8 and C9) provides additional suppression of the second harmonic, which increases the margin over the FCC limit.

The 24 MHz crystal, Y2, with loading capacitors is required and provides the high-frequency crystal oscillator source for the EM358x's main system clock. The optional 32.768 kHz crystal, Y1, with loading capacitors generates a highly accurate low-frequency crystal oscillator for use with peripherals, but it is not mandatory as the low-frequency internal RC oscillator can be used.

Loading capacitance and ESR (C3 and R3) provides proper loading for the internal 1.8 V regulator.

Loading capacitance C4 provides proper loading for the internal 1.25 V regulator, no ESR is required because it is contained within the chip.

Resistor R7 reduces the operating voltage of the flash memory. This reduces current consumption and improves sensitivity by 1 dB when compared to not using it.

Various decoupling capacitors, C12 – C21, are required, these should be placed as close to their corresponding pins as possible. For values and locations see one of the Silicon Labs reference designs.

An antenna impedance matched to 50 Ω is required.

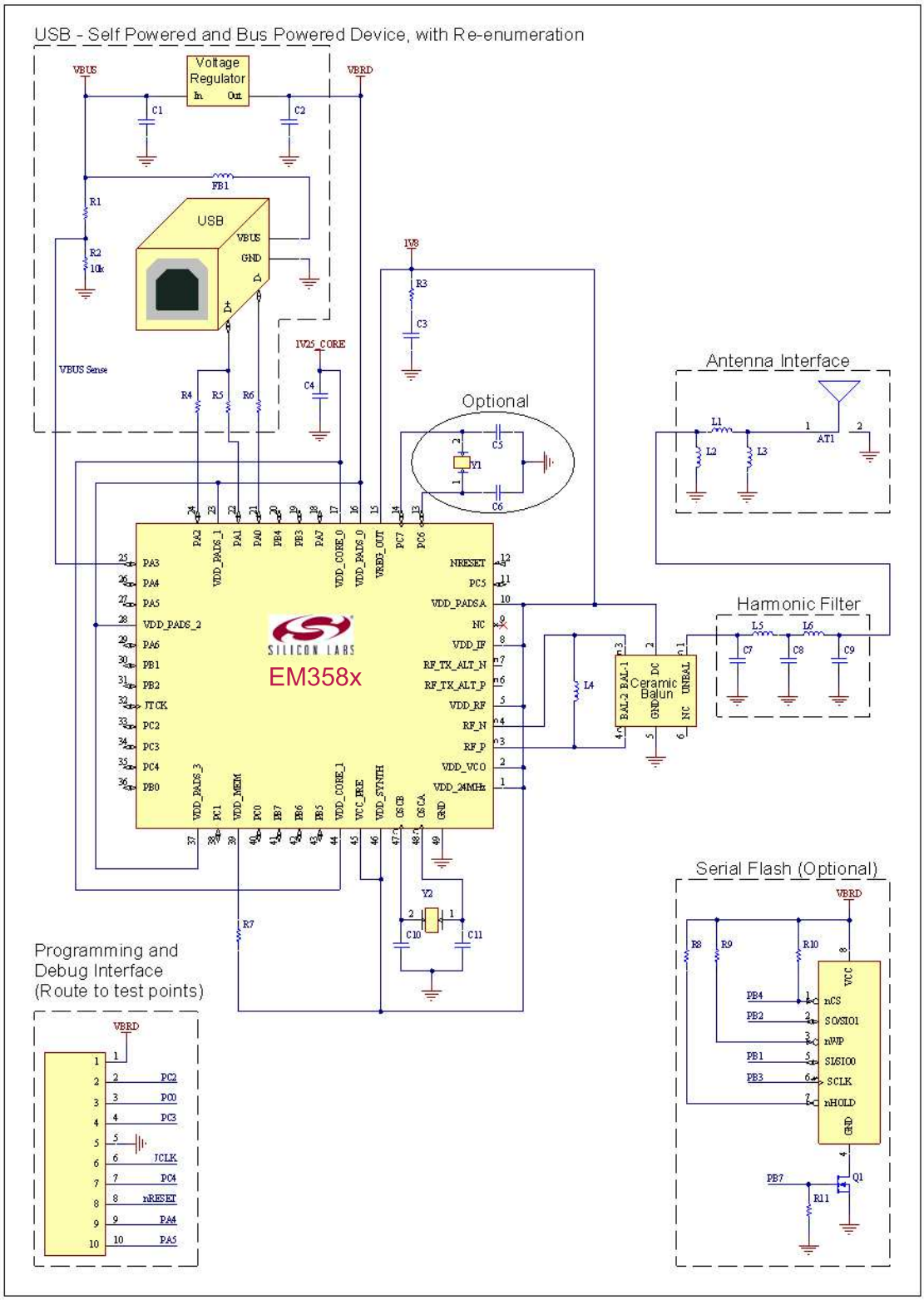


Figure 2.1. Typical Application Circuit

Table 2.1. Bill of Materials for Figure 2.1

Item	Qty	Reference	Description	Manufacturer
1	1	ANT1	ANTENNA, <not specified>	<not specified>
2	1	BLN1	BALUN, CHIP MULTILAYER CERAMIC, 2.4 GHZ. 50/100 OHM, -40C TO 85C, 0805	Wurth 748421245 Johanson 2450BL15B100E Murata LDB212G4010C-001 TDK HHM1520
3	1	C1	CAPACITOR, <not specified>	<not specified>
4	1	C2	CAPACITOR, <not specified>	<not specified>
5	1	C3	CAPACITOR, 2.2 µF, 10 V, X5R, 10%, 0603	<not specified>
6	1	C4	CAPACITOR, 1 µF, 6.3 V, X5R, 10%, 0402	<not specified>
7	1	C5	CAPACITOR, 33 pF, ±5%, 50 V, NPO, 0402	<not specified>
8	3	C6, C10, C11	CAPACITOR, 22 pF, ±5%, 50 V, NPO, 0402	<not specified>
9	2	C7, C9	CAPACITOR, 1 pF, ±0.25 pF, 50 V, 0402, NPO	<not specified>
10	1	C8	CAPACITOR, 1.8pF, ±0.25 pF, 50 V, 0402, NPO	<not specified>
11	1	FB1	FERRITE BEAD, 60 OHM, 500MA, 0603	Murata BLM18PG600SN1
12	1	J1	CONNECTOR, USB, END LAUNCH, THROUGH HOLE	Molex 67068-8110
13	1	J2	CONNECTOR, HEADER, SHROUDED, 10 POSITION, DUAL ROW, VERTICAL, 0.050"	Samtec FTSH-105-01-L-DV-K
14	4	L1, L2, L3, L4	INDUCTOR, <not specified>	<not specified>
15	2	L5, L6	INDUCTOR, 2.7 nH, ±0.3 nH, 0402, MULTI-LAYER	Murata LQG15HS2N7
16	1	R1	RESISTOR, 15K OHM, 5%, 1/10W, 0402	<not specified>
17	1	R2	RESISTOR, 10K OHM, 5%, 1/16W, 0402	<not specified>
18	1	R3	RESISTOR, 1 OHM, 5%, 1/16W, 0402	<not specified>
19	1	R4	RESISTOR, 1.5K OHM, 1%, 1/16W, 0402	<not specified>
20	2	R5, R6	RESISTOR, 26.1 OHM, 1%, 1/10W, 0402	<not specified>
21	1	R7	RESISTOR, 10 OHM, 5%, 1/16W, 0402	<not specified>
22	4	R8, R9, R10, R11	RESISTOR, 100K OHM, 5%, 1/16W, 0402	<not specified>
23	1	Q1	MOSFET, 2N7002, 300MA, 830MW, 60V, TO-236-3, SC-59, SOT-23-3	NXP Semiconductor 2N7002
24	1	U1	IC, VOLTAGE REGULATOR, <not specified>	<not specified>
25	1	U2	EM358x, ZIGBEE/802.15.4 RF TRANSCEIVER, ARM CORTEX-M3, 32 or 64 kB RAM, 256 or 512 kB FLASH, 48-QFN	EM3581-RTR/EM3582-RTR/ EM3585-RTR/ EM3586-RTR/EM3587-RTR/ EM3588-RTR

Table 2.1. Bill of Materials for Figure 2.1

26	1	U3	IC - PROGRAMMABLE MEMORY - BLANK, SERIAL FLASH, 8M (256K X 32), 2.7 V - 3.6 V, -40 to 85 ºC, 8-SOIC (0.154", 3.90MM WIDTH)	WinBond W25Q80BVSNIG
27	1	Y1	CRYSTAL, 32.768 kHz, ±20 ppm INITIAL TOLERANCE AT +25ºC, 12.5 pF	Abracon ABS07-32.768KHZ-T
28	1	Y2	OSCILLATOR, CRYSTAL, 24.000 MHz, 18 pF LOAD, ±10 PPM TOLERANCE, ±25 PPM STABILITY, -40 TO 85 ºC, AT49	Abracon ABLS-24.000MHZ-D1X-T ILSI HC49USM-24.000000M-2435 AEL X24M000000S067

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Table 3.1 lists the absolute maximum ratings for the EM358x.

Table 3.1. Absolute Maximum Ratings

Parameter	Test Condition	Min	Max	Unit
Regulator input voltage (VDD_PADS)		–0.3	+3.6	V
Analog, Memory and Core voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_MEM, VDD_PRE, VDD_SYNTH, VDD_CORE)		–0.3	+2.0	V
Voltage on RF_P,N; RF_TX_ALT_P,N		–0.3	+3.6	V
RF Input Power (for max level for correct packet reception see Table 3.7)	RX signal into a loss-less balun	—	+15	dBm
Voltage on any GPIO (PA[7:0], PB[7:0], PC[7:0]), SWCLK, nRESET, VREG_OUT		–0.3	VDD_PADS +0.3	V
Voltage on any GPIO pin (PA4, PA5, PB5, PB6, PB7, PC1), when used as an input to the general purpose ADC		–0.3	2.0	V
Voltage on OSCA, OSCB, NC		–0.3	VDD_PADSA +0.3	V
Storage temperature		–40	+140	°C

3.2. Recommended Operating Conditions

Table 3.2 lists the rated operating conditions of the EM358x.

Table 3.2. Operating Conditions

Parameter	Test Condition	Min	Typ	Max	Unit
Regulator input voltage (VDD_PADS)		2.1	—	3.6	V
Analog and memory input voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_MEM, VDD_PRE, VDD_SYNTH)		1.7	1.8	1.9	V
Core input voltage when supplied from internal regulator (VDD_CORE)		1.18	1.25	1.32	V
Operating temperature range		–40	—	+85	°C

3.3. Environmental Characteristics

Table 3.3 lists the rated environmental characteristics of the EM358x.

Table 3.3. Environmental Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
ESD (human body model)	On any pin	—	—	±2	kV
ESD (charged device model)	Non-RF pins	—	—	±400	V
ESD (charged device model)	RF pins	—	—	±225	V

3.4. DC Electrical Characteristics

Table 3.4 lists the DC electrical characteristics of the EM358x.

Table 3.4. DC Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Regulator input voltage (VDD_PADS)		2.1	—	3.6	V
Power supply range (VDD_MEM)	Regulator output or external input	1.7	1.8	1.9	V
Power supply range (VDD_CORE)	Regulator output	1.18	1.25	1.32	V
Deep Sleep Current					
Quiescent current, internal oscillator disabled, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	0.9	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.0	—	µA
	+85 °C, VDD_PADS=3.6 V	—	2.2	—	µA
Quiescent current, including internal RC oscillator, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	1.2	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.25	—	µA
	+85°C, VDD_PADS=3.6 V	—	2.5	—	µA
Quiescent current, including 32.768 kHz oscillator, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	1.3	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.6	—	µA
	+85 °C, VDD_PADS=3.6 V	—	2.9	—	µA
Quiescent current, including internal RC oscillator and 32.768 kHz oscillator, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	1.6	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.9	—	µA
	+85 °C, VDD_PADS=3.6 V	—	3.2	—	µA
Additional quiescent current per 4 kB block of RAM retained	–40 °C, VDD_PADS=3.6 V	—	0.007	—	µA
	+25 °C, VDD_PADS=3.6 V	—	0.067	—	µA
	+85 °C, VDD_PADS=3.6 V	—	0.76	—	µA
Additional quiescent current when retained RAM exceeds 32 kB	–40 °C, VDD_PADS=3.6 V	—	0.57	—	µA
	+25 °C, VDD_PADS=3.6 V	—	0.67	—	µA
	+85 °C, VDD_PADS=3.6 V	—	2.0	—	µA
Simulated deep sleep (debug mode) current	With no debugger activity	—	500	—	µA

Table 3.4. DC Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
Reset Current					
Quiescent current, nRESET asserted	Typ at 25 °C/3.0 V Max at 85 °C/3.6 V	—	2	3	mA
Processor and Peripheral Currents					
ARM® Cortex™-M3, RAM, and flash memory	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 running at 12 MHz from crystal oscillator Radio and all peripherals off	—	7.5	—	mA
ARM® Cortex™-M3, RAM, and flash memory	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 running at 24 MHz from crystal oscillator Radio and all peripherals off	—	8.5	—	mA
ARM® Cortex™-M3, RAM, and flash memory sleep current	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz from the crystal oscillator Radio and all peripherals off	—	4.0	—	mA
ARM® Cortex™-M3, RAM, and flash memory sleep current	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 6 MHz from the high frequency RC oscillator Radio and all peripherals off	—	2.5	—	mA
Serial controller current	For each controller at maximum data rate	—	0.2	—	mA
General purpose timer current	For each timer at maximum clock rate	—	0.25	—	mA
General purpose ADC current	At maximum sample rate, DMA enabled	—	1.1	—	mA
USB active current			1		mA
USB suspended mode current	1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 3 MHz from the high frequency RC oscillator. Radio and all peripherals off			2.5	mA
RX Current					
Radio receiver, MAC, and baseband	ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz	—	23.5	—	mA
Total RX current (= I_{Radio} receiver, MAC and baseband, CPU + IRAM, and Flash memory)	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 12 MHz	—	27.0	—	mA
	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 24 MHz	—	28.0	—	mA

Table 3.4. DC Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
Boost mode total RX current (= I_{Radio} receiver, MAC and baseband, CPU+ IRAM, and flash memory)	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 12 MHz	—	29.0	—	mA
	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 24 MHz	—	30.0	—	mA
TX Current					
Radio transmitter, MAC, and baseband	25 °C and 1.8 V core; max. power out (+3 dBm typical) ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz	—	27.5	—	mA
Total TX current (= I_{Radio} transmitter, MAC and baseband, CPU + IRAM, and flash memory)	25 °C, VDD_PADS=3.0 V; maximum power setting (+8 dBm); ARM® Cortex™-M3 running at 12 MHz	—	44	—	mA
	25 °C, VDD_PADS=3.0 V; +3 dBm power setting; ARM® Cortex™-M3 running at 12 MHz	—	31.5	—	mA
	25 °C, VDD_PADS=3.0 V; 0 dBm power setting; ARM® Cortex™-M3 running at 12 MHz	—	29	—	mA
	25 °C, VDD_PADS=3.0 V; minimum power setting; ARM® Cortex™-M3 running at 12 MHz	—	24	—	mA
	25 °C, VDD_PADS=3.0 V; maximum power setting (+8 dBm); ARM® Cortex™-M3 running at 24 MHz	—	45	—	mA
	25 °C, VDD_PADS=3.0 V; +3 dBm power setting; ARM® Cortex™-M3 running at 24 MHz	—	33.5	—	mA
	25 °C, VDD_PADS=3.0 V; 0 dBm power setting; ARM® Cortex™-M3 running at 24 MHz	—	30	—	mA
	25 °C, VDD_PADS=3.0 V; minimum power setting; ARM® Cortex™-M3 running at 24 MHz	—	24	—	mA

Figure 3.1 shows the variation of current in transmit mode (with the ARM® Cortex™-M3 running at 12 MHz).

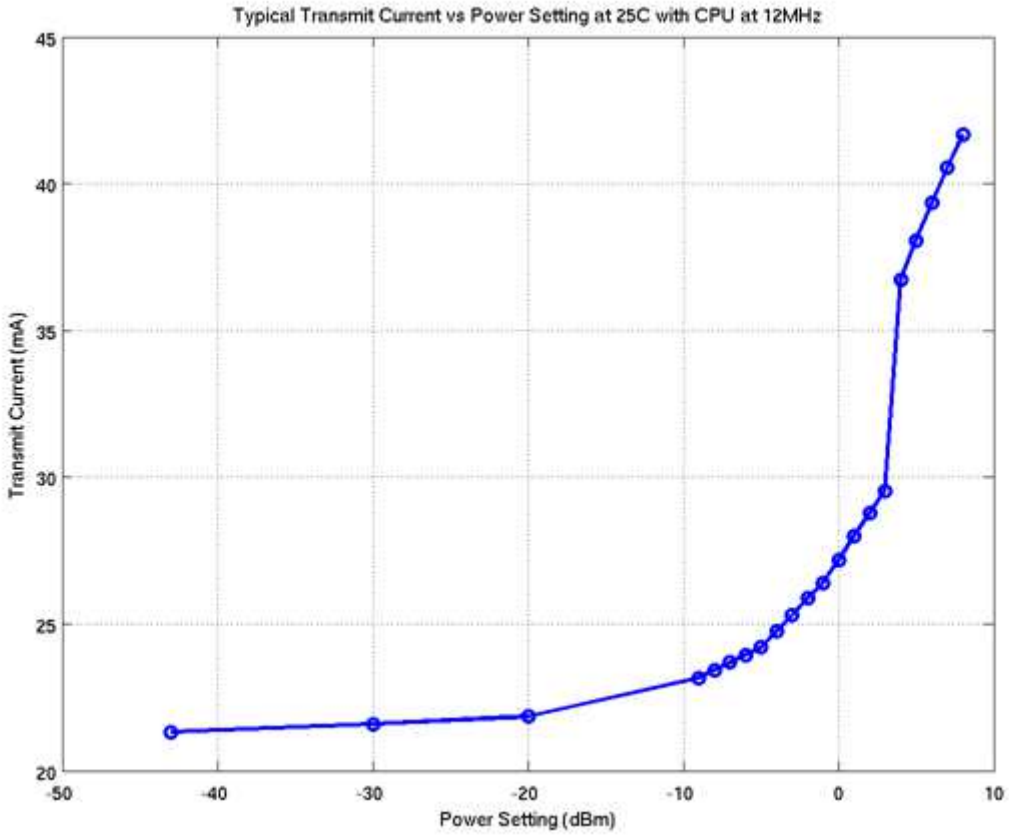


Figure 3.1. Transmit Power Consumption

Figure 3.2 shows typical output power against power setting on the Silicon Labs reference design.

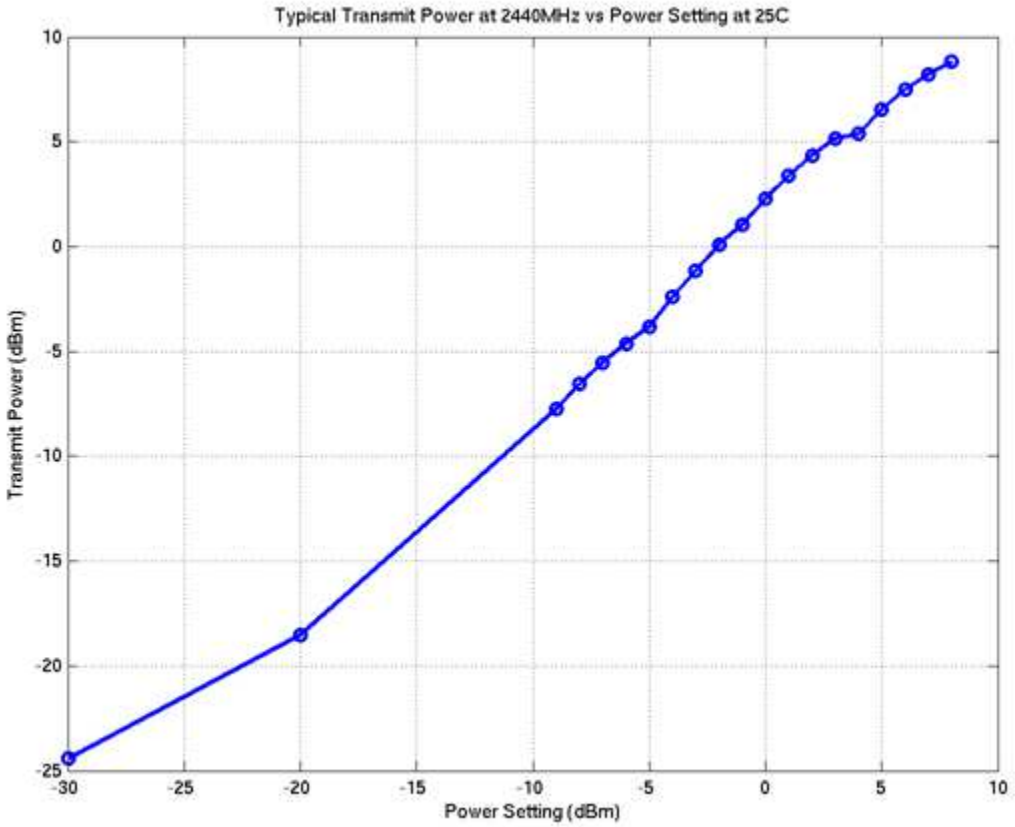


Figure 3.2. Transmit Output Power

3.5. Digital I/O Specifications

Table 3.5 lists the digital I/O specifications for the EM358x. The digital I/O power (named VDD_PADS) comes from three dedicated pins (Pins 23, 28, and 37). The voltage applied to these pins sets the I/O voltage.

Table 3.5. Digital I/O Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Voltage supply (regulator input voltage)		2.1	—	3.6	V
Low Schmitt switching threshold	V_{SWIL} Schmitt input threshold going from high to low	0.42 x VDD_PADS	—	0.50 x VDD_PADS	V
High Schmitt switching threshold	V_{SWIH} Schmitt input threshold going from low to high	0.62 x VDD_PADS	—	0.80 x VDD_PADS	V
Input current for logic 0	I_{IL}	—	—	–0.5	µA
Input current for logic 1	I_{IH}	—	—	+0.5	µA
Input pull-up resistor value	R_{IPU}	24	29	34	kΩ
Input pull-down resistor value	R_{IPD}	24	29	34	kΩ
Output voltage for logic 0	V_{OL} (I_{OL} = 4 mA for standard pads, 8 mA for high current pads)	0	—	0.18 x VDD_PADS	V
Output voltage for logic 1	V_{OH} (I_{OH} = 4 mA for standard pads, 8 mA for high current pads)	0.82 x VDD_PADS	—	VDD_PADS	V
Output source current (standard current pad)	I_{OHS}	—	—	4	mA
Output sink current (standard current pad)	I_{OLS}	—	—	4	mA
Output source current high current pad: PA6, PA7, PB6, PB7, PC0	I_{OHH}	—	—	8	mA
Output sink current high current pad: PA6, PA7, PB6, PB7, PC0	I_{OLH}	—	—	8	mA
Total output current (for I/O Pads)	$I_{OH} + I_{OL}$	—	—	40	mA

Table 3.6 lists the nRESET pin specifications for the EM358x. The digital I/O power (named VDD_PADS) comes from three dedicated pins (Pins 23, 28, and 37). The voltage applied to these pins sets the I/O voltage.

Table 3.6. nReset Pin Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Low Schmitt switching threshold	V_{SWIL} Schmitt input threshold going from high to low	0.42 x VDD_PADS	—	0.50 x VDD_PADS	V
High Schmitt switching threshold	V_{SWIH} Schmitt input threshold going from low to high	0.62 x VDD_PADS	—	0.80 x VDD_PADS	V
Input current for logic 0	I_{IL}	—	—	–0.5	µA
Input current for logic 1	I_{IH}	—	—	+0.5	µA
Input pull-up resistor value	R_{IPU} Pull-up value while the chip is not reset	24	29	34	kΩ
Input pull-up resistor value	$R_{IPURESET}$ Pull-up value while the chip is reset	12	14.5	17	kΩ

3.6. Non-RF System Electrical Characteristics

Table 3.7 lists the non-RF system level characteristics for the EM358x.

Table 3.7. Non-RF System Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
System wake time from deep sleep	From wakeup event to first ARM® Cortex™-M3 instruction running from 6 MHz internal RC clock Includes supply ramp time and oscillator startup time	—	110	—	µs
Shutdown time going into deep sleep	From last ARM® Cortex™-M3 instruction to deep sleep mode	—	5	—	µs

3.7. RF Electrical Characteristics

3.7.1. Receive

Table 3.8 lists the key parameters of the integrated IEEE 802.15.4-2003 receiver on the EM358x.

Receive measurements were collected with the Silicon Labs EM358x Ceramic Balun Reference Design (Version A0) at 2440 MHz. The typical number indicates one standard deviation above the mean, measured at room temperature (25 °C). The Min and Max numbers were measured over process corners at room temperature.

Table 3.8. Receive Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	—	2500	MHz
Sensitivity (boost mode)	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	—	–102	–96	dBm
Sensitivity	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	—	–100	–94	dBm
High-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	35	—	dB
Low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	35	—	dB
2nd high-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	46	—	dB
2nd low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	46	—	dB
High-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	39	—	dB
Low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	47	—	dB
2nd high-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	49	—	dB
2nd low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	49	—	dB
High-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	44	—	dB
Low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	47	—	dB

Table 3.8. Receive Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
2nd high-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	59	—	dB
2nd low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	59	—	dB
Channel rejection for all other channels	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	40	—	dB
802.11g rejection centered at +12 MHz or –13 MHz	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	36	—	dB
Maximum input signal level for correct operation		0	—	—	dBm
Co-channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	–6	—	dBc
Relative frequency error tolerance (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		–120	—	+120	ppm
Relative timing error tolerance (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		–120	—	+120	ppm
Linear RSSI range	As defined by IEEE 802.15.4-2003	40	—	—	dB
RSSI Range		–90	—	–40	dBm

Figure 3.3 shows the variation of receive sensitivity with temperature for boost mode and normal mode for a typical chip.

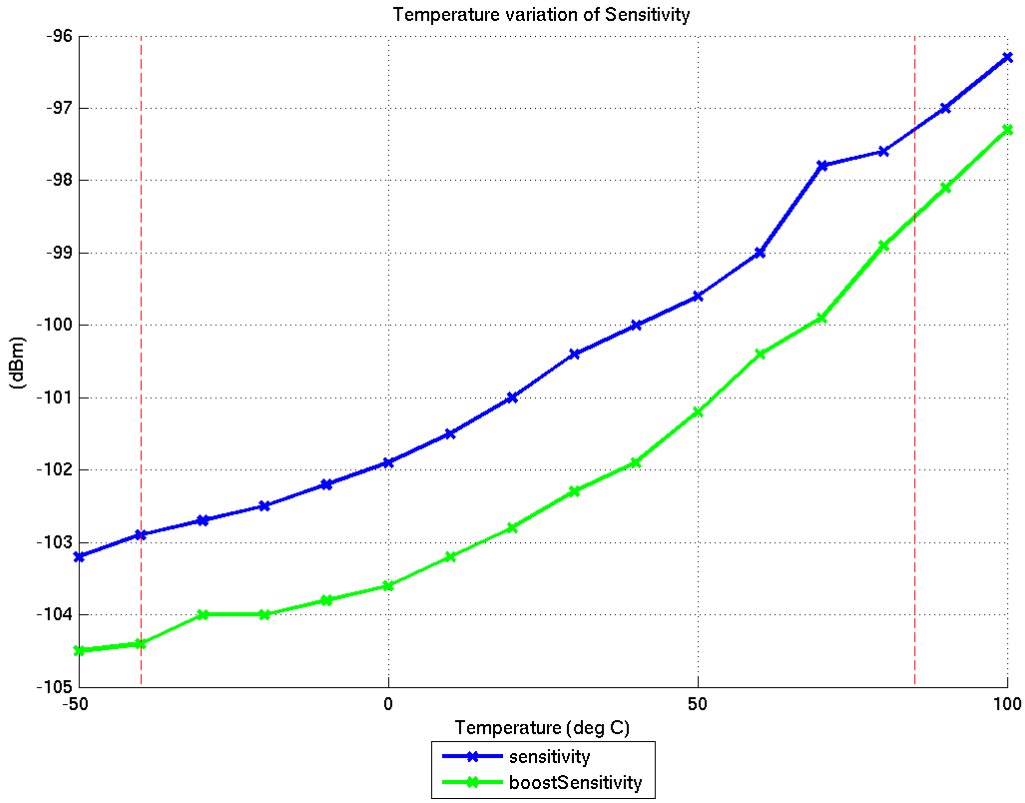


Figure 3.3. Receive Sensitivity vs. Temperature

3.7.2. Transmit

Table 3.9 lists the key parameters of the integrated IEEE 802.15.4-2003 transmitter on the EM358x.

Transmit measurements were collected with the Silicon Labs EM358x Ceramic Balun Reference Design (Version A0) at 2440 MHz. The Typical number indicates one standard deviation below the mean, measured at room temperature (25 °C). The Min and Max numbers were measured over process corners at room temperature. In terms of impedance, this reference design presents a 3n3 inductor in parallel with a 100:50 Ω balun to the RF pins.

Table 3.9. Transmit Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power (boost mode)	At highest boost mode power setting (+8)	—	8	—	dBm
Maximum output power	At highest normal mode power setting (+3)	1	5	—	dBm
Minimum output power	At lowest power setting	—	–55	—	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	—	5	15	%
Carrier frequency error		–40	—	+40	ppm
PSD mask relative	3.5 MHz away	–20	—	—	dB
PSD mask absolute	3.5 MHz away	–30	—	—	dBm

Figure 3.4 shows the variation of transmit power with temperature for maximum boost mode power, and normal mode for a typical chip.

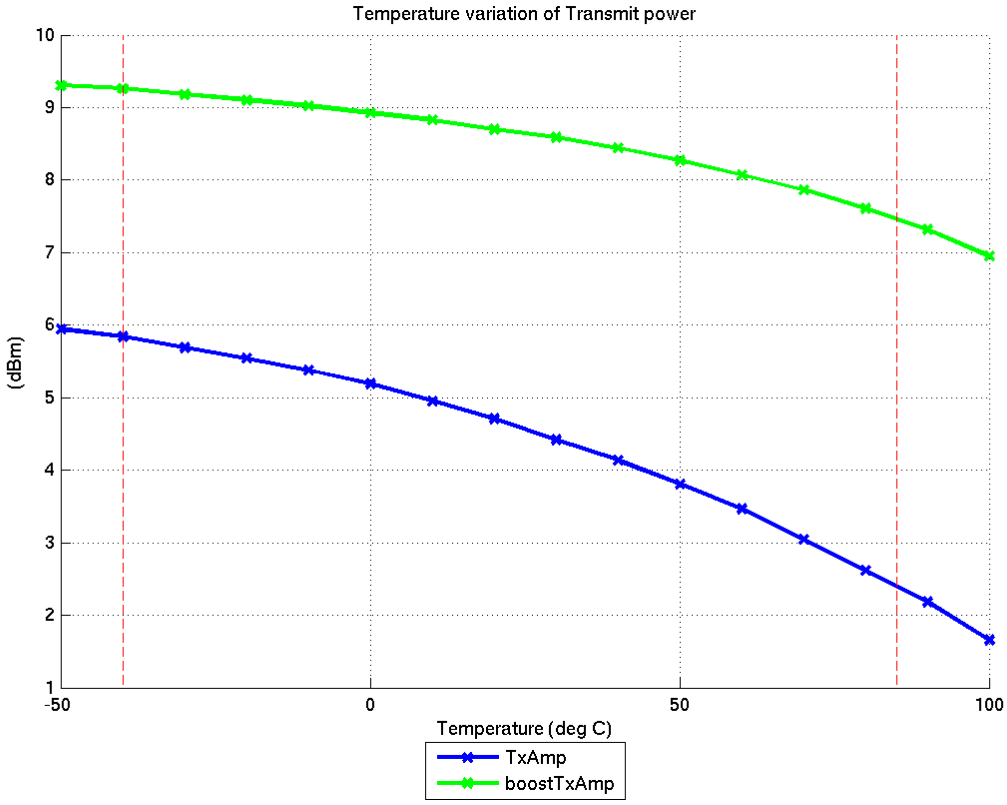


Figure 3.4. Transmit Power vs. Temperature