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# 2.5V Drive Nch+Pch MOSFET

## EM6M1

### ●Structure

Silicon N-channel MOSFET /  
Silicon P-channel MOSFET

### ●Features

- 1) Nch MOSFET and Pch MOSFET are put in EMT6 package.
- 2) High-speed switching.
- 3) Low voltage drive (2.5V drive).
- 4) Built-in G-S Protection Diode.

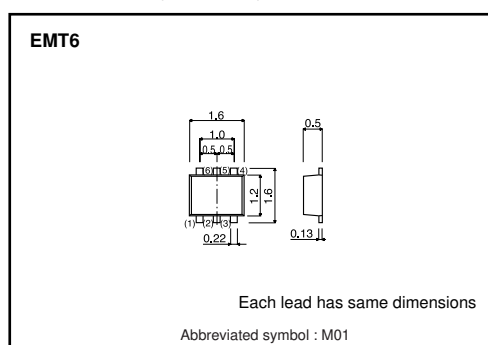
### ●Applications

Switching

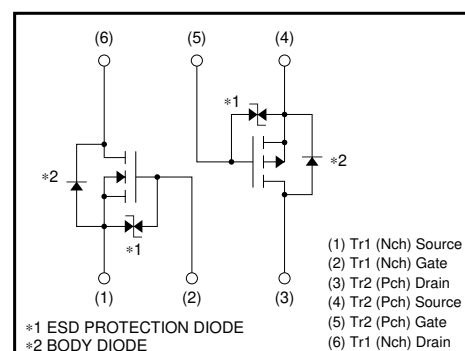
### ●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6M1		○

### ●Dimensions (Unit : mm)



### ●Inner circuit



### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	$V_{DSS}$	30	-20	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	$\pm 12$	V
Drain current	Continuous	$I_D$	$\pm 0.1$	A
	Pulsed	$I_{DP}^{*1}$	$\pm 0.4$	A
Power dissipation	$P_D^{*2}$	150		mW / TOTAL
		120		mW / ELEMENT
Channel temperature	$T_{ch}$	150		°C
Range of storage temperature	$T_{stg}$	-55 to +150		°C

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$

\*2 Mounted on a ceramic board

### ●Notice

This product might cause chip aging and breakdown under the large electrified environment.  
Please consider to design ESD protection circuit.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±1	μA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	30	–	–	V	I <sub>D</sub> =10μA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	1	μA	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	0.8	–	1.5	V	V <sub>DS</sub> =3V, I <sub>D</sub> =100μA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	5	8	Ω	I <sub>D</sub> =10mA, V <sub>GS</sub> =4V
		–	7	13	Ω	I <sub>D</sub> =1mA, V <sub>GS</sub> =2.5V
Forward transfer admittance	Y <sub>fs</sub>  *	20	–	–	mS	V <sub>DS</sub> =3V, I <sub>D</sub> =10mA
Input capacitance	C <sub>iss</sub>	–	13	–	pF	V <sub>DS</sub> =5V
Output capacitance	C <sub>oss</sub>	–	9	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	4	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	15	–	ns	V <sub>DD</sub> ≐5V
Rise time	t <sub>r</sub> *	–	35	–	ns	I <sub>D</sub> =10mA
Turn-off delay time	t <sub>d(off)</sub> *	–	80	–	ns	V <sub>GS</sub> =5V
Fall time	t <sub>f</sub> *	–	80	–	ns	R <sub>L</sub> =500Ω
Total gate charge	Q <sub>g</sub> *	–	0.9	–	nC	V <sub>DD</sub> ≐15V, I <sub>D</sub> =0.1A
Gate-source charge	Q <sub>gs</sub> *	–	0.2	–	nC	V <sub>GS</sub> =4.5V
Gate-drain charge	Q <sub>gd</sub> *	–	0.2	–	nC	R <sub>L</sub> =150Ω, R <sub>G</sub> =10Ω

\*Pulsed

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> = ±12V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–20	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –20V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–0.7	–	–2.0	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	1.0	1.5	Ω	I <sub>D</sub> = –0.2A, V <sub>GS</sub> = –4.5V
		–	1.1	1.6	Ω	I <sub>D</sub> = –0.2A, V <sub>GS</sub> = –4V
		–	2.0	3.0	Ω	I <sub>D</sub> = –0.2A, V <sub>GS</sub> = –2.5V
Forward transfer admittance	Y <sub>fs</sub>  *	0.2	–	–	S	V <sub>DS</sub> = –10V, I <sub>D</sub> = –0.15A
Input capacitance	C <sub>iss</sub>	–	50	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	5	–	pF	V <sub>GS</sub> = 0V
Reverse transfer capacitance	C <sub>rss</sub>	–	5	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	9	–	ns	V <sub>DD</sub> ≐ –15V
Rise time	t <sub>r</sub> *	–	6	–	ns	I <sub>D</sub> = –0.15A
Turn-off delay time	t <sub>d(off)</sub> *	–	35	–	ns	V <sub>GS</sub> = –4.5V
Fall time	t <sub>f</sub> *	–	45	–	ns	R <sub>L</sub> = 100Ω
Total gate charge	Q <sub>g</sub> *	–	1.2	–	nC	V <sub>DD</sub> ≐ –15V, I <sub>D</sub> = –0.2A
Gate-source charge	Q <sub>gs</sub> *	–	0.2	–	nC	V <sub>GS</sub> = –4.5V
Gate-drain charge	Q <sub>gd</sub> *	–	0.2	–	nC	R <sub>L</sub> = 75Ω, R <sub>G</sub> = 10Ω

\*Pulsed

Transistors

N-ch

●Electrical characteristic curve

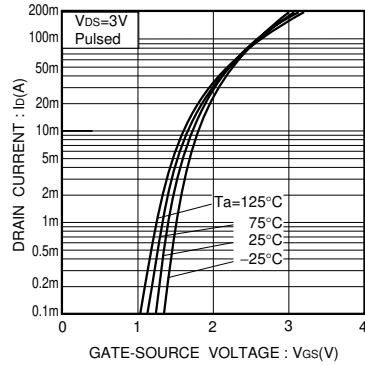


Fig.1 Typical Transfer Characteristics

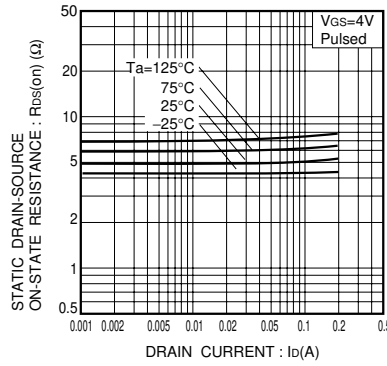


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current ( I )

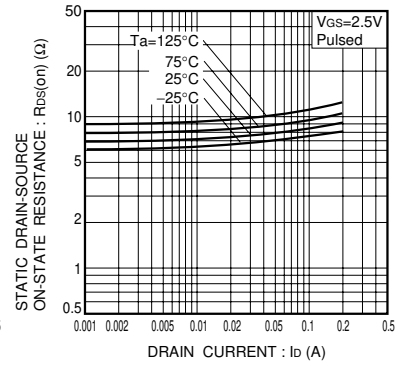


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current ( II )

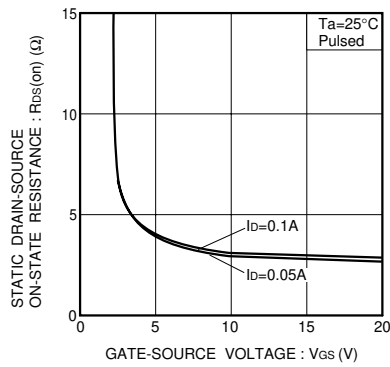


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

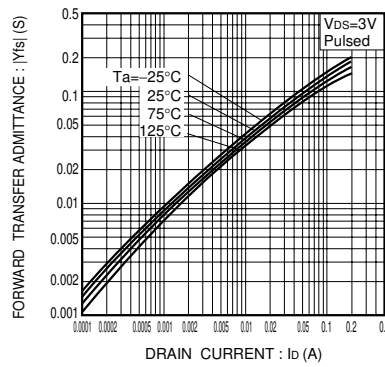


Fig.5 Forward Transfer Admittance vs. Drain Current

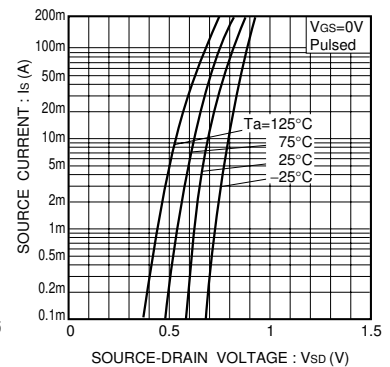


Fig.6 Reverse Drain Current vs. Source-Drain Voltage ( I )

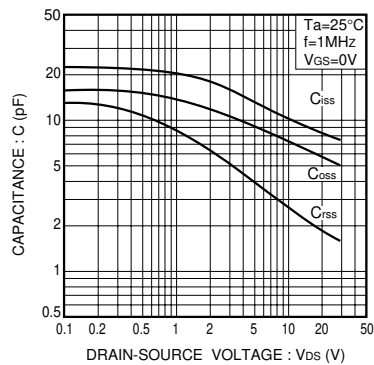


Fig.7 Typical Capacitance vs. Drain-Source Voltage

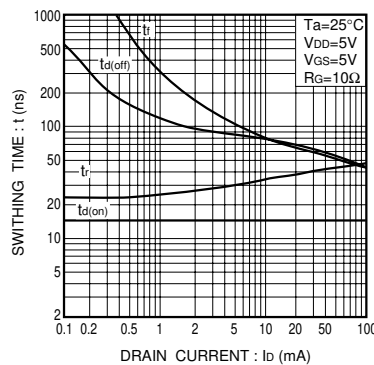


Fig.8 Switching Characteristics

Transistors

P-ch

●Electrical characteristic curve

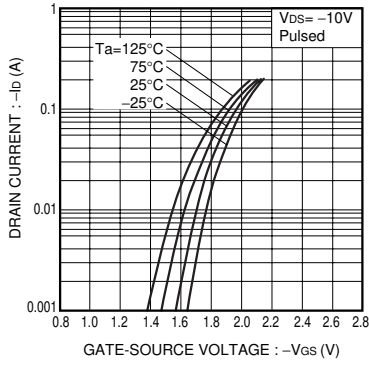


Fig.1 Typical Transfer Characteristics

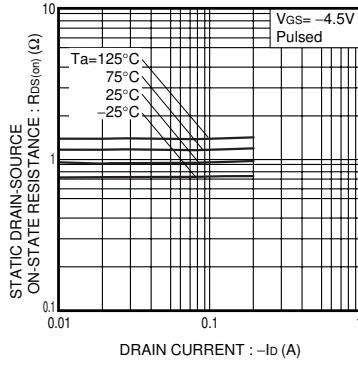


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current ( I )

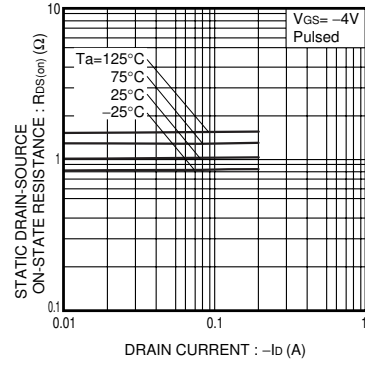


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current ( II )

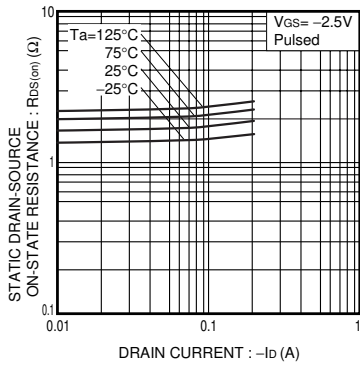


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current ( III )

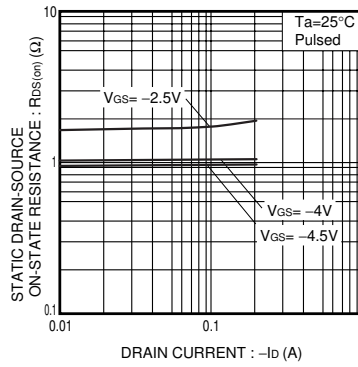


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current ( IV )

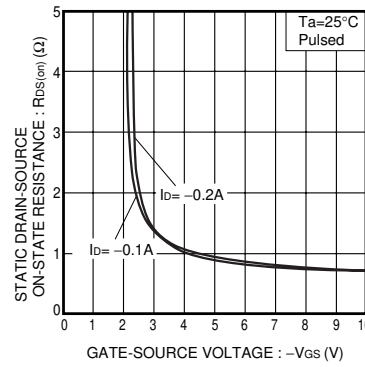


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

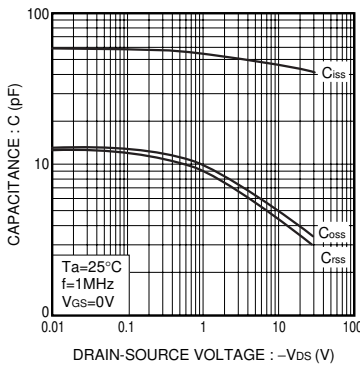


Fig.7 Typical Capacitance vs. Drain-Source Voltage

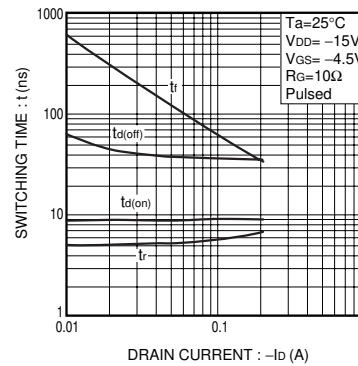


Fig.8 Switching Characteristics

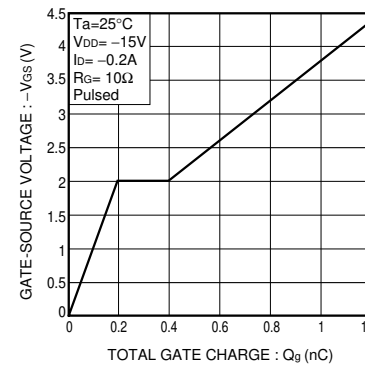


Fig.9 Dynamic Input Characteristics

Transistors

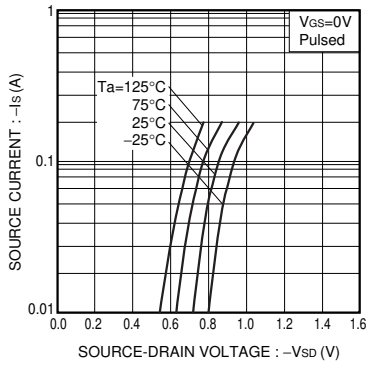


Fig.10 Source Current vs. Source-Drain Voltage

N-ch

●Measurement circuit

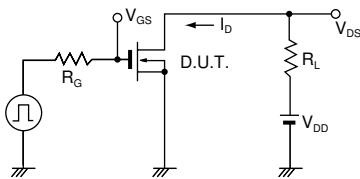


Fig.9 Switching Time Test Circuit

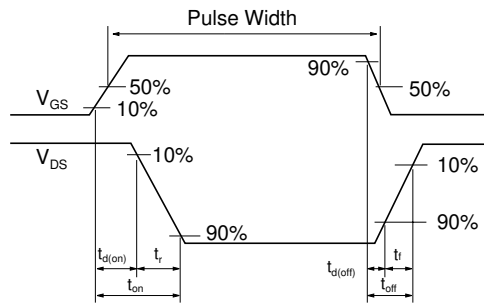


Fig.10 Switching Time Waveforms

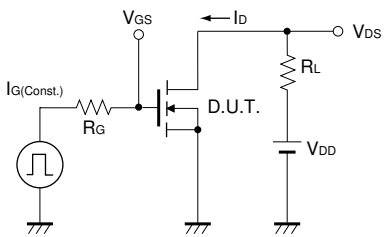


Fig.11 Gate Charge Measurement Circuit

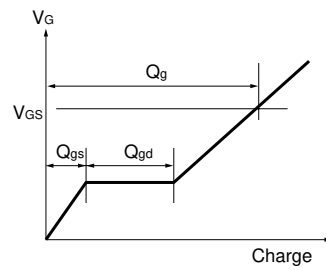


Fig.12 Gate Charge Waveform

Transistors

P-ch

●Measurement circuit

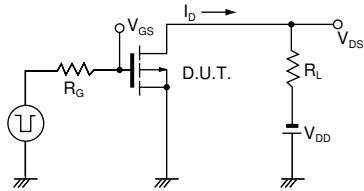


Fig.11 Switching Time Test Circuit

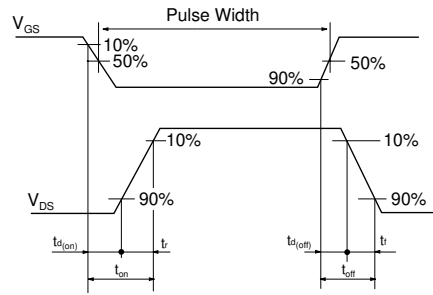


Fig.12 Switching Time Waveforms

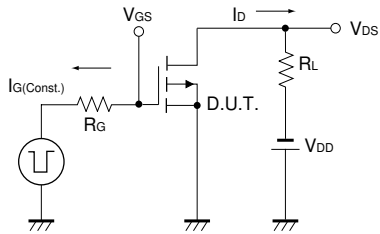


Fig.13 Gate Charge Measurement Circuit

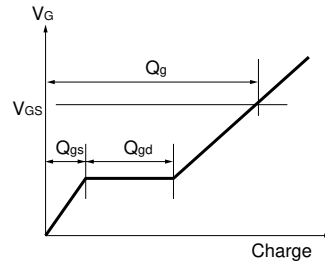


Fig.14 Gate Charge Waveform

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