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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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EMC1186

Dual Channel 1°C Temperature Sensor with Hardware Thermal Shutdown and 1.8V SMBus Communications

PRODUCT FEATURES

Datasheet

General Description

The EMC1186 is a high accuracy, low cost, 1.8V System Management Bus (SMBus) compatible temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 65nm and lower geometry processors) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications. The ability to communicate at 1.8V SMBus levels provides compatible I/O for the advanced processors found in today's tablet and smartphone applications.

The EMC1186 monitors two temperature channels (one external and one internal), providing ±1°C accuracy for both external and internal diode temperatures.

Additionally, the EMC1186provides a hardware programmable system shutdown feature that is programmed at part power-up via two pull-up resistor values and that cannot be masked or corrupted through the SMBus.

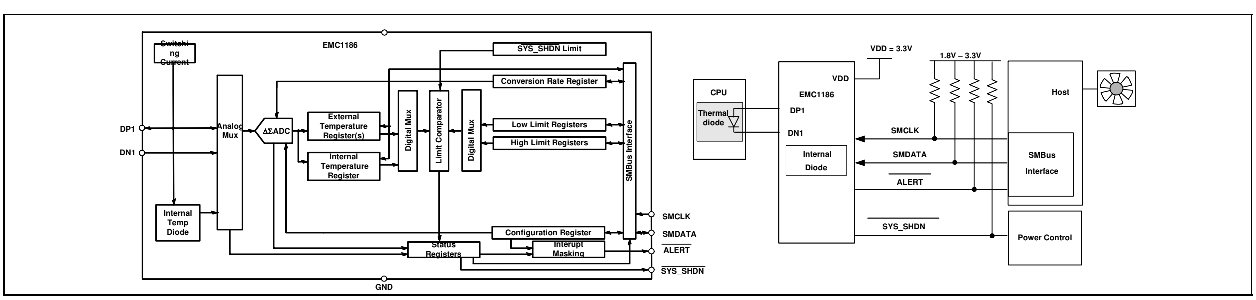
REC automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Frequency hopping* and analog filters ensure remote diode traces can be as far as eight (8) inches without degrading the signal. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus ±1°C measurement accuracy provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded applications

Features

- Hardware Thermal Shutdown
  - triggers dedicated SYS_SHDN pin
  - hardware configured range 77°C to 112°C in 1°C steps
  - cannot be disabled or modified by software
- Support for diodes requiring the BJT/transistor model
  - Supports 65nm and lower geometry CPU thermal diodes
- Pin and register compatible with EMC1422
- Automatically determines external diode type and optimal settings
- Resistance Error Correction
- Frequency hops the remote sample frequency to reject DC converter and other coherent noise sources*
- Consecutive Alert queue to further reduce false Alerts
- Up to 1 External Temperature Monitors
  - 25°C typ, ±1°C max accuracy (20°C < T_{DIODE} < 110°C)
  - 0.125°C resolution
  - Supports up to 2.2nF diode filter capacitor
- Internal Temperature Monitor
  - ±1°C accuracy
  - 0.125°C resolution
- 3.3V Supply Voltage
- 1.8V SMBus operation
- Programmable temperature limits for ALERT (85°C default high limit and 0°C default low limit)
- Available in small 8-pin 2mm x 3mm TDFN RoHS compliant package



*** Technology covered under the US patent 7,193,543.**

Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES	SMBUS ADDRESS
EMC1186-1-AC3-TR	8-pin TDFN 2mm x 3mm (RoHS compliant)	Two temperature sensors, hardware set system shutdown, ALERT and SYS_SHDN pins, fixed SMBus address	1001_100(r/w)
EMC1186-2-AC3-TR	8-pin TDFN 2mm x 3mm (RoHS compliant)	Two temperature sensors, hardware set system shutdown, ALERT and THERM pins, fixed SMBus address	1001_101(r/w)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Block Diagram

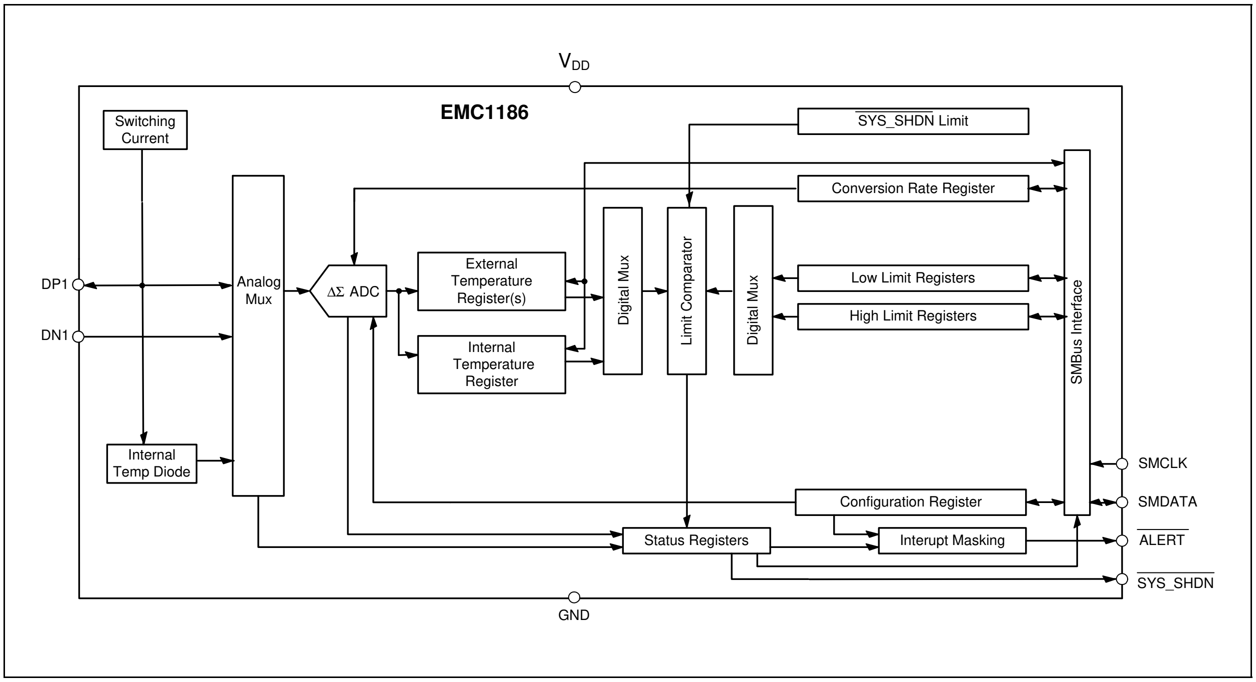

Figure 1.1 EMC1186 Block Diagram

Chapter 2 Pin Description

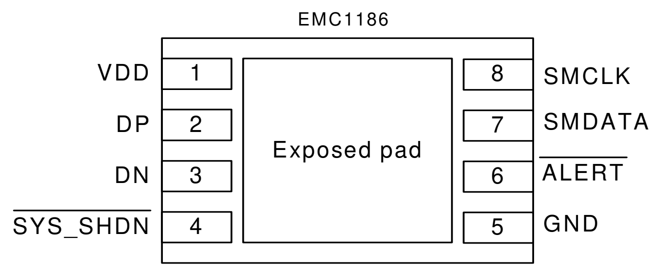

Figure 2.1 EMC1186 Pin Diagram, TDFN-8 2mm x 3mm

The pin types are described Table 2.2.

Table 2.1 EMC1186 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	VDD	Power supply	Power
2	DP	External diode positive (anode) connection	AIO
3	DN	External diode negative (cathode) connection	AIO
4	$\overline{\text{SYS\_SHDN}}$	Active low system shutdown output signal - requires pull-up resistor which selects the Hardware Thermal Shutdown Limit	OD (5V)
5	GND	Ground	Power
6	$\overline{\text{ALERT}}$	Active low digital $\overline{\text{ALERT}}$ output signal - requires pull-up resistor	OD (5V)
7	SMDATA	SMBus Data input/output - requires pull-up resistor	DIOD (5V)
8	SMCLK	SMBus Clock input - requires pull-up resistor	DI (5V)
Bottom Pad	Exposed Pad	Not internally connected, but recommend grounding.	-

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
AIO	Analog Input / Output -This pin is used as an I/O for analog signals.
DI	Digital Input - This pin is used as a digital input. This pin is 5V tolerant.
DIOD	Digital Input / Open Drain Output - This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\lvert V_{5VT\_pin} - V_{DD} \rvert$) (see Note 3.1)	0 to 3.6	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for DFN-10		
Thermal Resistance (θ_{j-a})	77.1	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{SYS\_SHDN}}$, and ALERT), the pull-up voltage must not exceed 3.6V when the device is unpowered.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}		200	410	µA	0.0625 conversion / sec, dynamic averaging disabled
			215	425	µA	1 conversion / sec, dynamic averaging disabled
			325	465	µA	4 conversions / sec, dynamic averaging disabled

Table 3.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
			890	1050	µA	4 conversions / sec, dynamic averaging enabled
			1120		µA	≥ 16 conversions / sec, dynamic averaging enabled
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	-5°C < T_A < 100°C
				±2	°C	-40°C < T_A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+20°C < T_{DIODE} < +110°C 0°C < T_A < 100°C
			±0.5	±2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Conversion Time all Channels	t_{CONV}		150		ms	default settings
Capacitive Filter	C_{FILTER}		2.2	2.7	nF	Connected across external diode
$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins						
Output Low Voltage	V_{OL}	0.4			V	I_{SINK} = 8mA
Leakage Current	I_{LEAK}			±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins Device powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V

3.3 SMBus Electrical Characteristics

Table 3.3 SMBus Electrical Specifications

V_{DD} = 3.0 to 3.6V, T_A = -40°C to 125°C, all typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	1.4		V_{DD}	V	5V Tolerant. Voltage threshold based on 1.8V operation
Input Low Voltage	V_{IL}	-0.3		0.8	V	5V Tolerant. Voltage threshold based on 1.8V operation
Leakage Current	I_{LEAK}			±5	µA	Powered or unpowered TA < 85°C

Table 3.3 SMBus Electrical Specifications (continued)

V_{DD} = 3.0 to 3.6V, T_A = -40°C to 125°C, all typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Hysteresis		50			mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current	I_{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3			µs	
Hold Time: Start	$t_{HD:STA}$	0.6			µs	
Setup Time: Start	$t_{SU:STA}$	0.6			µs	
Setup Time: Stop	$t_{SU:STO}$	0.6			µs	
Data Hold Time	$t_{HD:DAT}$	0			µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3			µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			µs	
Clock High Period	t_{HIGH}	0.6			µs	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line
Timeout	$t_{TIMEOUT}$	25		35	ms	Disabled by default

Chapter 4 System Management Bus Interface Protocol

4.1 Communications Protocol

The EMC1186 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1.

For the first 15ms after power-up the device may not respond to SMBus communications.

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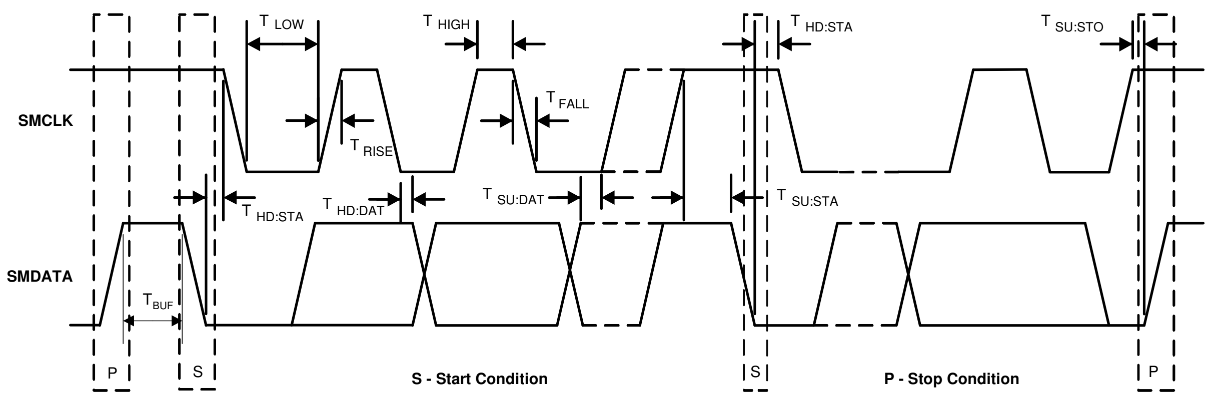

Figure 4.1 SMBus Timing Diagram

4.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

4.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, the SMBus Host is reading data from the client device.

The EMC1186-1 SMBus address is hard coded to 1001_100(r/$\overline{w}$).

The EMC1186-2 SMBus address is hard coded to 1001_101(r/$\overline{w}$).

4.1.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

4.1.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to the Write Byte protocol.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent.

4.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the device detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

4.1.6 SMBus Timeout

The EMC1186 supports SMBus Timeout. If the clock line is held low for longer than $t_{TIMEOUT}$, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit (see Section 6.11, "Consecutive ALERT Register 22h").

4.1.7 SMBus and I^2C Compatibility

The EMC1186 is compatible with SMBus and I^2C. The major differences between SMBus and I^2C devices are highlighted here. For more information, refer to the SMBus 2.0 and I^2C specifications. For information on using the EMC1186 in an I^2C system, refer to SMSC AN 14.0 SMSC Dedicated Slave Devices in I^2C Systems.

1. EMC1186 supports I^2C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
2. Minimum frequency for SMBus communications is 10kHz.
3. The SMBus client protocol will reset if the clock is held at a logic ‘0’ for longer than 30ms. This timeout functionality is disabled by default in the EMC1186 and can be enabled by writing to the TIMEOUT bit. I^2C does not have a timeout.
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

Attempting to communicate with the EMC1186 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

4.2 SMBus Protocols

The device supports Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers, as shown in Table 4.2.

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

4.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_ YYY	0	0	XXh	0	1 -> 0	YYYY_ YYY	1	0	XX	1	0 -> 1

4.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1

4.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

4.3 Alert Response Address

The ALERT output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the ALERT pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	YYYY_YYY	1	0 -> 1

The EMC1186 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK_ALL bit to clear the ALERT pin.

APPLICATION NOTE: The ARA does not clear the Status Register and if the MASK_ALL bit is cleared prior to the Status Register being cleared, the ALERT pin will be reasserted.

Chapter 5 Product Description

The is an SMBus temperature sensor with Hardware Thermal Shutdown. The EMC1186 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1186 and using that data to control the speed of one or more fans.

The EMC1186 has two levels of monitoring. The first provides a maskable ALERT signal to the host when the measured temperatures exceeds user programmable limits. This allows the EMC1186 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring asserts the SYS_SHDN pin when the External Diode 1 temperature exceeds a hardware specified threshold temperature. Additionally, the internal diode can be configured to assert the SYS_SHDN pin when the measured temperature exceeds user programmable limits.

Figure 5.1 shows a system level block diagram of the EMC1186.

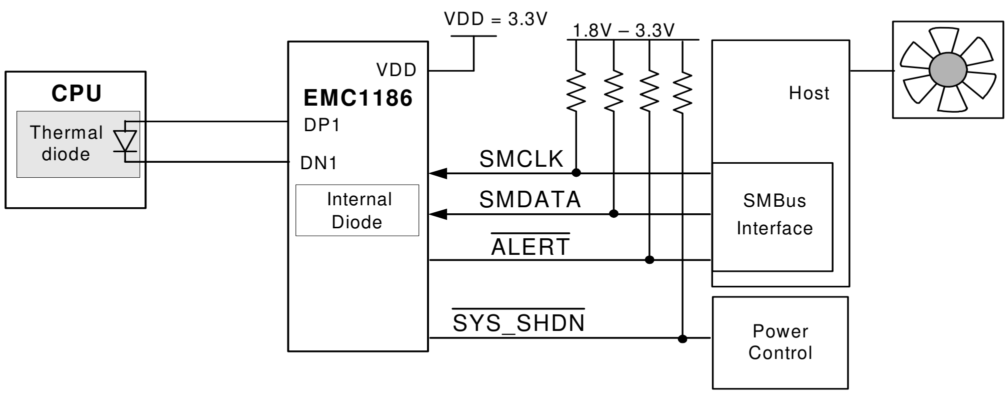

Figure 5.1 System Diagram for EMC1186

5.1 Conversion Rates

The EMC1186 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 6.4. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 6.5, "Conversion Rate".

5.2 Dynamic Averaging

Dynamic averaging causes the EMC1186 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 6.3, "Configuration Register 03h / 09h"). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 5.1.

Table 5.1 Supply Current vs. Conversion Rate for EMC1186

CONVERSION RATE	AVERAGE SUPPLY CURRENT (TYPICAL)		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	ENABLED (DEFAULT)	DISABLED	ENABLED (DEFAULT)	DISABLED
1 / 16 sec	210uA	200uA	16x	1x
1 / 8 sec	265uA	200uA	16x	1x
1 / 4 sec	330uA	200uA	16x	1x
1 / 2 sec	395uA	200uA	16x	1x
1 / sec	460uA	215uA	16x	1x
4 / sec (default)	890uA	325uA	8x	1x
8 / sec	1010uA	630uA	4x	1x
16 / sec	1120uA	775uA	2x	1x
32 / sec	1200uA	1050uA	1x	1x
64 / sec	1400uA	1100uA	0.5x	0.5x

5.3 .SYS_SHDN Output

The SYS_SHDN output is asserted independently of the ALERT output and cannot be masked. If the External Diode 1 temperature exceeds the Hardware Thermal Shutdown Limit for the programmed number of consecutive measurements, the SYS_SHDN pin is asserted.

The Hardware Thermal Shutdown Limit is defined at power-up via the pull-up resistors on the SYS_SHDN and ALERT pins as shown in Table 5.2. This limit cannot be modified or masked via software.

In addition to External Diode 1 channel triggering the SYS_SHDN pin when the measured temperature exceeds to the Hardware Thermal Shutdown Limit, each of the measurement channels can be configured to assert the SYS_SHDN pin when they exceed the corresponding THERM Limit.

When the SYS_SHDN pin is asserted, it will not release until the External Diode 1 temperature drops below the Hardware Thermal Shutdown Limit minus 10°C and all other measured temperatures drop below the THERM Limit minus the THERM Hysteresis value (when linked to SYS_SHDN).

Figure 5.2 shows a block diagram of the interaction between the input channels and the SYS_SHDN pin.

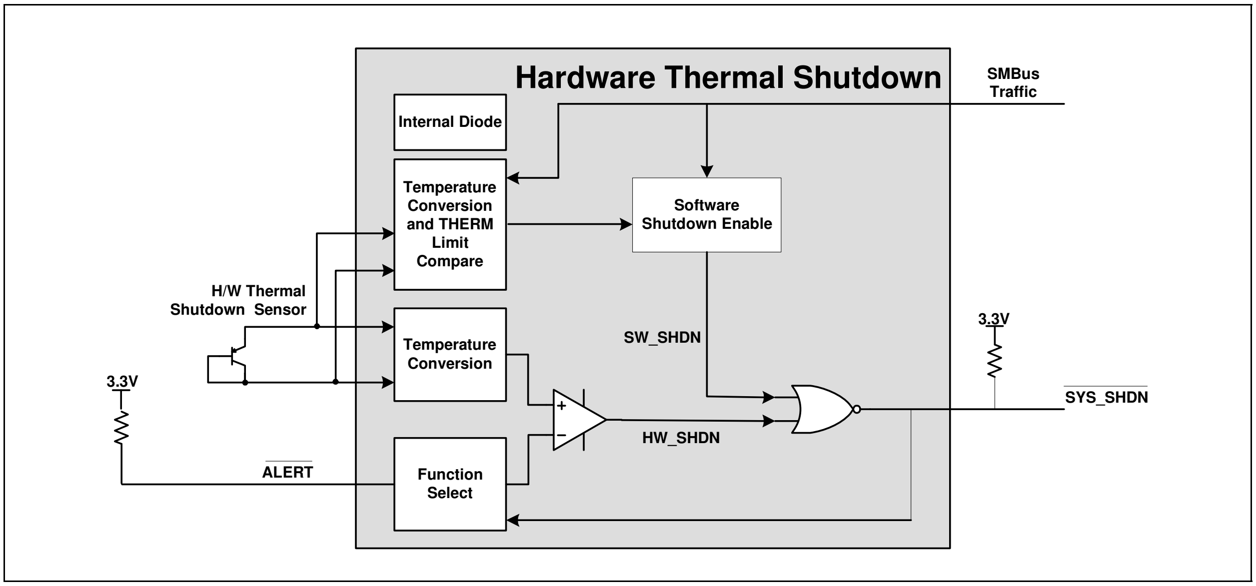

Figure 5.2 Block Diagram of Hardware Thermal Shutdown

5.4 Hardware Thermal Shutdown Limit

The Hardware Thermal Shutdown Limit temperature is determined by pull-up resistors on the SYS_SHDN and ALERT pins shown in Table 5.2.

Table 5.2 SYS_SHDN Threshold Temperature

SYS_SHD PULL-UP / ALERT PULL-UP	4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10K OHM ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM ±10%	82°C	88°C	94°C	100°C	106°C	112°C

5.5 ALERT Output

The ALERT pin is an open drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: interrupt mode and comparator mode. The mode of the ALERT output is selected via the ALERT / COMP bit in the Configuration Register (see Section 6.3).

5.5.1 ALERT Pin Interrupt Mode

When configured to operate in interrupt mode, the ALERT pin asserts low when an out of limit measurement (≥ high limit or ≤ low limit) is detected on any diode or when a diode fault is detected, functioning as any standard ALERT in on the SMBus. The ALERT pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT pin will remain asserted until the appropriate status bits are cleared.

The ALERT pin can be masked by setting the MASK_ALL bit. Once the ALERT pin has been masked, it will be de-asserted and remain de-asserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the ALERT pin is masked will update the Status Register normally. There are also individual channel masks (see Section 6.10).

The ALERT pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more ALERT outputs can be hard-wired together.

5.5.2 ALERT Pin Comparator Mode

When the ALERT pin is configured to operate in comparator mode, it will be asserted if any of the measured temperatures exceeds the respective high limit. The ALERT pin will remain asserted until all temperatures drop below the corresponding high limit minus the Therm Hysteresis value.

When the ALERT pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the ALERT pin is deasserted. Once the ALERT pin is deasserted, the status bits will be automatically cleared.

The MASK_ALL bit will not block the ALERT pin in this mode; however, the individual channel masks (see Section 6.10) will prevent the respective channel from asserting the ALERT pin.

5.6 ALERT and SYS_SHDN Pin Considerations

Because of the decode method used to determine the Hardware Thermal Shutdown Limit, it is important that the pull-up resistance on both the ALERT and SYS_SHDN pins be within the tolerances shown in Table 5.2. Additionally, the pull-up resistor on the ALERT and SYS_SHDN pins must be connected to the same 3.3V supply that drives the VDD pin.

For 15ms after power up, the ALERT and SYS_SHDN pins must not be pulled low or the Hardware Thermal Shutdown Limit will not be decoded properly. If the system requirements do not permit these conditions, the ALERT and SYS_SHDN pins must be isolated from their respective busses during this time.

One method of isolating the ALERT pin is shown in Figure 5.3.

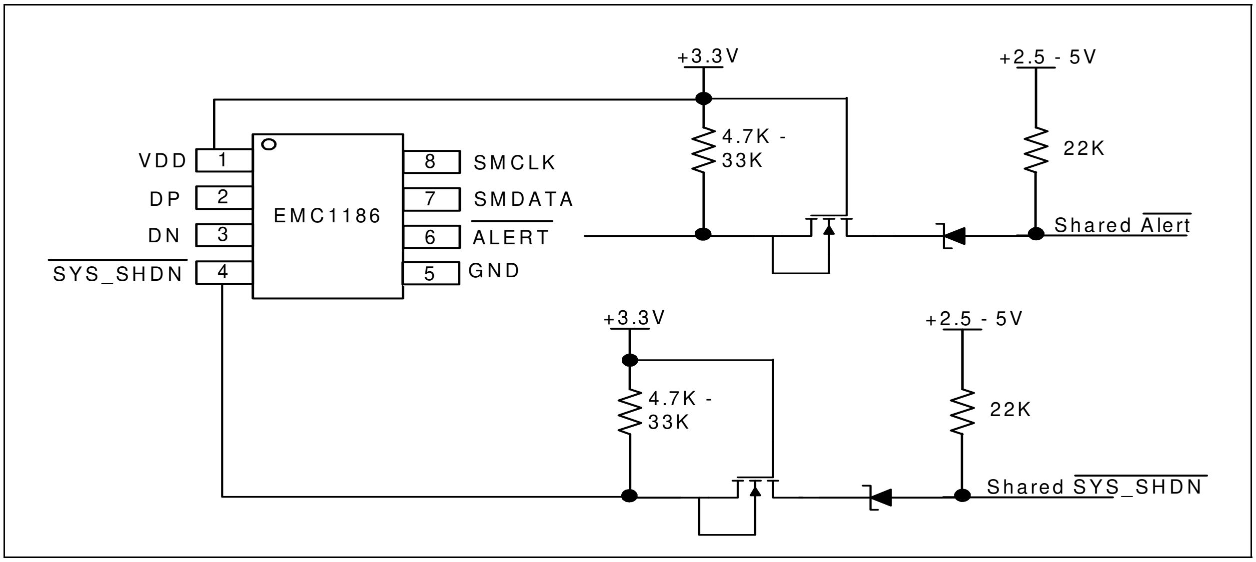

Figure 5.3 Isolating ALERT and SYS_SHDN Pin

5.7 Temperature Measurement

The EMC1186 can monitor the temperature of one externally connected diodes.

The device contains programmable High, Low, and Therm limits for all measured temperature channels. If the measured temperature goes below the Low limit or above the High limit, the ALERT pin can be asserted (based on user settings).

5.7.1 Beta Compensation

The EMC1186 is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU thermal diodes. For External Diode 1, it automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

5.7.2 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1186 automatically corrects up to 100 ohms of series resistance.

5.7.3 Programmable External Diode Ideality Factor

The EMC1186 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1186 provides a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

APPLICATION NOTE: When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

5.8 Diode Faults

The EMC1186 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the $\overline{\text{ALERT}}$ pin asserts (unless masked, see Section 5.9) and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the $\overline{\text{ALERT}}$ pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

5.9 Consecutive Alerts

The EMC1186 contain multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{SYS\_SHDN}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the $\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See Section 6.11, "Consecutive ALERT Register 22h" for more details on the consecutive alert function.

5.10 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode 1 channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled (default) (see Section 6.13). The typical filter performance is shown in Figure 5.4 and Figure 5.5.

Figure 5.4 Temperature Filter Step Response

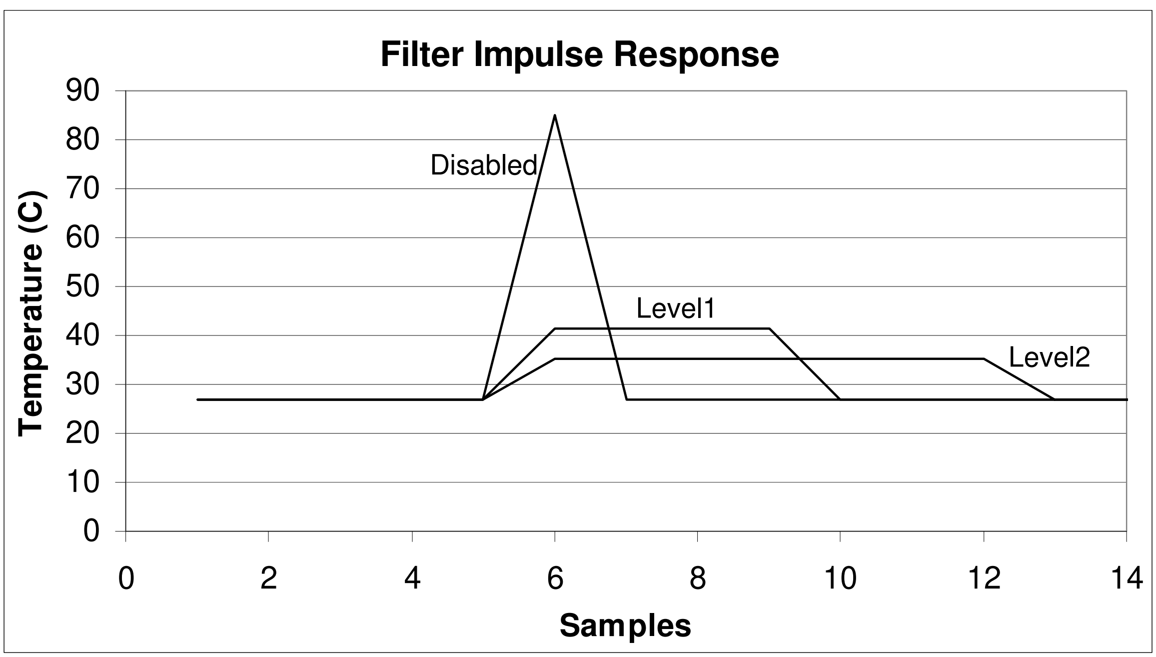

Figure 5.5 Temperature Filter Impulse Response

5.11 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1186 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 5.3 shows the default and extended range formats.

Table 5.3 Temperature Data Format

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE -64°C TO 191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000
-1	000 0000 0000	001 1111 1000
0	000 0000 0000	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
>= 191.875	011 1111 1111	111 1111 1111

Chapter 6 Register Description

The registers shown in Table 6.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 6.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 27
01h	R	External Diode 1 Data High Byte	Stores the integer data for External Diode 1	00h	
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 28
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 29
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 29
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	
07h	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 0Dh)	55h (85°C)	
08h	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 0Eh)	00h (0°C)	
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 28
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 29