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1°C Temperature Sensor with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC1422 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm, 65nm and 90nm processors) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Additionally, the EMC1422 provides a hardware programmable system shutdown feature that is programmed at part power-up via two pull-up resistor values and that cannot be masked or corrupted through the SMBus.

Each device provides $\pm 1^\circ$ accuracy for external diode temperatures and $\pm 2^\circ$ accuracy for the internal diode temperature. The EMC1422 monitors two temperature channels (one external and one internal).

Resistance Error Correction automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus $\pm 1^\circ$ C measurement accuracy provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded applications

Features

- Hardware Thermal Shutdown
 - triggers dedicated `SYS_SHDN` pin
 - hardware configured range 77°C to 112°C in 1°C steps
 - cannot be disabled or modified by software
- Support for diodes requiring the BJT/transistor model
 - supports 45nm, 65nm, and 90nm CPU thermal diodes.
- Pin compatible with ADM1032, MAX6649, and LM99
- Automatically determines external diode type and optimal settings
- Resistance Error Correction
- External Temperature Monitors
 - $\pm 1^\circ$ C Accuracy ($60^\circ\text{C} < T_{\text{DIODE}} < 100^\circ\text{C}$)
 - 0.125°C Resolution
 - Supports up to 2.2nF diode filter capacitor
- Internal Temperature Monitor
 - $\pm 2^\circ$ C accuracy
- 3.3V Supply Voltage
- Programmable temperature limits for `ALERT`
- Available in Small 8-pin MSOP Lead-free RoHS Compliant Package

Ordering Information:**EMC1422-1-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE****Note:** See [Table 1.1, "Part Selection"](#) for SMBus addressing options.**REEL SIZE IS 4,000 PIECES.****This product meets the halogen maximum concentration values per IEC61249-2-21****For RoHS compliance and environmental information, please visit www.smSC.com/rohs***Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.*

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Chapter 1 Block Diagram

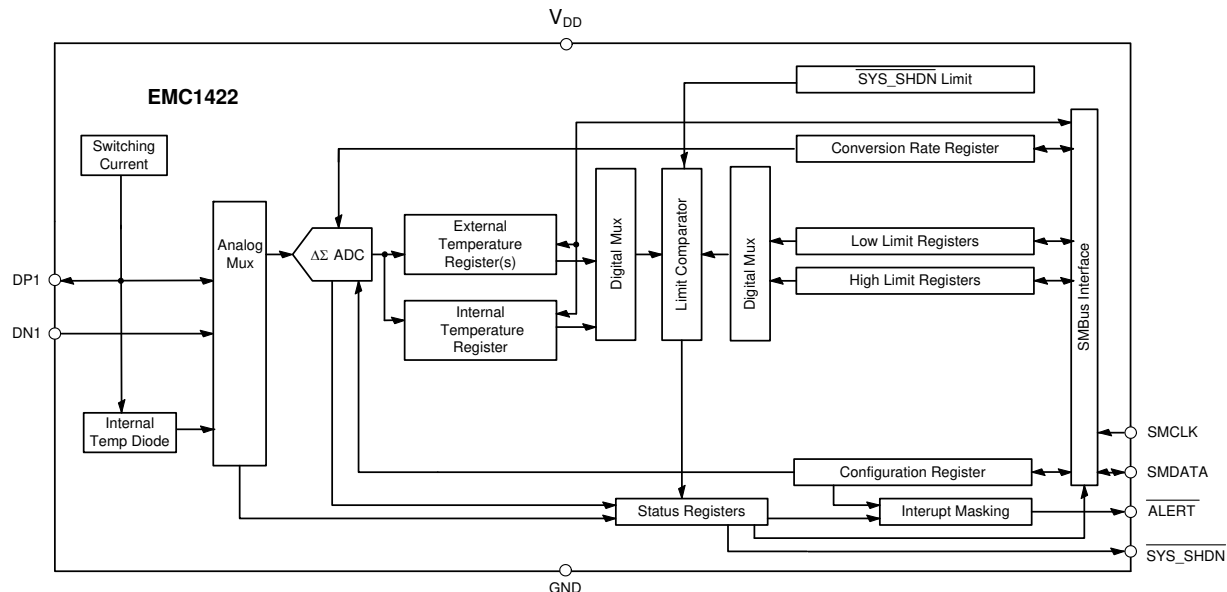


Figure 1.1 EMC1422 Block Diagram

1.1 Part Selection

The EMC1422 device configuration is highlighted below.

Table 1.1 Part Selection

PART NUMBER	SMBUS ADDRESS	FUNCTIONALITY				PRODUCT ID
		EXTERNAL DIODES	DIODE 1 DEFAULT CONFIGURATION	DIODE 2 DEFAULT CONFIGURATION	OTHER	
EMC1422 - 1	1001_100xb	1	Detect Diode w/ REC enabled	N/A	Software programmable and maskable High Limit Software programmable and maskable SYS_SHDN Limit Hardware set SYS_SHDN Limit on External Diode 1	22h

Chapter 2 Pin Description

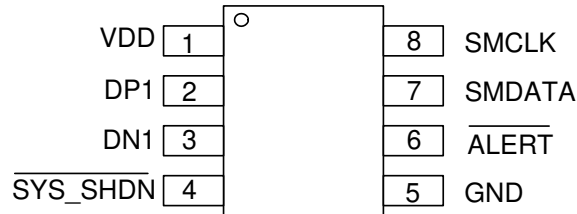


Figure 2.1 EMC1422 Pin Diagram

Table 2.1 EMC1422 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	VDD	Power supply	Power
2	DP	External diode positive (anode) connection	AIO
3	DN	External diode negative (cathode) connection	AIO
4	$\overline{\text{SYS_SHDN}}$	Active low System Shutdown output signal - requires pull-up resistor which selects the Hardware Thermal Shutdown Limit	OD (5V)
5	GND	Ground	Power
6	$\overline{\text{ALERT}}$	Active low digital $\overline{\text{ALERT}}$ output signal - requires pull-up resistor	OD (5V)
7	SMDATA	SMBus Data input/output - requires pull-up resistor	DIOD (5V)
8	SMCLK	SMBus Clock input - requires pull-up resistor	DI (5V)

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{SYS_SHDN}}$, and $\overline{\text{ALERT}}$), the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

The pin types are described below:

Power - these pins are used to supply either VDD or GND to the device.

AIO - Analog Input / Output.

DI - Digital Input.

OD - Open Drain Digital Output.

DIOD - Digital Input / Open Drain Output.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($ V_{5VT_pin} - V_{DD} $) (see Note 3.1)	-0.3 to 3.6	V
Voltage on any other pin to Ground	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for MSOP-8		
Thermal Resistance (θ_{j-a})	140.8	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{SYS_SHDN}}$, and $\overline{\text{ALERT}}$), the pull-up voltage must not exceed 3.6V when the device is unpowered.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values at T _A = 27°C unless otherwise noted.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
DC Power						
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Supply Current	I _{DD}		430	850	µA	1 conversion / sec, dynamic averaging disabled
			930	1200	µA	4 conversions / sec, dynamic averaging enabled
			1120		µA	≥ 16 conversions / sec, dynamic averaging enabled
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	-5°C < T _A < 100°C
				±2	°C	-40°C < T _A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+20°C < T _{DIODE} < +110°C 0°C < T _A < 100°C
			±0.5	±2	°C	-40°C < T _{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Conversion Time all Channels	t _{CONV}		190		ms	EMC1422, default settings
Capacitive Filter	C _{FILTER}		2.2	2.5	nF	Connected across external diode
$\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins						
Output Low Voltage	V _{OL}	0.4			V	I _{SINK} = 8mA
Leakage Current	I _{LEAK}			±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins Device powered or unpowered T _A < 85°C pull-up voltage ≤ 3.6V
Power up time				15	ms	Temp selection read Note 3.2

Note 3.2 During the power up time, SMBus communication is permitted, however the $\overline{\text{SYS_SHDN}}$ and $\overline{\text{ALERT}}$ pins must not be pulled low.

3.3 SMBus Electrical Characteristics

Table 3.3 SMBus Electrical Specifications

V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values are at T _A = 27°C unless otherwise noted.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
SMBus Interface						
Input High Voltage	V _{IH}	2.0		V _{DD}	V	5V Tolerant
Input Low Voltage	V _{IL}	-0.3		0.8	V	5V Tolerant
Input High/Low Current	I _{IH} / I _{IL}			±5	uA	Powered or unpowered T _A < 85°C
Hysteresis			420		mV	
Input Capacitance	C _{IN}		5		pF	
Output Low Sink Current	I _{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f _{SMB}	10		400	kHz	
Spike Suppression	t _{SP}			50	ns	
Bus free time Start to Stop	t _{BUF}	1.3			us	
Hold Time: Start	t _{HD:STA}	0.6			us	
Setup Time: Start	t _{SU:STA}	0.6			us	
Setup Time: Stop	t _{SU:STP}	0.6			us	
Data Hold Time	t _{HD:DAT}	0			us	When transmitting to the master
Data Hold Time	t _{HD:DAT}	0.3			us	When receiving from the master
Data Setup Time	t _{SU:DAT}	100			ns	
Clock Low Period	t _{LOW}	1.3			us	
Clock High Period	t _{HIGH}	0.6			us	
Clock/Data Fall time	t _{FALL}			300	ns	Min = 20+0.1C _{LOAD} ns
Clock/Data Rise time	t _{RISE}			300	ns	Min = 20+0.1C _{LOAD} ns
Capacitive Load	C _{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC1422 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in [Figure 4.1](#).

For the first 15ms after power-up the device may not respond to SMBus communications.

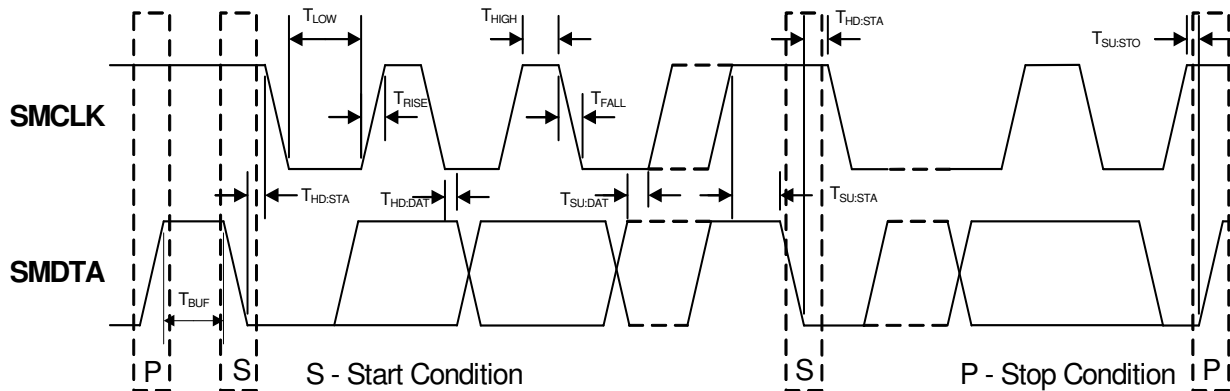


Figure 4.1 SMBus Timing Diagram

The EMC1422 is SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in [Table 4.1](#).

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

Attempting to communicate with the EMC1422 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below [Table 4.2](#):

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	1001_100	0	0	XXh	0	XXh	0	0 -> 1

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in [Table 4.3](#).

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	1001_100	0	1	XXh	0	1 -> 0	1001_100	1	1	XX	1	0 -> 1

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in [Table 4.4](#).

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	1001_100	0	0	XXh	0	0 -> 1

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in [Table 4.5](#).

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	1001_100	1	0	XXh	1	0 -> 1

4.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in [Table 4.6](#).

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	1001_1000	1	0 -> 1

The EMC1422 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

APPLICATION NOTE: The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

4.7 SMBus Address

The EMC1422 responds to hard-wired SMBus slave address as shown in [Table 1.1](#).

Note: Other addresses are available. Contact SMSC for more information.

4.8 SMBus Timeout

The EMC1422 supports SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (see [Section 6.13](#)).

Chapter 5 Product Description

The EMC1422 is an SMBus temperature sensor with Hardware Thermal Shutdown. The EMC1422 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1422 and using that data to control the speed of one or more fans.

The EMC1422 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when measured temperatures meet or exceed user programmable limits. This allows the EMC1422 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host.

The second level of monitoring asserts the $\overline{\text{SYS_SHDN}}$ pin when the External Diode temperature exceeds a hardware specified threshold temperature. Additionally, the internal diode can be configured to assert the $\overline{\text{SYS_SHDN}}$ pin when the measured temperature exceeds user programmable limits.

Since the EMC1422 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available with non-resistance error correcting devices. The automatic beta detection feature means that there is no need to program the device according to which type of diode is present. This also includes CPU diodes that require the transistor or BJT model for monitoring their temperature. Therefore, the EMC1422 can power up ready to operate for any system configuration.

Figure 5.1 shows a system level block diagram of the EMC1422.

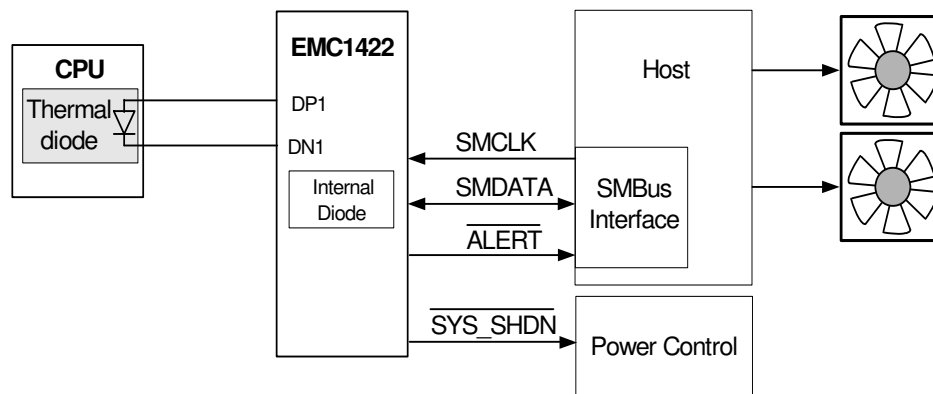


Figure 5.1 System Diagram for EMC1422

5.0.1 Conversion Rates

The EMC1422 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 6.5. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 6.6.

5.0.2 Dynamic Averaging

Dynamic averaging causes the EMC1422 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 6.4). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel)

while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in [Table 5.1](#) for the EMC1422.

Table 5.1 Supply Current vs. Conversion Rate for EMC1422

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	ENABLED (DEFAULT)	DISABLED	ENABLED (DEFAULT)	DISABLED
1 / sec	660uA	430uA	16x	1x
2 / sec	930uA	475uA	16x	1x
4 / sec (default)	950uA	510uA	8x	1x
8 / sec	1010uA	630uA	4x	1x
16 / sec	1020uA	775uA	2x	1x
32 / sec	1050uA	1050uA	1x	1x
64 / sec	1100uA	1100uA	0.5x	0.5x

5.1 SYS_SHDN Output

The SYS_SHDN output is asserted independently of the ALERT output and cannot be masked. If the External Diode temperature exceeds the Hardware Thermal Shutdown Limit for the programmed number of consecutive measurements, then the SYS_SHDN pin is asserted.

The Hardware Thermal Shutdown Limit is defined at power-up via the pull-up resistors on the SYS_SHDN and ALERT pins as shown in [Table 5.2](#). This limit cannot be modified or masked via software.

In addition to External Diode channel triggering the SYS_SHDN pin when the measured temperature exceeds to the Hardware Thermal Shutdown Limit, each of the measurement channels can be configured to assert the SYS_SHDN pin when they exceed the corresponding THERM Limit.

When the SYS_SHDN pin is asserted, it will not release until the External Diode temperature drops below the Hardware Thermal Shutdown Limit minus 10°C and all other measured temperatures drop below the THERM Limit minus the THERM Hysteresis value (when linked to SYS_SHDN).

[Figure 5.2](#) shows a block diagram of the interaction between the input channels and the SYS_SHDN pin.

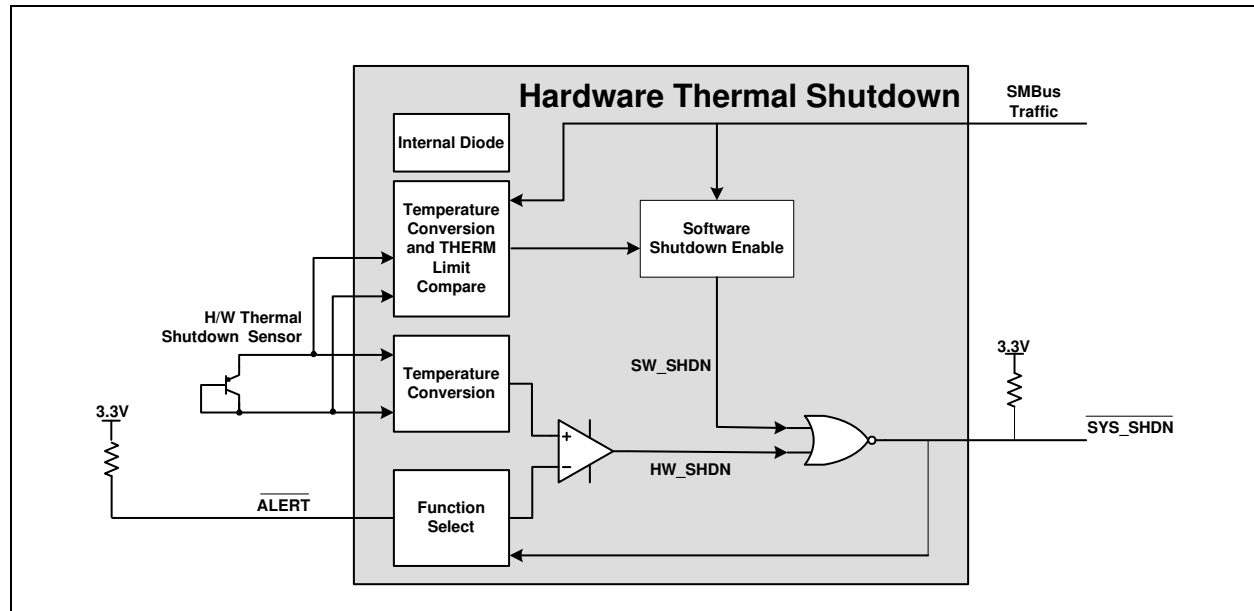


Figure 5.2 Block Diagram of Hardware Thermal Shutdown

5.2 Hardware Thermal Shutdown Limit

The Hardware Thermal Shutdown Limit temperature is determined by pull-up resistors on the SYS_SHDN and ALERT pins shown in [Table 5.2](#).

Table 5.2 SYS_SHDN Threshold Temperature

<u>SYS_SHD</u> PULL-UP <u>ALERT</u> PULL-UP	4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10K OHM ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM ±10%	82°C	88°C	94°C	100°C	106°C	112°C

5.3 ALERT Output

The ALERT pin is an open drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: interrupt mode and comparator Mode. The mode of the ALERT output is selected via the ALERT / COMP bit in the Configuration Register (see [Section 6.4](#)).

5.3.1 ALERT Pin Interrupt Mode

When configured to operate in interrupt mode, the $\overline{\text{ALERT}}$ pin asserts low when an out of limit measurement (\geq high limit or $<$ low limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}$ pin can be masked by setting the MASK bit. Once the $\overline{\text{ALERT}}$ pin has been masked, it will be de-asserted and remain de-asserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the Status Register normally.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an Smbus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more $\overline{\text{ALERT}}$ outputs can be hard-wired together.

5.3.2 ALERT Pin Comparator Mode

When the ALERT pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures exceeds the respective high limit. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the $\overline{\text{ALERT}}$ pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. Once the $\overline{\text{ALERT}}$ pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the $\overline{\text{ALERT}}$ pin in this mode, however the individual channel masks (see [Section 6.12](#)) will prevent the respective channel from asserting the $\overline{\text{ALERT}}$ pin.

5.4 ALERT and SYS_SHDN Pin Considerations

Because of the decode method used to determine the Hardware Thermal Shutdown Limit, it is important that the pull-up resistance on both the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins be within the tolerances shown in [Table 5.2](#). Additionally, the pull-up resistor on the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins must be connected to the same 3.3V supply that drives the VDD pin.

For 15ms after power up, the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins must not be pulled low or the Hardware Thermal Shutdown Limit will not be decoded properly. If the system requirements do not permit these conditions, then the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins must be isolated from their respective busses during this time.

One method of isolating this pin is shown in [Figure 5.3](#).

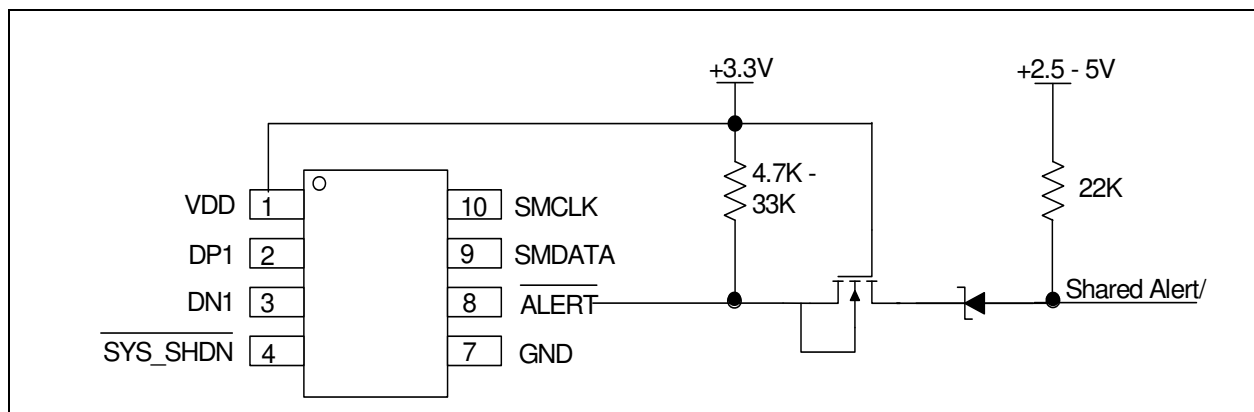


Figure 5.3 Isolating $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ Pins

5.5 Beta Compensation

The EMC1422 is configured to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

5.6 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1422 automatically corrects up to 100 ohms of series resistance.

APPLICATION NOTE: When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

5.7 Diode Faults

The EMC1422 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see [Section 5.8](#)) and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000degC (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

5.8 Consecutive Alerts

The EMC1422 contains multiple consecutive alert counters. One set of counters applies to the ALERT pin and the second set of counters applies to the SYS_SHDN pin. Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT and SYS_SHDN pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See [Section 6.13](#) for more details on the consecutive alert function.

5.9 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled. The typical filter performance is shown in [Figure 5.4](#) and [Figure 5.5](#).

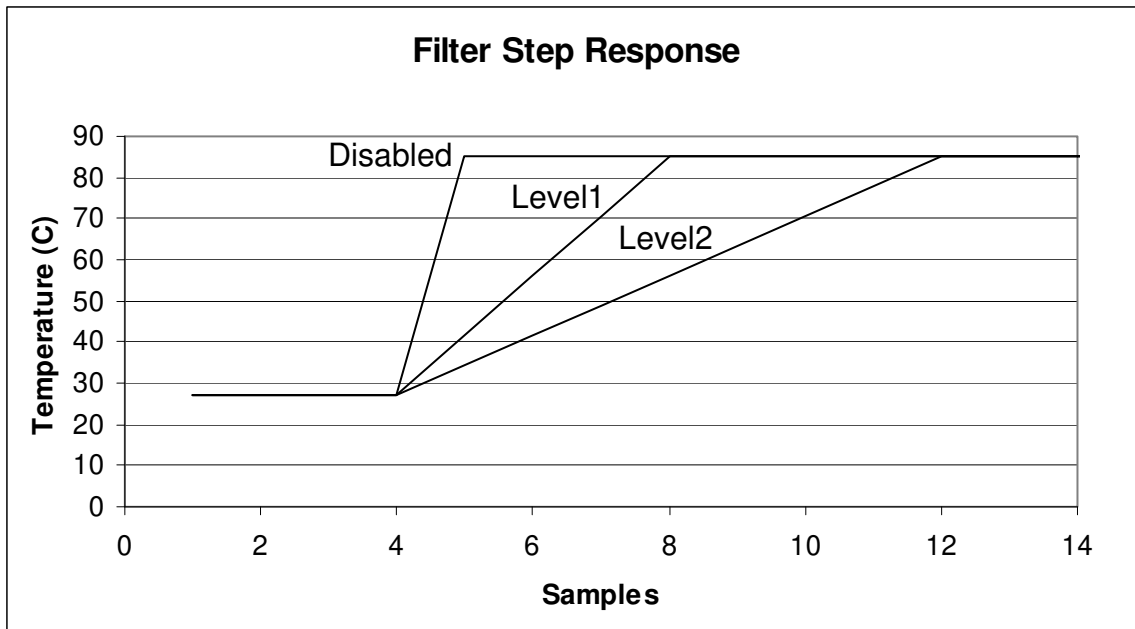


Figure 5.4 Temperature Filter Step Response

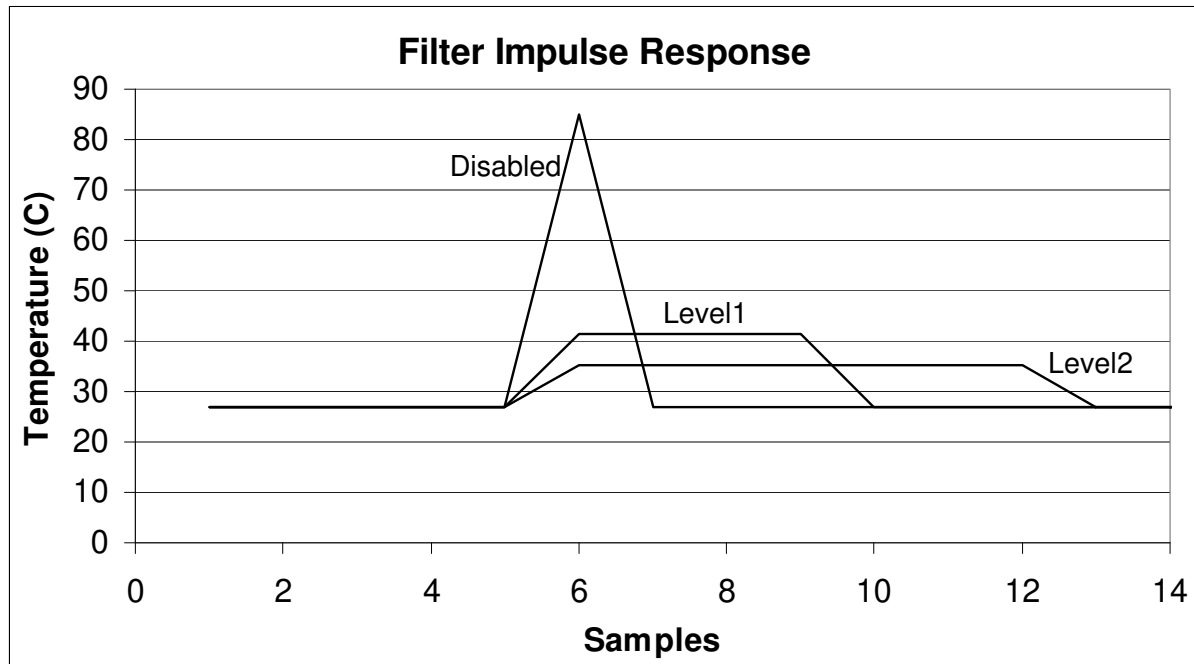


Figure 5.5 Temperature Filter Impulse Response

5.10 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. This ΔV_{BE} is proportional to absolute temperature as shown in the following equation:

$$\Delta V_{BE} = \frac{\eta kT}{q} \ln \left(\frac{I_{HIGH}}{I_{LOW}} \right)$$

where:

k = Boltzmann's constant

T = absolute temperature in Kelvin [1]

q = electron charge

η = diode ideality factor

Figure 5.6 shows a block diagram of the temperature measurement circuit. The negative terminal for the remote temperature diode, DN, is internally biased with a forward diode voltage referenced to ground.

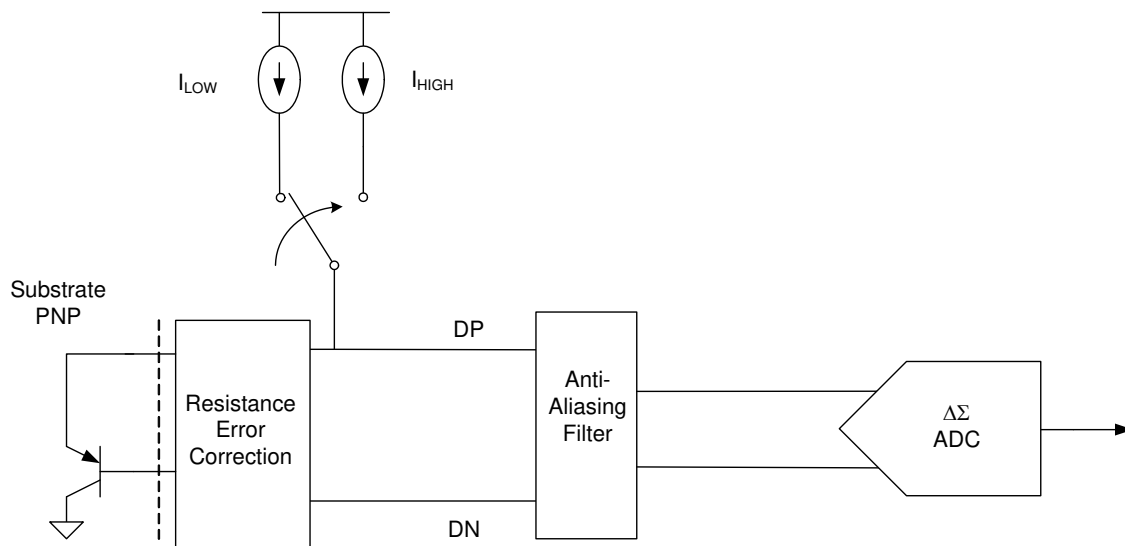


Figure 5.6 Block Diagram of Temperature Monitoring Circuit

5.11 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1422 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 5.3 shows the default and extended range formats.

Table 5.3 Temperature Data Format

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE -64°C TO 191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 Note 5.2
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 Note 5.1	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000

Table 5.3 Temperature Data Format (continued)

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE -64°C TO 191°C
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 Note 5.3	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
>= 191.875	011 1111 1111	111 1111 1111 Note 5.4

Note 5.1 In default mode, all temperatures < 0°C will be reported as 0°C.

Note 5.2 In the extended range, all temperatures < -64°C will be reported as -64°C.

Note 5.3 For the default range, all temperatures > +127.875°C will be reported as +127.875°C.

Note 5.4 For the extended range, all temperatures > +191.875°C will be reported as +191.875°C.

5.12 External Diode Connections

The EMC1422 is hard-wired to measure a specific kind of thermal diode and none of the measurement options can be changed by software. [Figure 5.7](#) shows the different diode configurations.

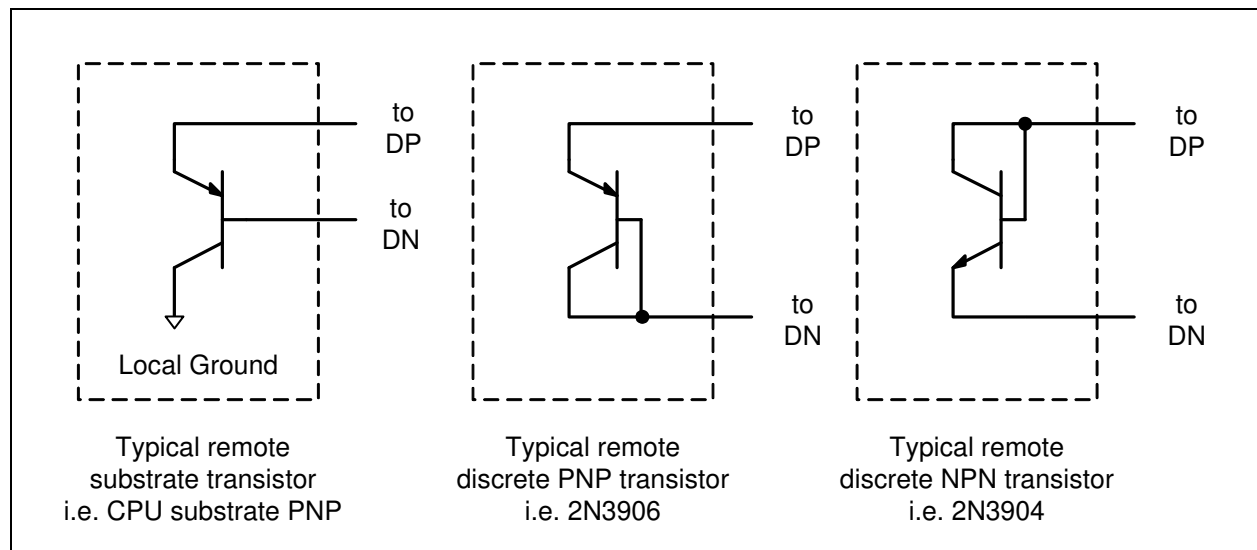


Figure 5.7 Diode Configurations

Chapter 6 Register Description

The registers shown in [Table 6.1](#) are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 6.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 26
01h	R	External Diode Data High Byte	Stores the integer data for the External Diode	00h	
02h	R	Status	Stores the status bits for the Internal Diode and External Diodes	00h	Page 26
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 27
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 28
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 29
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	
07h	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for the External Diode (mirrored at register 0Dh)	55h (85°C)	
08h	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for the External Diode (mirrored at register 0Eh)	00h (0°C)	
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 27
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 28

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 29
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)	
0Dh	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for the External Diode (mirrored at register 07h)	55h (85°C)	
0Eh	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for the External Diode (mirrored at register 08h)	00h (0°C)	
10h	R	External Diode Data Low Byte	Stores the fractional data for the External Diode	00h	Page 26
11h	R/W	Scratchpad	Scratchpad register for software compatibility	00h	Page 29
12h	R/W	Scratchpad	Scratchpad register for software compatibility	00h	Page 29
13h	R/W	External Diode High Limit Low Byte	Stores the fractional portion of the high limit for the External Diode	00h	Page 29
14h	R/W	External Diode Low Limit Low Byte	Stores the fractional portion of the low limit for the External Diode	00h	
19h	R/W	External Diode THERM Limit	Stores the 8-bit critical temperature limit for the External Diode	55h (85°C)	Page 30
1Dh	R/W	SYS_SHDN Configuration	Controls which software channels, if any, are linked to the SYS_SHDN pin	00h	Page 30
1Eh	R	Hardware Thermal Shutdown Limit	When read, returns the selected Hardware Thermal Shutdown Limit	N/A	Page 31
1Fh	R/W	Channel Mask Register	Controls the masking of individual channels	00h	Page 31
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (85°C)	Page 30
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted	70h	Page 32
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h	Page 26
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 33
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 34