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EMC1428

1°C Multiple Temperature Sensor with HW Thermal Shutdown & Hottest of Thermal Zones

PRODUCT FEATURES

Data Sheet

General Description

The EMC1428 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to CPU diodes requiring the BJT or transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Additionally, the EMC1428 provides a hardware programmable system shutdown feature that is programmed at part power-up via a single TRIP_SET voltage channel that cannot be masked or corrupted through the SMBus.

The EMC1428 provides ±1° accuracy for external diode temperatures and ±2°C accuracy for the internal diode temperature. The device monitors up to eight temperature channels (up to seven external and one internal).

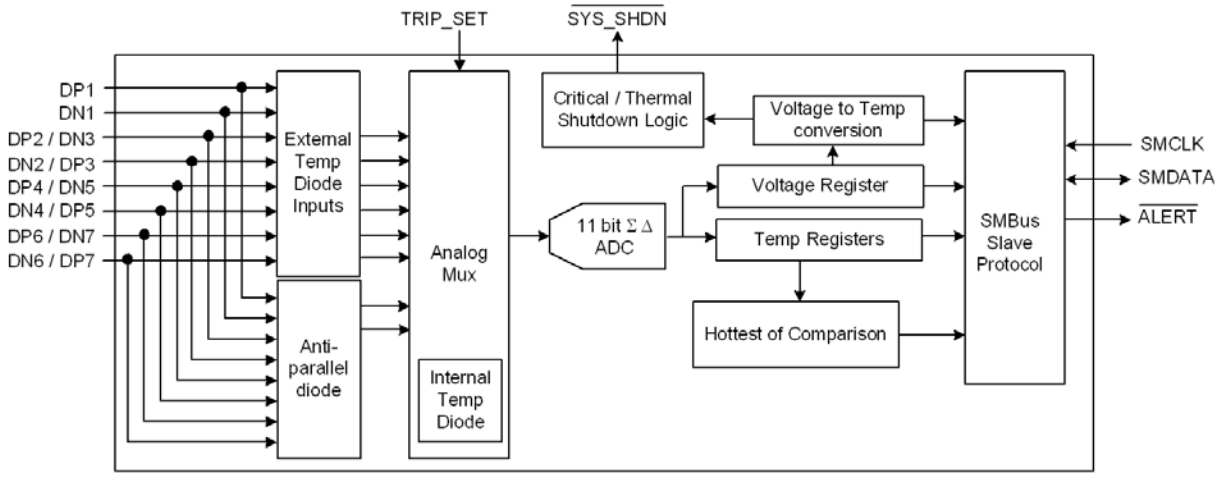
Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Features

- Hardware Thermal Shutdown
  - triggers dedicated $\overline{\text{SYS\_SHDN}}$ pin
  - hardware configured range 65°C to 127°C in 1°C steps
  - cannot be disabled or modified by software
- Supports diodes requiring the BJT or transistor model
- Resistance Error Correction (up to 100 Ohms)
- Up to seven External Temperature Monitors
  - ±1°C Accuracy (60°C < T_{DIODE} < 100°C)
  - 0.125°C Resolution
  - Supports up to 2.2nF filter capacitor
  - Anti-parallel diodes for extra diode support and compact design
- Internal Temperature Monitor
  - ±2°C accuracy
- 3.3V Supply Voltage
- Available in a 16-pin 4mm x 4mm QFN RoHS Compliant package
- Programmable temperature limits for $\overline{\text{ALERT}}$

Block Diagram



ORDER NUMBERS:

ORDERING NUMBER	PACKAGE	FEATURES	DIODE MODES SUPPORTED	SMBUS ADDRESS
EMC1428-1-AP-TR	16-pin QFN (RoHS Compliant)	Up to 7 external diodes. “Hottest Of” temperature comparison. Hardware set Critical / Thermal shutdown, ALERT output	Intel CPU and 3904	1001_100(r/w)
EMC1428-6-AP-TR	16-pin QFN (RoHS Compliant)	Up to 7 external diodes. “Hottest Of” temperature comparison. Hardware set Critical / Thermal shutdown, ALERT output	Intel CPU and 3904	1001_101(r/w)
EMC1428-7-AP-TR-CB7	16-pin QFN (RoHS Compliant)	Up to 7 external diodes. “Hottest Of” temperature comparison. Hardware set Critical / Thermal shutdown, ALERT output	Intel CPU and 3904	Selected by pull-up resistor on SYS_SHDN pin

Reel Size is 4,000 pieces

This product meets the halogen maximum concentration values per IEC61249-2-21

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Chapter 1 Pin Description

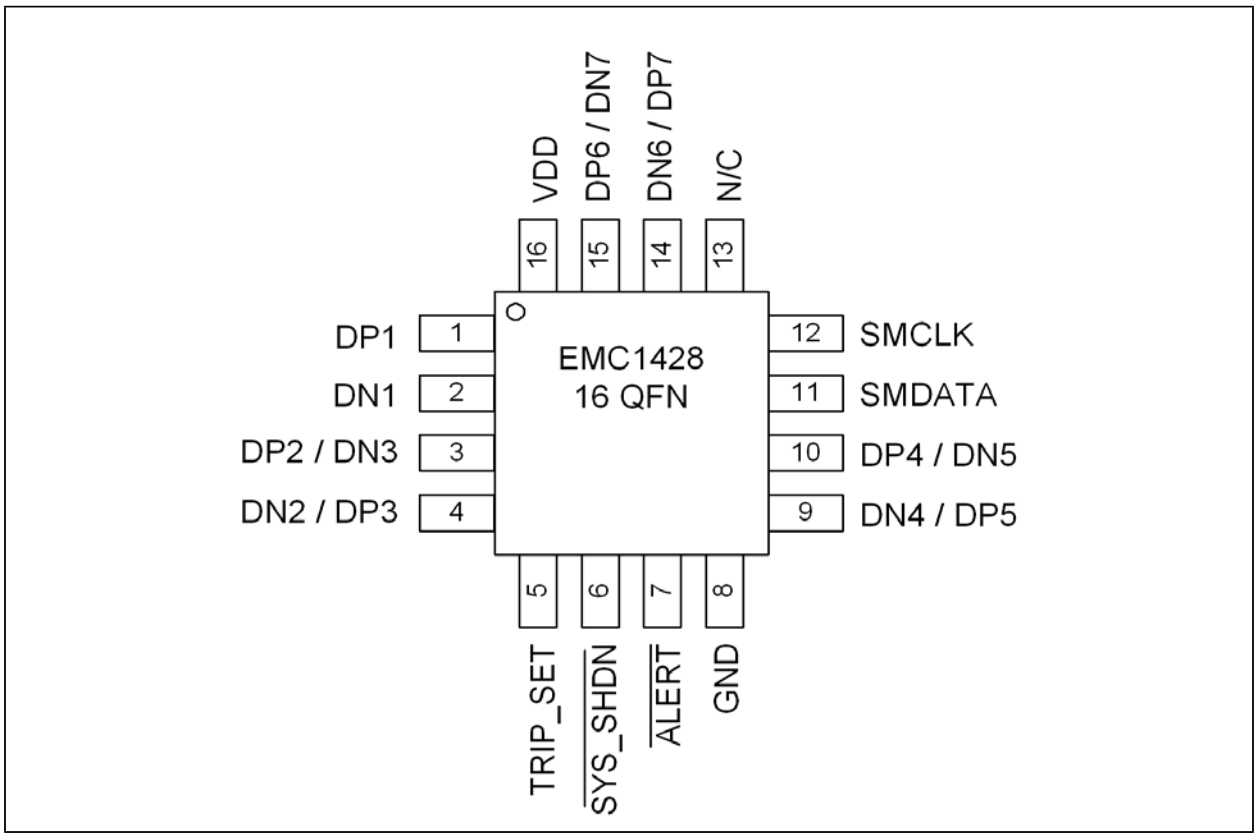

Figure 1.1 EMC1428 Pin Diagram

Table 1.1 EMC1428 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	DP1	DP1 - External Diode 1 positive (anode) connection.	AIO
2	DN1	External Diode 1 negative (cathode) connection.	AIO
3	DP2 / DN3	External Diode 2 positive (anode) connection and External Diode 3 negative (cathode) connection	AIO
4	DN2 / DP3	External diode 2 negative (cathode) connection and External Diode 3 positive (anode) connection	AIO
5	TRIP_SET	Voltage input to set Critical / Thermal Shutdown temperature	AIO

Table 1.1 EMC1428 Pin Description (continued)

PIN NUMBER	NAME	FUNCTION	TYPE
6	$\overline{\text{SYS\_SHDN}}$	Active low System Shutdown output signal - requires pull-up resistor EMC1428-7 - The pull-up resistor is used to determine SMBus address	OD (5V)
7	$\overline{\text{ALERT}}$	Active low interrupt - requires pull-up resistor	OD (5V)
8	GND	Ground Connection	Power
9	DN4 / DP5	External diode 4 negative (cathode) connection and External Diode 5 positive (anode) connection	AIO
10	DP4 / DN5	External Diode 4 positive (anode) connection and External Diode 5 negative (cathode) connection	AIO
11	SMDATA	SMBus Data input/output - requires pull-up resistor	DIOD (5V)
12	SMCLK	SMBus Clock input - requires pull-up resistor	DI (5V)
13	N/C	Not used - connect to Ground - see EMC1428 Anomaly Sheet	n/a
14	DN6 / DP7	External diode 6 negative (cathode) connection and External Diode 7 positive (anode) connection	AIO
15	DP6 / DN7	External Diode 6 positive (anode) connection and External Diode 7 negative (cathode) connection	AIO
16	VDD	Power supply	Power

The pin types are described below. All pins labelled (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

Table 1.2 Pin Type

PIN TYPE	FUNCTION
Power	Used to supply either VDD or GND to the device
DI	5V tolerant digital input
OD	5V tolerant Open drain digital output. Requires a pull-up resistor
DIOD	5V tolerant bi-directional digital input / open-drain output. Requires a pull-up resistor.
AIO	Analog input / output used for external diodes or analog inputs

Chapter 2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_pin} - V_{DD}\|$) (see Note 2.1)	-0.3 to 3.6	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for QFN-16		
Thermal Resistance (θ_{j-a})	50	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 2.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered.

2.2 Electrical Specifications

Table 2.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Supply Current	I_{DD}		450	600	uA	1 conversion / sec, dynamic averaging disabled
Supply Current	I_{DD}		900	1200	uA	4 conversions / sec, dynamic averaging enabled
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	0°C < T_A < 100°C
				±2	°C	-40°C < T_A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+40°C < T_{DIODE} < +110°C 0°C < T_A < 110°C
			±0.5	±2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Conversion Time all Channels	t_{CONV}		190		ms	default settings
Capacitive Filter	C_{FILTER}		2.2	2.7	nF	Connected across external diode
Resistance Error Correction	R_{SERIES}			100	Ω	In series with DP and DN lines
TRIP_SET Measurement						
Decoded Temperature Accuracy	T_{SET}			0.5	°C	R_{SET} = 1% resistor (see Note 2.2)
$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK} = 8mA
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V
Power Up Timing						
First conversion ready	t_{CONV_f}			300	ms	Time after power up before all channels updated with valid data
SMBus delay	t_{SMB_d}			15	ms	Delay before SMBus communications should be sent by host

Note 2.2 If a 1% resistor is used for RSET, then it is guaranteed to decode as shown in Table 4.1.

2.3 SMBus Electrical Characteristics

Table 2.3 SMBus Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0		V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3		0.8	V	5V Tolerant
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered or unpowered T_A < 85°C
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current	I_{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns f_{SMB} > 100kHz
Clock/Data Rise time	t_{RISE}			1000	ns	Min = 20+0.1C_{LOAD} ns f_{SMB} ≤ 100kHz
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 3 System Management Bus Interface Protocol

3.1 System Management Bus Interface Protocol

The EMC1428 communicate with a host controller, such as a Microchip SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1.

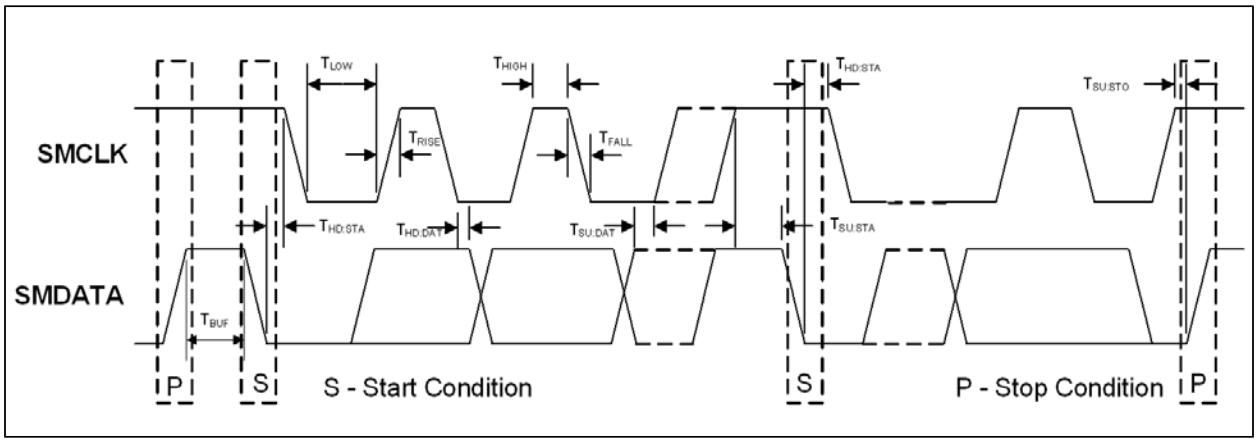

Figure 3.1 SMBus Timing Diagram

The EMC1428 are SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 3.1.

Table 3.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST

Attempting to communicate with the EMC1428 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

3.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 3.2:

Table 3.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	1001_100	0	0	XXh	0	XXh	0	0 -> 1

3.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.3.

Table 3.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1-> 0	1001_100	0	0	XXh	0	0 -> 1	1001_100	1	0	XXh	1	0 -> 1

3.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.4.

Table 3.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	1001_100	0	0	XXh	0	1 -> 0

3.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.5.

Table 3.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	1001_100	1	0	XXh	1	1 -> 0

3.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 000_1100b. All devices with active interrupts will respond with their client address as shown in Table 3.6.

Table 3.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	1001_1000	1	1 -> 0

The EMC1428 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

APPLICATION NOTE: The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

3.7 SMBus Address

The EMC1428-1 devices respond to the 7-bit slave address 1001_100xb.

The EMC1428-6 will respond to the 7-bit slave address 1001_101xb.

The EMC1428-7 slave address is determined at power up via the pull-up resistor on the $\overline{\text{SYS\_SHDN}}$ pin as shown in Table 3.7.

Table 3.7 Address Select Decode on $\overline{\text{SYS\_SHDN}}$ Pin

PULL UP RESISTOR	SMBUS ADDRESS
4.7k Ohm ±5%	1001_000xb
6.8k Ohm ±5%	1001_001xb
10k Ohm ±5%	1001_010xb
15k Ohm ±5%	1001_011xb
22k Ohm ±5%	1001_100xb
33k Ohm ±5%	1001_101xb

Note: Other addresses are available. Contact Microchip for more information.

3.8 SMBus Timeout

The EMC1428 support SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (see Section 5.14).

Chapter 4 Product Description

The EMC1428 is an SMBus temperature sensor with Hardware Critical / Thermal Shutdown support. The EMC1428 monitors up to seven (7) external diodes and one internal diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1428 and using that data to control the speed of one or more fans.

The EMC1428 device has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when measured temperatures meet or exceed user programmable limits. This allows the EMC1428 to be used as an independent thermal watchdog to warn the host of temperature hot spots without constant monitoring by the host.

The second level of monitoring asserts the $\overline{\text{SYS\_SHDN}}$ pin when the External Diode 1 temperature meets or exceeds a hardware specified threshold temperature. Additionally, any of the external diode channels can be configured to assert the $\overline{\text{SYS\_SHDN}}$ pin when the measured temperature meets or exceeds user programmable limits.

Because the EMC1428 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available devices without resistance error correction. As well, the automatic beta detection feature means that there is no need to program the device according to which type of diode is present. Therefore, the device can power up ready to operate for any system configuration including those diodes that require the BJT or transistor model.

Figure 4.1 shows a system level block diagram of the EMC1428.

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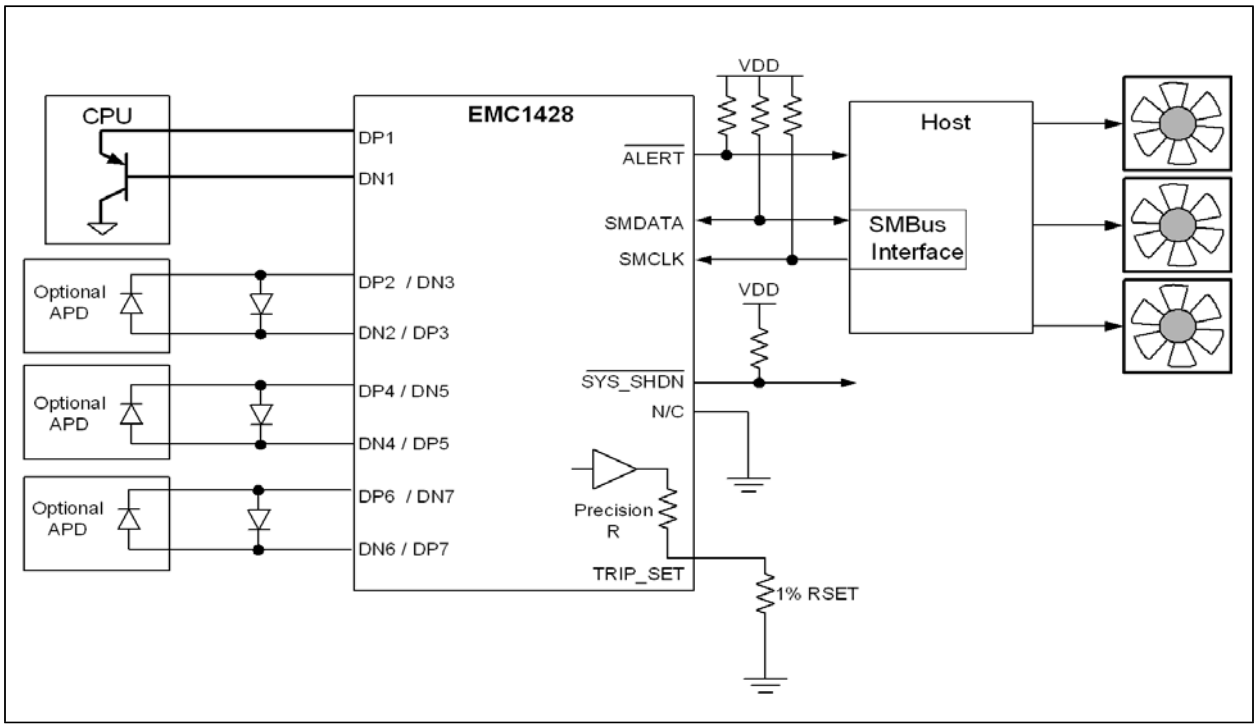

Figure 4.1 System Diagram for EMC1428

4.1 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open drain output and has two modes of operation: interrupt mode and comparator Mode. The mode of the $\overline{\text{ALERT}}$ output is selected via the ALERT / COMP bit in the Configuration Register.

4.1.1 $\overline{\text{ALERT}}$ Pin Interrupt Mode

When configured to operate in interrupt mode, the $\overline{\text{ALERT}}$ pin asserts low when an out of limit measurement ($\geq$ high limit or < low limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared. Each channel is subject to the fault queue (see Section 5.14).

The $\overline{\text{ALERT}}$ pin can be masked by setting the MASK bit. Once the $\overline{\text{ALERT}}$ pin has been masked, it will be de-asserted and remain de-asserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the Status Register normally.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more $\overline{\text{ALERT}}$ outputs can be hard-wired together.

4.1.2 $\overline{\text{ALERT}}$ Pin Comparator Mode

When the $\overline{\text{ALERT}}$ pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures meets or exceeds the respective high limit or drops below the respective low limit. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the $\overline{\text{ALERT}}$ pin is asserted in comparator mode, the corresponding status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. Once the $\overline{\text{ALERT}}$ pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the $\overline{\text{ALERT}}$ pin in this mode, however the individual channel masks (see Section 5.13) will prevent the respective channel from asserting the $\overline{\text{ALERT}}$ pin. In addition, each channel is subject to the fault queue (see Section 5.14).

4.2 $\overline{\text{SYS\_SHDN}}$ Output

The $\overline{\text{SYS\_SHDN}}$ output is asserted independently of the $\overline{\text{ALERT}}$ output and cannot be masked. If the External Diode 1 temperature exceeds the Hardware Critical / Thermal Shutdown Limit for the programmed number of consecutive measurements, then the $\overline{\text{SYS\_SHDN}}$ pin is asserted.

The Hardware Critical / Thermal Shutdown Limit is defined by the TRIP_SET pin as described in Section 4.3.

In addition to External Diode 1 channel triggering the $\overline{\text{SYS\_SHDN}}$ pin when the measured temperature exceeds to the Hardware Critical / Thermal Shutdown Limit, each of the temperature measurement channels can be configured to assert the $\overline{\text{SYS\_SHDN}}$ pin when they exceed the corresponding THERM Limit.

When the $\overline{\text{SYS\_SHDN}}$ pin is asserted, it will not release until the External Diode 1 temperature drops below the Hardware Thermal Shutdown Limit minus 10°C and all other measured temperatures drop below the THERM Limit minus the THERM Hysteresis value (when linked to $\overline{\text{SYS\_SHDN}}$).

The External Diode 1 channel and any software enabled channels are subject to the fault queue such that the error must exceed the threshold for one to four consecutive measurements before the $\overline{\text{SYS\_SHDN}}$ pin is asserted.

Figure 4.2 shows a block diagram of the interaction between the input channels and the $\overline{\text{SYS\_SHDN}}$ pin.

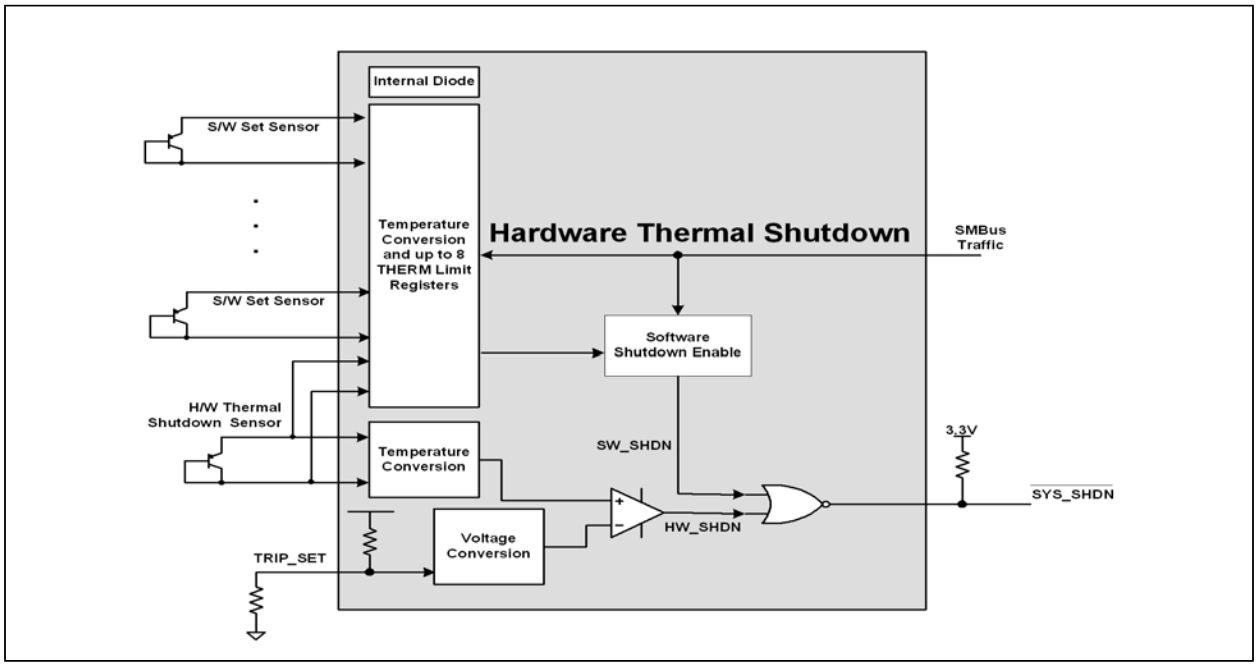

Figure 4.2 Block Diagram of Hardware Thermal Shutdown

4.3 TRIP_SET Pin

The EMC1428's TRIP_SET pin is an input to the Critical / Thermal Shutdown logic block which sets the Critical / Thermal shutdown temperature. The system designer creates a voltage level at this input through a simple resistor connected to GND as shown in Figure 4.3. The value of this resistor is used to create an input voltage on the TRIP_SET pin which is translated into a temperature ranging from 65°C to 127°C as enumerated in Table 4.1.

APPLICATION NOTE: Current only flows when the TRIP_SET pin is being monitored. At all other times, the internal reference voltage is removed and the TRIP_SET pin will be pulled down to ground.

APPLICATION NOTE: The TRIP_SET pin circuitry is designed to use a 1% resistor externally. Using a 1% resistor will result in the Thermal / Critical Shutdown temperature being decoded correctly. If a 5% resistor is used, then the Thermal / Critical Shutdown temperature may be decoded with as much as ±1°C error.

APPLICATION NOTE: Note that an open condition on the TRIP_SET pin will be decoded as a minimum temperature threshold level.

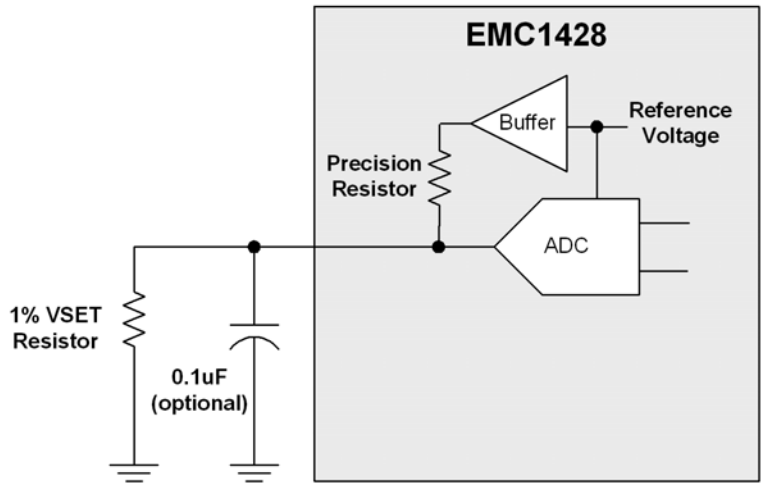

Figure 4.3 Vset Circuit

Table 4.1 V_{TRIP} Resistor Settings

TEMP (°C)	RSET (Ω)	TEMP (°C)	RSET (Ω)
65	0.0	97	1240.0
66	28.7	98	1330.0
67	48.7	99	1400.0
68	69.8	100	1500.0
69	90.9	101	1580.0
70	113.0	102	1690.0
71	137.0	103	1820.0
72	158.0	104	1960.0
73	182.0	105	2050.0
74	210.0	106	2210.0
75	237.0	107	2370.0
76	261.0	108	2550.0
77	294.0	108	2740.0
78	324.0	110	2940.0
79	348.0	111	3160.0
80	383.0	112	3480.0

Table 4.1 V_{TRIP} Resistor Settings (continued)

TEMP (°C)	RSET (Ω)	TEMP (°C)	RSET (Ω)
81	412.0	113	3740.0
82	453.0	114	4120.0
83	487.0	115	4530.0
84	523.0	116	4990.0
85	562.0	117	5490.0
86	604.0	118	6040.0
87	649.0	119	6810.0
88	698.0	120	7870.0
89	750.0	121	9090.0
90	787.0	122	10700.0
91	845.0	123	12700.0
92	909.0	124	15800.0
93	953.0	125	20500.0
94	1020.0	126	29400.0
95	1100.0	127	49900.0
96	1150.0	65	Open

4.4 Consecutive Alerts

The EMC1428 contains multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{SYS\_SHDN}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the interrupt conditions (High, Low, Diode fault). All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding status bit is set or pin is asserted.

See Section 5.14 for more details on the consecutive alert function.

4.5 Temperature Monitoring

The EMC1428 can monitor the temperature of up to seven (7) externally connected diodes as well as the internal or ambient temperature. Each channel is configured with the following features enabled or disabled based on user settings and system requirements.

APPLICATION NOTE: When measuring a 45nm CPU diode, the reported temperature has an error of approximately +1.5C at 100°C. This error is related to non-perfect ideality in the CPU diode.

4.5.1 Resistance Error Correction

The EMC1428 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of series resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC1428 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

4.5.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. Compensating for this error is also known as implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC1428 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

4.5.3 Digital Averaging

To reduce the effect of noise and temperature spikes on the reported temperature, all of the external diode channels use digital averaging. This averaging acts as a running average using the previous four measured values.

The default setting is to have digital averaging disabled for all channels. It can be enabled for each channel individually by the Filter Control Register (see Section 5.24).

4.5.4 “Hottest Of” Comparison

At the end of every measurement cycle, the EMC1428 compares all of the user selectable External Diode channels to determine which of these channels is reporting the hottest temperature. The hottest temperature is stored in the Hottest Temperature Registers and the appropriate status bit in the Hottest Status Register is set. As an optional feature, the EMC1428 can also flag an event if the hottest temperature channel changes. For example, suppose that External Diode channels 1, 3, and 4 are programmed to be compared in the “Hottest Of” Comparison. If the External Diode 1 channel reports the hottest temperature of the three, its temperature is copied into the Hottest Temperature Registers (in addition to the External Diode 1 Temperature registers) and it is flagged in the Hottest Status bit. If, on the next measurement, the External Diode 3 channel temperature has increased such that it is now the hottest temperature, the EMC1428 can flag this event as an interrupt condition and assert the $\overline{\text{ALERT}}$ pin.

4.5.5 Conversion Rates

The EMC1428 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 5.5. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 5.7.

4.5.6 Dynamic Averaging

Dynamic averaging causes the EMC1428 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 5.5). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 4x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 4.2 for EMC1428.

Table 4.2 Supply Current vs. Conversion Rate for EMC1428

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	DYNAMIC AVERAGING ENABLED (DEFAULT)	DYNAMIC AVERAGING DISABLED	DYNAMIC AVERAGING ENABLED (DEFAULT)	DYNAMIC AVERAGING DISABLED
1 / sec	715uA	450uA	4x	1x
2 / sec	750uA	550uA	2x	1x
4 / sec (default)	900uA	815uA	1x	1x
Continuous (see Table 5.8)	950uA	950uA	0.5x	0.5x

4.6 Diode Connections

The diode connection for the External Diode 1 channel is determined based on the selected device. For the EMC1428, this channel can support a diode-connected transistor (such as a 2N3904) or a substrate transistor (such as those found in an CPU or GPU) as shown in Figure 4.4. Anti-parallel diodes are not supported on the External Diode 1 channel.

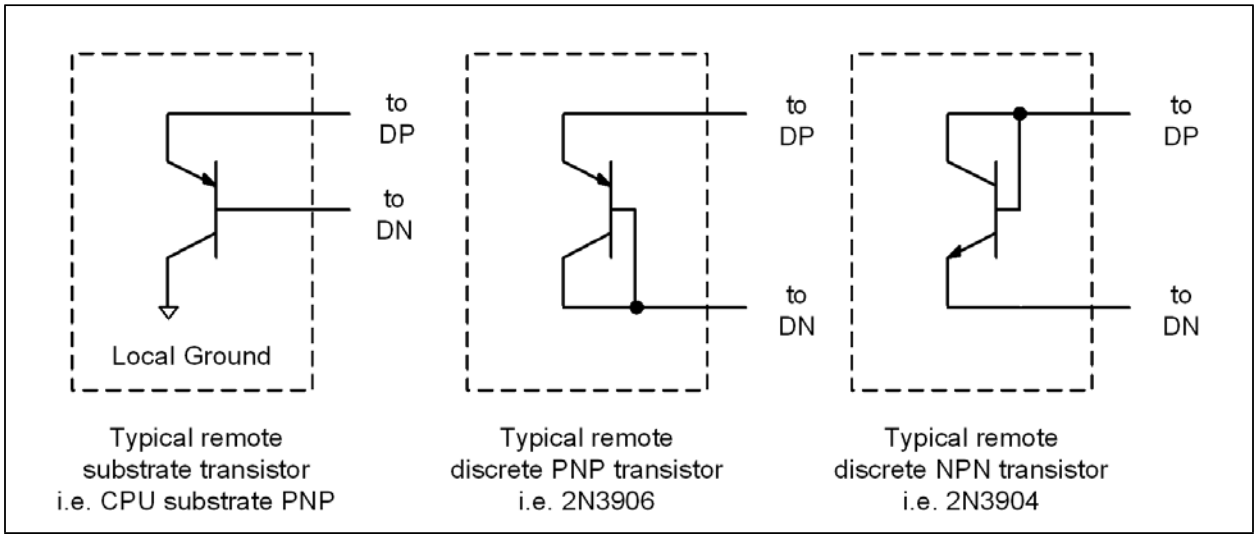

Figure 4.4 Diode Connections

4.6.1 Diode Faults

The EMC1428 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register. When an external diode channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions, however a short condition will be shared between the APD channels.

Chapter 5 Register Description

The registers shown in Table 5.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 28
01h	R	External Diode 1 Data High Byte	Stores the integer data for the External Diode 1	00h	Page 28
02h	R-C	Status	Stores the status bits for the Internal Diode and External Diodes	00h	Page 30
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 30
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 31
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 32
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	Page 32
07h	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 0Dh)	55h (85°C)	Page 32
08h	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 0Eh)	00h (0°C)	Page 32
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 30
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 31
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 32
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)	Page 32

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Dh	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 07h)	55h (85°C)	Page 32
0Eh	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 08h)	00h (0°C)	Page 32
10h	R	External Diode 1 Data Low Byte	Stores the fractional data for the External Diode 1	00h	Page 28
13h	R/W	External Diode 1 High Limit Low Byte	Stores the fractional portion of the high limit for the External Diode 1	00h	Page 32
14h	R/W	External Diode 1 Low Limit Low Byte	Stores the fractional portion of the low limit for the External Diode 1	00h	Page 32
15h	R/W	External Diode 2 High Limit High Byte	Stores the integer portion of the high limit for External Diode 2	55h (85°C)	Page 32
16h	R/W	External Diode 2 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 2	00h (0°C)	Page 32
17h	R/W	External Diode 2 High Limit Low Byte	Stores the fractional portion of the high limit External Diode 2	00h	Page 32
18h	R/W	External Diode 2 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 2	00h	Page 32
19h	R/W	External Diode 1 THERM Limit	Stores the 8-bit critical temperature limit for the External Diode 1	55h (85°C)	Page 35
1Ah	R/W	External Diode 2 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 2	55h (85°C)	Page 35
1Bh	R-C	External Diode Fault	Stores status bits indicating which external diode detected a diode fault	00h	Page 36
1Ch	R	TRIP_SET Voltage	Voltage measured on the TRIP_SET pin to determine the Critical / Thermal shutdown threshold	00h	Page 36
1Dh	R/W	SYS_SHDN Configuration	Controls which software channels, if any, are linked to the SYS_SHDN pin	00h	Page 36
1Eh	R	Hardware Thermal Shutdown Limit	When read, returns the selected Hardware Thermal Shutdown Limit	N/A	Page 37
1Fh	R/W	Interrupt Mask Register	Controls the masking of individual channels	F0h	Page 37
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (85°C)	Page 35

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	Page 35
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before the status bit is asserted	70h	Page 38
23h	R	External Diode 2 Data High Byte	Stores the integer data for External Diode 2	00h	Page 28
24h	R	External Diode 2 Data Low Byte	Stores the fractional data for External Diode 2	00h	Page 28
25h	R	External Diode 1 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 1	08h	Page 40
26h	R/W	External Diode 2 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 2	08h	Page 40
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h	Page 28
2Ah	R	External Diode 3 High Byte	Stores the integer data for External Diode 3	00h	Page 28
2Bh	R	External Diode 3 Low Byte	Stores the fractional data for External Diode 3	00h	Page 28
2Ch	R/W	External Diode 3 High Limit High Byte	Stores the integer portion of the high limit for External Diode 3	55h (85°C)	Page 32
2Dh	R/W	External Diode 3 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 3	00h (0°C)	Page 32
2Eh	R/W	External Diode 3 High Limit Low Byte	Stores the fractional portion of the high limit for External Diode 3	00h	Page 32
2Fh	R/W	External Diode 3 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 3	00h	Page 32
30h	R/W	External Diode 3 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 3	55h (85°C)	Page 35
32h	R	Hottest Diode High Byte	Stores the integer data for the hottest temperature	00h	Page 41
33h	R	Hottest Diode Low Byte	Stores the fractional data for the hottest temperature	00h	Page 41
34h	R-C	Hottest Status	Status bits indicating which external diode is hottest	00h	Page 41
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 42
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 43