Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

MICROCHIP

EMC1501

Memory Module Temperature Sensor and Serial Presence Detect EEPROM

PRODUCT FEATURES

General Description

The EMC1501 is a combination temperature monitor and Serial Presence Detect (SPD) EEPROM compatible with the TSE2002av JEDEC Specification. It contains an internal temperature monitor as well as an integrated 2k bit EEPROM with two methods of software protection. This product is different from other devices in that it can operate at any of three voltage ranges (1.8V, 2.5V, or 3.3V). It provides accuracy beyond the JEDEC requirements and offers 1°C accuracy from 25°C to 100°C.

The low current consumption can be reduced using the software programmed shutdown mode. The EMC1501 contains programmable high, low, and critical temperature limits. Finally, the device EVENT pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

Applications

- Dual In-line Memory Modules (DIMMs)
- Desktop and Mobile Computers
- Telecom

Features

- Meets JEDEC Standard TSE2002av (JC-42.4) for Serial Presence Detect with Temperature Sensor
- Integrated 2k bit EEPROM
- Software EEPROM protection
  — Permanent and temporary software locks
- Event pin
- Internal Temperature Monitor
  — 1°C accuracy (25°C to 100°C)
- Programmable High, Low, and TCRIT Limits
- SMBus 2.0 and I^2C Compliant 2-wire interface
  — Supports Page Read and Write operations

Block Diagram
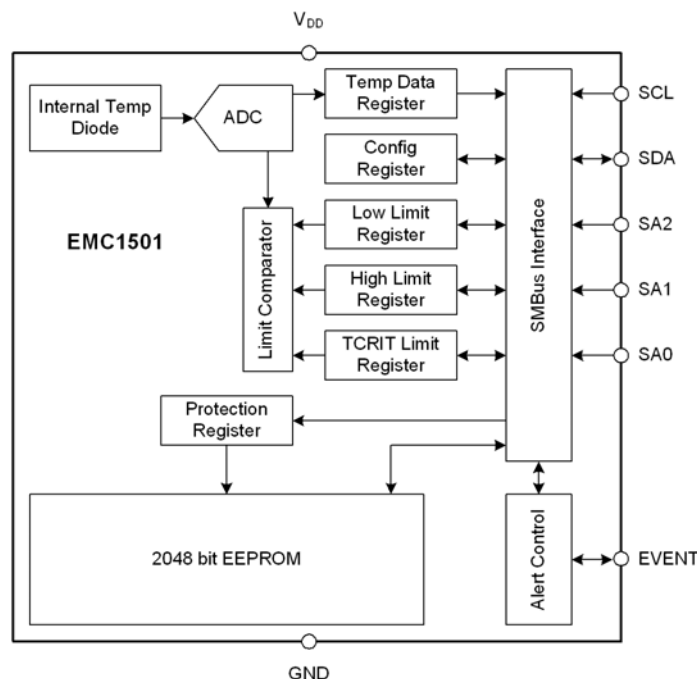
ORDERING INFORMATION:

ORDERING NUMBER	PACKAGE	FEATURES
EMC1501-1-AC3-TR	8 pin, TDFN 2mm x 3mm RoHS Compliant	Internal temperature sensor and 256 byte EEPROM with SW lock

REEL SIZE IS 5,000 PIECES

Table of Contents

Datasheet

List of Figures

List of Tables

Chapter 1 Pin Layout

Figure 1.1 Pin Diagram

Table 1.1 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	SA0	Address Selection Input - includes internal pull-down	DI (10V tolerant)
2	SA1	Address Selection Input - includes internal pull-down	DI
3	SA2	Address Selection Input - includes internal pull-down	DI
4	GND	Ground Connection	Power
5	SDA	SMBus Data Bi-directional Input - requires pull-up resistor to VDD	DIOD
6	SCL	SMBus Clock Input - requires pull-up resistor to VDD	DI
7	EVENT	Open Drain interrupt output - requires pull-up resistor	OD
8	VDD	Positive supply voltage	Power

Table 1.2 Pin Types

PIN TYPE	DESCRIPTION
DI	Digital Input
DIOD	Digital Input / Open Drain Output - This pin requires a pull-up resistor to VDD.
OD	Open Drain Output - This pin requires a pull-up resistor to VDD.
Power	This pin is used as a power supply input or ground.

Chapter 2 Electrical Specifications

Table 2.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.5 to 4.3	V
Voltage on EVENT pin (see Note 2.1)	-0.5 to VDD + 0.3	V
Voltage on SA0 pin	-0.5 to 10	V
Voltage on any other pin to GND (see Note 2.1)	-0.5 to VDD + 0.3	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for TDFN-8		
Thermal Resistance (θ_{j-a})	89	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 2.1 For those pins that have a pull-up resistor, the difference in voltage from V_{PULLUP} to V_{DD} must not exceed 3.6V.

2.1 Electrical Specifications

Table 2.2 Electrical Specifications

V_{DD} = 1.7V TO 3.6V T_A = -20°C TO 125°C, ALL TYPICAL VALUES AT T_A = 27°C UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
DC Power						
Supply Voltage - Low Range	V_{DD}	1.7	1.8	1.9	V	
Supply Voltage - Middle Range	V_{DD}	2.3	2.5	2.7	V	
Supply Voltage - High Range	V_{DD}	3.0	3.3	3.6	V	

Table 2.2 Electrical Specifications (continued)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V$_{DD}$ = 1.7V TO 3.6V T$_A$ = -20°C TO 125°C, ALL TYPICAL VALUES AT T$_A$ = 27°C UNLESS OTHERWISE NOTED.						
Supply Current	I$_{DD}$		500	1000	uA	8 conversion / sec, no EEPROM access
			20	100	uA	Standby mode (per JEDEC spec) Voltage on SA0 $\leq$ V$_{DD}$ 0°C < T$_A$ < 95°C
				2	mA	EEPROM write access at 100kHz Temperature Monitoring disabled Page Write at 20 Hz rate.
				2	mA	EEPROM read access at 100kHZ, Temperature Monitoring enabled
High Voltage Input	V$_{HV}$	7		10	V	V$_{HV}$ - V$_{DD}$ $\geq$ 4.8V
Internal Temperature Monitor						
Temperature Accuracy			±0.5	±1	°C	25°C < T$_A$ < 100°C (Active Range)
			±1	±2	°C	-20°C < T$_A$ < 125°C
Temperature Resolution			0.125		°C	
SA0, SA1, SA2 Pins						
Input Impedance	Zin	30			kOhm	V$_{IN}$ < 0.3 * V$_{DD}$
	Zin	800			kOhm	V$_{IN}$ > 0.7 * V$_{DD}$
Input Low Voltage	V$_{IL}$	-	-	0.3 * V$_{DD}$	V	
Input High Voltage	V$_{IH}$	0.7 * V$_{DD}$	-	-	V	
Input Leakage Current	I$_{IH}$ / I$_{IL}$			±5	uA	Powered or unpowered T$_A$ < 85°C, V$_{IN}$ = V$_{DD}$ or V$_{SS}$
EVENT, SDA, SCL pins						
Output Low Voltage	V$_{OL}$	0.4			V	I$_{SINK}$ = 2.1mA (2.3 < V$_{DD}$ $\leq$ 3.6V)
		0.2			V	I$_{SINK}$ = 700uA (1.7 < V$_{DD}$ $\leq$ 2.3V)
Input Low Voltage	V$_{IL}$	-	-	0.3 * V$_{DD}$	V	
Input High Voltage	V$_{IH}$	0.7 * V$_{DD}$	-	-	V	
Input Leakage Current	I$_{IH}$ / I$_{IL}$			±2	uA	Powered or unpowered T$_A$ < 85°C, V$_{IN}$ = V$_{DD}$ or V$_{SS}$
Output Leakage Current	I$_{OH}$ / I$_{OL}$			±2	uA	V$_{OUT}$ = V$_{DD}$ or V$_{SS}$
Input Capacitance	C$_{IN}$		5		pF	

Table 2.2 Electrical Specifications (continued)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD} = 1.7V TO 3.6V T_A = -20°C TO 125°C, ALL TYPICAL VALUES AT T_A = 27°C UNLESS OTHERWISE NOTED.						
EEPROM						
Sector Endurance	N_{END}	10000			cycles	
Data Retention	t_{DR}	100			yrs	
Read Time	t_{READ}		1.5		us	
Program Time	t_{WRITE}			9	ms	

Table 2.3 SMBus Timing Specifications

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD} = 1.7V to 3.6V, T_A = -20°C - 125°C, Typical values are at T_A = 27°C unless otherwise noted						
Clock Frequency	f_{SMB}	10		400	kHz	$V_{DD} > 2.3V$
		10		100	kHz	$V_{DD} \leq 2.3V$
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 3 Communications

3.1   System Management Bus Interface Protocol

The EMC1501 communicates with a host controller through the SMBus which is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the EMC1501 will not stretch the clock signal.
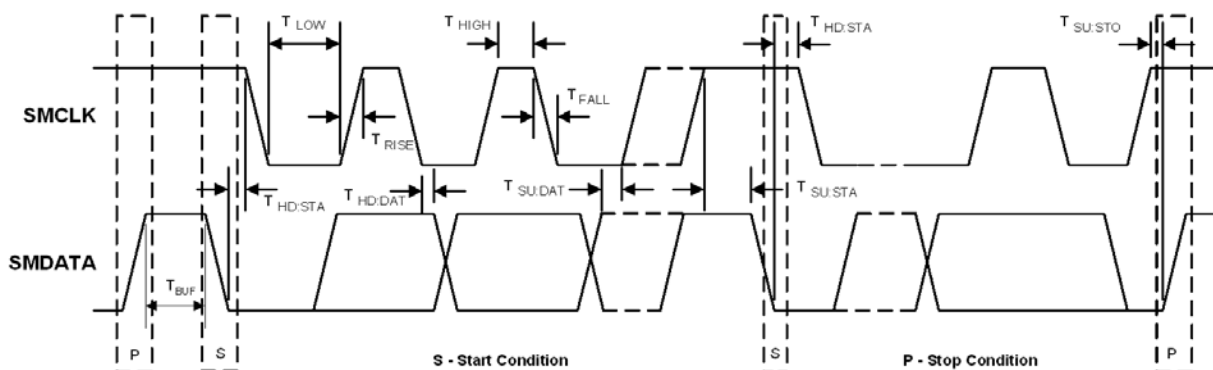
Figure 3.1 SMBus Timing Diagram

The EMC1501 is SMBus 2.0 compatible and supports the Read Byte, Write Byte, Page Read, and Page Write protocols as shown below.

3.1.1   SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

3.1.2   SMBus Address and RD / $\overline{\text{WR}}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD / $\overline{\text{WR}}$ indicator bit. If this RD / $\overline{\text{WR}}$ bit is a logic '0', the SMBus Host is writing data to the client device. If this RD / $\overline{\text{WR}}$ bit is a logic '1', the SMBus Host is reading data from the client device.

The EMC1501 contains three SMBus addresses. See Section 3.9 for details.

3.1.3   SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

Table 3.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

3.1.4   ACK and NACK Bits

The ACK bit is used to indicate that a data byte was received properly. The client will drive the SDA pin low (thus acknowledging that it received the data) after it receives the 8-bit Slave Address (7-bit Slave Address plus the read or write bit) and again after it receives the register address. If the host is trying to write data to a register that is locked, the client will hold the SDA pin high after it receives the data byte (a NACK or not acknowledge signal) and will ignore the data.

Attempting to write to any locked bytes will cause the device to send a NACK bit and ignore data. Attempting to write data beyond a page boundary will cause the device to send a NACK bit and ignore data.

Table 3.2 shows the ACK and NACK behavior of the accessing options for Write commands while Table 3.3 shows the ACK and NACK behavior of the accessing options for Read commands.

Note: *PSWP = Permanently Set Write Protection
SWP = Set Write Protection
CWP = Clear Write Protection

Table 3.2 Write Acknowledge Behavior

INSTRUCTION	STATUS	SLAVE ADDR		ADDR BYTE		DATA BYTE	
		DATA	ACK	DATA	ACK	DATA	ACK
Write PSWP*	Not Locked or locked w/ SWP	0110_XXX0	ACK	Don't Care	ACK	Don't Care	ACK
	Locked w/ PSWP	0110_XXX0	NACK	Don't Care	NACK	Don't Care	NACK
Write SWP*	Not Locked	0110_00H0	ACK	Don't Care	ACK	Don't Care	ACK
	Locked w/ SWP or PSWP	0110_00H0	NACK	Don't Care	NACK	Don't Care	NACK
Write CWP*	Not Locked or locked w/ PSWP	0110_01H0	NACK	Don't Care	NACK	Don't Care	NACK
	Locked w/ SWP	0110_01H0	ACK	Don't Care	ACK	Don't Care	ACK
Write EEPROM Data in lower 128 bytes	Not Locked	1010_XXX0	ACK	XXh	ACK	XXh	ACK (NACK if cross page boundary)
	Locked w/ SWP or PSWP	1010_XXX0	ACK	XXh	ACK	XXh	NACK
Write EEPROM Data in upper 128 bytes	n/a	1010_XXX0	ACK	XXh	ACK	XXh	ACK (NACK if cross page boundary)
Write Temperature Data	n/a	0011_XXX0	ACK	XXh	ACK	XXh	ACK

Table 3.3 Read Acknowledge Behavior

INSTRUCTION	STATUS	SLAVE ADDR		ADDR BYTE		REPEATED SLAVE ADDR	
		DATA	ACK	DATA	ACK	DATA	ACK
Read PSWP	Not Locked	0110_XXX0	ACK	Don't Care	ACK	0110_XXX1	NACK
	Locked w/ PSWP	0110_XXX0	NACK	Don't Care	NACK	0110_XXX1	NACK
	Locked w/ SWP	0110_XXX0	ACK	Don't Care	ACK	0110_XXX1	NACK
Read SWP	Not Locked	0110_00H0	ACK	Don't Care	ACK	0110_00H1	NACK
	Locked w/ PSWP	0010_00H0	NACK	Don't Care	NACK	0110_00H1	NACK
	Locked w/ SWP	0110_00H0	NACK	Don't Care	NACK	0110_00H1	NACK
Read CWP	Not Locked or locked w/ PSWP	0110_01H0	NACK	Don't Care	NACK	0110_01H1	NACK
	Locked w/ SWP	0110_01H0	ACK	Don't Care	ACK	0110_01H1	NACK
Read EEPROM Data	n/a	1010_XXX0	ACK	XXh	ACK	1010_XXX1	ACK
Read Temperature Data	n/a	0011_XXX0	ACK	XXh	ACK	0011_XXX1	ACK

APPLICATION NOTE: When reading the PSWP, SWP, or CWP, all bytes received will be NACK'd if the RD / $\overline{WR}$ bit is set to a logic '1' indicating a read.

3.1.5   SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC1501 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.1.6   SMBus Timeout

The EMC1501 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will timeout and reset the SMBus interface.

The timeout function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Configuration register (see Section 5.9).

3.1.7 SMBus and I²C Compliance

The major difference between SMBus and I²C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz. The I²C bus had no minimum frequency.

2. The client protocol will reset if the clock is held low longer than 30ms. The I²C bus may hold the clock low indefinitely.

3. The client protocol will reset if both the clock and the data line are high for longer than 150us (idle condition). The I²C bus is not required to reset except on a STOP bit.

4. The I²C Block Read and Write protocols do not use an additional data byte to indicate the number of data bytes that will be transmitted. Therefore, it may transmit as many bytes as desired provided that the bytes are ACK'd or NACK'd correctly. The EMC1501 only supports the I²C style block read and write.

3.2 Communications Protocols

The EMC1501 is SMBus 2.0 compatible and supports Read Byte and Write Byte as valid protocols as shown below. The EMC1501 also supports the I²C Page (Block) Read and Page (Block) Write protocols. The I²C Block Read and Block Write protocols, if used with two data bytes, function as a SMBus Word Read or Word Write protocols.

All of the below protocols use the convention in Table 3.1.

Table 3.4 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
Data sent	Data sent

3.2.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 3.5.

Table 3.5 Write Byte Protocol

START	CLIENT ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 ->0	0011_XXX	0	0	XXh	0	XXh	0	0 -> 1

3.2.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.6.

Table 3.6 Read Byte Protocol

START	CLIENT ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	CLIENT ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1->0	0011_XXX	0	0	XXh	0	1 ->0	0011_XXX	1	0	XXh	1	0 -> 1

3.3   Page Read

The Page Read protocol is used to read data from up to sixteen (16) consecutive registers. This protocol is an extension of the Read Byte and Receive Byte protocols. After a data byte is received by the host, instead of sending a NACK bit, the host sends and ACK bit prompting the client to send another data byte. So long as the host sends an ACK bit after the data byte, the client will continue to send data bytes.

Table 3.7 shows a partial example of the Block Read command starting with the Read Byte protocol while.

Table 3.7 Page Read Protocol

START	CLIENT ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	CLIENT ADDRESS	RD	ACK	REGISTER DATA
1->0	1010_XXX	0	0	XXh	0	1 ->0	0011_XXX	1	0	XXh

ACK	REGISTER DATA	ACK	REGISTER DATA	ACK	REGISTER DATA	ACK	. . .	REGISTER DATA	NACK	STOP
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

3.4   Page Write

The Page Write protocol is used to write data to sixteen (16) consecutive registers. This protocol is an extension of the Write Byte protocol and is partially shown in Table 3.8. After the host sends a data byte and the slave sends the ACK bit, the host will send additional data bytes, each followed by an ACK from the client. When the host has send the last data byte, it will send the stop bit normally and end the transaction.

The EMC1501 EEPROM contains 16 pages each consisting of 16 bytes. The device will roll over across page boundaries; however, it will NACK all data bytes received that are beyond the page boundary of the write and discard all received data. This will occur regardless of where within the page the write is originated.

Table 3.8 Page Write Protocol

START	CLIENT ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	1010_XXX	0	0	XXh	0	XXh	0

REGISTER DATA	ACK	REGISTER DATA	ACK	. . .	REGISTER DATA	ACK	STOP
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

3.5   EEPROM Write Cycle

When the host is communicating with the EEPROM Data Set and it sends the stop bit the EEPROM will undergo its internal write cycle. When this occurs, it cannot receive any more data until the write cycle is complete.

If the host has sent the stop bit, the EEPROM Data Set will not respond to its SMBus address until the write cycle is completed. Once the write cycle has been completed, the device will respond normally. If the host has not sent the stop bit, all subsequent data bytes will be ignored.

3.6 SMBus Addressing

The EMC1501 contains multiple functional SMBus addresses depending on the functionality that is being accessed as shown in Table 3.9. The device supports SMBus activity to access Temperature Monitor controls independently of EEPROM data and the SA2, SA1, and SA0 pins apply to both addresses simultaneously.

3.6.1 SWP and CWP Addresses

The SWP (Set Write Protection) and CWP (Clear Write Protection) Commands act as a non-volatile, non-permanent software lock. The SWP Command (Set Write Protection) is invoked by writing to SMBus Address 0110_001x while driving the SA0 pin to a high voltage state (V_{HV}). Once the SWP command has been set, the lower 128 bytes of data will be locked and cannot be accessed.

The CWP Command is used to clear the previous SWP Command. If no SWP Command has been sent, then this command will do nothing. The CWP Command is invoked by writing to SMBus Address 0110_011 while driving the SA0 pin to a high voltage state (V_{HV}).

When sending the SWP and CWP addresses, only one device can be accessed at a time.

APPLICATION NOTE: The SWP and CWP commands can only be sent when the SA0 pin is driven to a high voltage upon device power up. If it is driven to a high voltage after device power up, then it will not be detected and a PSWP command will be sent.

APPLICATION NOTE: The SWP and CWP commands do not require the SA2 and SA1 pins to be tied to '00' and '01' respectively. All that these commands require is that the SA0 pin be pulled to a high voltage upon device power up. However, the SMBus Master must still transmit the appropriate SMBus slave address to invoke these commands (0110_0010 for SWP command and 0110_0110 for CWP command).

3.6.2 Protection Register

The EERPOM data can be permanently "locked" by accessing the Protection Register. The Protection Register is accessed using SMBus address 0110_000xb through 0110_111xb (set by the SA2, SA1, and SA0 pins). Writing to the Protection Register will lock the lower 128 bytes of the EEPROM Data Set. This state is non-volatile and cannot be reversed. Attempting to write to the Protection Register when the device is "locked" will cause the EMC1501 to send a NACK bit in response to the slave address.

Reading from the Protection Register will not cause the data to be locked; however it will be NACK'd.

APPLICATION NOTE: The SWP and CWP commands require that the SA0 pin be at a high voltage during power up. However, if the SA2 and SA1 are not '00' or '01' then writing to the Protection register with SA0 at a high voltage will still invoke the PSWP command. If the SA2 and SA1 pins are at '00' or '01', writing to the Protection Register will invoke the SWP or CWP commands respectively.

Table 3.9 SMBus Addressing

FUNCTIONALITY ACCESSED	BASE ADDRESS	SA2	SA1	SA0	SMBUS ADDRESS
					BINARY
Temperature Monitor	0011b (3h)	VSS	VSS	VSS	0011_000x
		VSS	VSS	VDD	0011_001x
		VSS	VDD	VSS	0011_010x
		VSS	VDD	VDD	0011_011x
		VDD	VSS	VSS	0011_100x
		VDD	VSS	VDD	0011_101x
		VDD	VDD	VSS	0011_110x
		VDD	VDD	VDD	0011_111x
EEPROM Data	1010b (Ah)	VSS	VSS	VSS	1010_000x
		VSS	VSS	VDD	1010_001x
		VSS	VDD	VSS	1010_010x
		VSS	VDD	VDD	1010_011x
		VDD	VSS	VSS	1010_100x
		VDD	VSS	VDD	1010_101x
		VDD	VDD	VSS	1010_110x
		VDD	VDD	VDD	1010_111x
Protection Register (permanent)	0110b (6h)	SA2	SA1	SA0	0110_000x through 0110_111x
Protection Register (SWP)	0110b (6h)	VSS	VSS	VHV	0110_001x
Protection Register (CWP)	0110b (6h)	VSS	VDD	VHV	0110_011x

Chapter 4 General Description

The EMC1501 is a combination temperature monitor and Serial Presence Detect EEPROM compatible with the TSE2002av JEDEC Specification. It contains an internal temperature monitor as well as an integrated 2k bit EEPROM with two methods of software protection. This product is different from other devices in that it can operate at any of three voltage ranges (1.8V, 2.5V, or 3.3V). It provides accuracy beyond the JEDEC requirements and offers 1°C accuracy from 25°C to 100°C.

The EMC1501 EEPROM module contains 2048 bits of non-volatile memory that can be write protected. Both functions, EEPROM and temperature sensor, are controlled independently of each other via the 2-wire SMBus communications protocol. Each uses a different SMBus address so that cross communications are not possible.

A system diagram is shown in Figure 4.1.
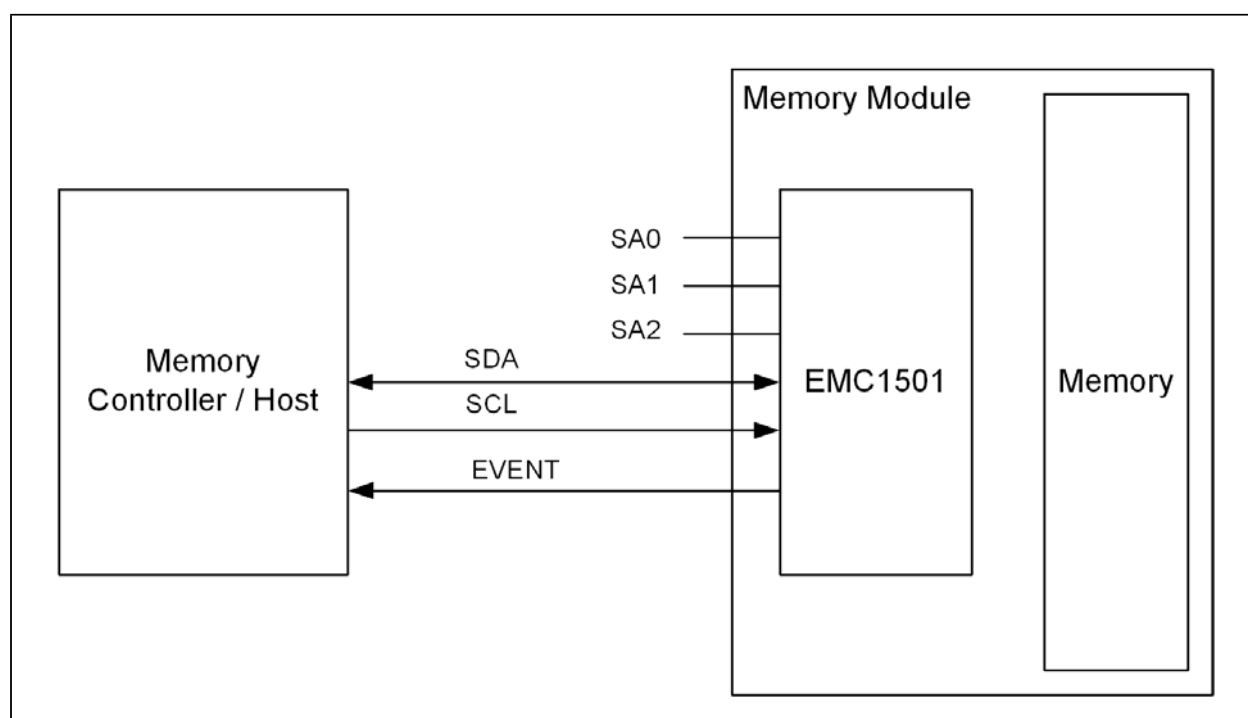
Figure 4.1 EMC1501 System Diagram

4.1   Power Modes

The EMC1501 contains three modes of operation. They are:

1. Full Power Mode - In this mode of operation, the device is monitoring temperature and the EEPROM block is being actively accessed.

2. Temperature Only - In this mode of operation, the device is monitoring temperature and the EEPROM block is not being accessed.

3. Standby - In this mode of operation, the device is not monitoring temperature data. Access to all register data and the EEPROM block is permitted. This mode is entered by setting the SHDN bit in the Configuration Register (see Section 5.2).

4.2 EVENT

The EVENT pin is an open-drain digital I/O. During normal operation, the pin acts as an open-drain interrupt output with programmable polarity. This pin is asserted to the "active" state as set by the EVENT_POL bit in the Configuration Register (see Section 5.2) whenever the temperature crosses one of the programmed thresholds.

4.2.1 EVENT Modes

The EMC1501 EVENT pin has three operating states during normal operation. These states depend on user programmed settings as well as the out-of-limit conditions that are present.

1. Interrupt Mode - In this mode, the EVENT pin will remain asserted until the CLEAR bit in the Configuration Register is written (see Section 5.2). Once the pin is cleared by the host, it will remain cleared until a different interrupt condition is met. This mode is not used when the temperature is compared against the TCRIT limit (see Section 5.5).

2. Comparator Mode - In this mode, the EVENT pin will clear itself when the error condition that caused the pin to be asserted is removed. When configured in Comparator Mode, the CLEAR bit is ignored. When the temperature is compared against the TCRIT limit, this mode is always used. This is the default operating mode.

APPLICATION NOTE: If the EVENT pin operating state is changed from Comparator Mode to Interrupt Mode while the measured temperature is above the high limit or below the low limit, then the EVENT pin will be released immediately regardless of whether the CLEAR bit has been written or not.

APPLICATION NOTE: If the EVENT pin operating state is changed from Interrupt Mode to Comparator Mode while the measured temperature is above the high limit or below the low limit, then the EVENT pin will be released immediately.

3. TCRIT Only Mode - In this mode, the EVENT pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis.
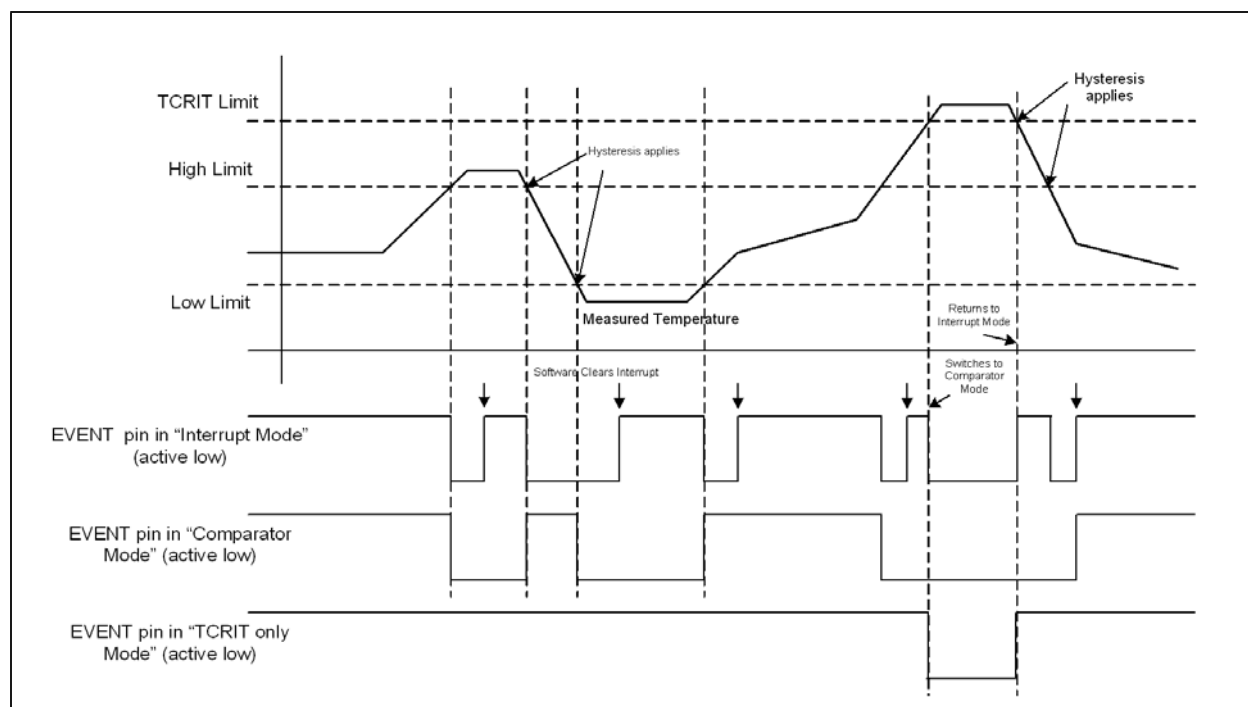
Figure 4.2 shows the three interrupt modes.

Figure 4.2 EVENT Modes

4.3   Serial Presence Detection

The EMC1501 Serial Presence Detection functionality contains 2048 bits of user definable EEPROM memory that is used to identify the memory size, type, and special operating conditions of the Memory Module. This information is placed in the lower 128 bytes of EEPROM storage and can be protected from being written by future applications. The upper 128 bytes of EEPROM storage are available for scratch pad use by any application.

4.4   Serial Presence Detection Protection

There are three methods to protect the lower 128 bytes of data in the EEPROM. The first mechanism is a software programmed, non-permanent lock accessed via the register set. The second mechanism is a non-permanent lock initiated using the SWP Command. The third and final mechanism is a permanent lock initiated by writing to the Protection Register. These methods are not exclusive and multiple methods can be used simultaneously.

4.4.1   Locking using the SWP and CWP Commands

The EMC1501 supports a non-volatile, clearable software lock using the SWP and CWP Commands. When the SWP Command is issued, the lower 128 bytes of data in the EEPROM Data Set is locked and cannot be updated. This lock is only cleared using the CWP Command. See Section 3.6.1.

4.4.2   Locking via Protection Register

The EMC1501 EEPROM data can be locked via software by writing to the Protection Register. Any write to the Protection Register (accessed at base address 0110), regardless of the data written, will

lock the lower 128 bytes of the EEPROM data set. This data lock is permanent and cannot be reversed.

4.5 Temperature Monitor

The EMC1501 contains an internal temperature monitor. This temperature monitor measures the ambient die temperature of the device and updates the data registers. In addition, it compares this temperature against user-programmed limits to flag out-of-limit conditions or critical temperature conditions.

The EMC1501 updates the temperature data at a fixed update rate of 8 measurements per second.

4.5.1 Temperature Limits

The EMC1501 contains three user programmable temperature limits each with hysteresis.

The High and Low Limits are used to form an operating window. Whenever the temperature measurement crosses the threshold of this window (either on the high or low side), the EVENT pin is asserted. When configured in Interrupt Mode, the pin will remain asserted until it is cleared by the host. If configured in Comparator Mode, the pin will be released when the temperature returns to within the programmed window.

The TCRIT Limit is used to used as an absolute temperature limit. Whenever the temperature measurement crosses the TCRIT Limit, the EVENT pin will be asserted and remain asserted until the temperature drops below the limit minus hysteresis.

APPLICATION NOTE: The hysteresis applies for all of the temperature limits in the same direction. This means that an interrupt condition is generated when the temperature drops below the respective limit minus the hysteresis or meets or exceeds the respective limit.

4.5.2 Temperature Data Format

The EMC1501 reports data in a range from -64°C to +191.875°C with 0.125°C resolution. The format is standard 2's complement format as shown in Table 4.1.

Table 4.1 Temperature Data Format

TEMPERATURE (C)	DATA	
	HEX	BINARY
≤ -64	1C_00h	xxx1 1100 0000 000xb
-63.75	1C_04x	xxx1 1100 0000 010xb
-1	1F_F0h	xxx1 1111 1111 000xb
-0.75	1F_F4h	xxx1 1111 1111 010xb
-0.5	1F_F8h	xxx1 1111 1111 100xb
-0.25	1F_FCh	xxx1 1111 1111 110xb
-0.125	1F_FEh	xxx1 1111 1111 111xb
0	00_00h	xxx0 0000 0000 000xb
0.125	00_02h	xxx0 0000 0000 001xb
0.25	00_04h	xxx0 0000 0000 010xb

Table 4.1 Temperature Data Format (continued)

TEMPERATURE (C)	DATA	
	HEX	BINARY
0.5	00_08h	xxx0 0000 0000 100xb
0.75	00_0Ch	xxx0 0000 0000 110xb
1	00_10h	xxx0 0000 0001 000xb
64	04_00h	xxx0 0100 0000 000xb
128	08_00h	xxx0 1000 0000 000xb
191	0B_F0h	xxx0 1011 1111 000xb
≥ 191.875	0B_FEh	xxx0 1011 1111 111xb

Chapter 5 Temperature Registers

The EMC1501 contains two independent register sets: Temperature and EEPROM Data Set. The Temperature Register Set is accessed via SMBus address 0011_000xb through 0011_111xb.

The Temperature Register Set stores the temperature data, limits, and configuration registers. All registers are 16-bit wide with the address pointing to the high byte. In order to read or write from the entire register, the block read and write commands must be used.

All other registers are 8-bits wide.

Table 5.1 Temperature Register Set

ADDR	R/W	NAME	FUNCTION	DEFAULT	PAGE
00h	R	Capabilities	Indicate the functions and capabilities of the temperature sensor	00_17h	pg 23
01h	R/W	Configuration	Controls the operation of the temperature monitor	00_00h	pg 25
02h	R/W	High Limit	Sets the High Limit	05_50h	pg 26
03h	R/W	Low Limit	Sets the Low Limit	00_00h	pg 27
04h	R/W	TCRIT Limit	Sets the critical temperature limit	05_A0h	pg 27
05h	R	Temperature Data	Stores the measured internal temperature	N/A	pg 27
06h	R	Manufacturer ID	Stores the pci-sig manufacturer ID	10_55h	pg 28
07h	R	Device / Revision ID	Stores the device ID and revision number of the device	08_42h	pg 28
09h	R/W	MCHP Configuration	Controls MCHP specific configuration bits	00_00h	pg 28
10h	W	One-Shot	Initiates an update of the temperature data when the device is in low power mode	00h	pg 29

5.1   Capabilities Register

Table 5.2 Capabilities Register

ADDR	R/W	NAME	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
00h	R	Capabilities	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	00_57h
			EVSD	TMOUT	0	TRES[1:0]		RANGE	ACC	EVENT	

The Capabilities Register indicates the capabilities of the temperature sensor.

Bits 15 - Bit 8 - RFU - Reserved for future use. These bits will always read '0' and writing to them will have no effect.

Bit 7 - EVSD - Indicates the behavior of the EVENT pin when the device is in Shutdown.

- '0' (default) - The EVENT pin retains its previous state when the device enters the Shutdown mode. It will remain in its previous state until the next temperature sample is measured at which point it will return to normal operation as determined by its operating mode and the measured temperature.

- '1' - The EVENT pin is deasserted when the device enters Shutdown. It will remain deasserted until the next temperature sample is measured at which point it will return to normal operation as determined by its operating mode and the measured temperature.

Bit 6 - TMOUT - Indicates the SMBus / I^2C timeout behavior supported. Timeout is supported in all modes of operation and for all modes of access (Temperature, EEPROM, or Locking).

- '0' - The timeout time varies from 10ms to 60ms.

- '1' (default) - The timeout time varies from 25ms to 35ms (SMBus compatible).

Bit 5 - '0' - This bit will return a logic '0'.

Bits 4 - 3 - TRES[1:0] - Indicates the resolution of the temperature monitor as shown in Table 5.3.

Table 5.3 TRES Bit Decode

TRES[1:0]		TEMPERATURE RESOLUTION
1	**0**	
0	0	0.5°C (9-bit)
0	1	0.25°C (10-bit)
1	0	0.125°C (11-bit) (default)
1	1	0.0625°C (12-bit)

Bit 2 - RANGE - Indicates the supported temperature range.

- '0' - The temperature monitor clamps values lower than 0°C.

- '1' (default) - The temperature monitor can read temperatures below 0°C and sets the sign bit appropriately.

Bit 1 - ACC - Indicates the supported temperature accuracy.

- '0' - The temperature monitor has ±2°C accuracy of the active range (25°C to 100°C) and 3°C accuracy over the entire operating range.

- '1' (default) - The temperature monitor has ±1°C accuracy over the active range (25°C to 100°C) and 2°C accuracy over the entire operating range.

Bit 0 - EVENT - Indicates whether the temperature monitor supports interrupt capabilities.

- '0' - The device does not support interrupt capabilities.

- '1' (default) - The device supports interrupt capabilities.

5.2   Configuration Register

Table 5.4 Configuration Register

ADDR	R/W	NAME	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
01h	R/W	Configuration	RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN	00_00h
			TCRIT_ LOCK	LIMIT_ LOCK	CLEAR	EVENT_ STS	EVENT_ CTRL	TCRIT_ ONLY	EVENT_ POL	EVENT_ MODE	

The Configuration Register holds the control and status bits of the EVENT pin as well as general hysteresis on all limits.

Bits 15 - 11 - RFU - Reserved for future use. These bits will always read '0' and writing to them will have no effect.

Bits 10 - 9 - HYST[1:0] - Control the hysteresis that is applied to all temperature limits as shown in Table 5.5. This hysteresis applies to the High and Tcrit temperature limits when the temperature is dropping below the threshold. Once the temperature is above the threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event.

The hysteresis applies to the low temperature limit so that the temperature must drop below the limit minus the hysteresis value before an interrupt event is flagged (and rise above the limit without the hysteresis).

The HYST[1:0] bits are locked if the TCRIT_LOCK bit has been set.

Table 5.5 HYST Bit Decode

HYST[1:0]		HYSTERESIS
1	**0**	**HYSTERESIS**
0	0	disable hysteresis (default)
0	1	1.5°C
1	0	3°C
1	1	6°C

Bit 8 - SHDN - Controls the power state of the temperature monitor. If either of the lock bits are set (bit 7 and bit 6), this bit cannot be set until they are unlocked. It can be cleared at any time.

- '0' (default) - The temperature monitor is active and converting.
- '1' - The temperature monitor is disabled and will not generate interrupts or update the temperature data.

Bit 7 - TCRIT_LOCK - Locks the TCRIT Limit Register from being updated.

- '0' (default) - The TCRIT Limit Register can be updated normally.
- '1' - The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset. The HYST[1:0] bits are likewise locked and cannot be updated.

Bit 6 - LIMIT_LOCK - Locks the High and Low Limit Registers from being updated.

- '0' (default) - The High and Low Limit Registers can be updated normally.