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High-Side Current-Sense and Multiple 1°C Temperature Monitor

PRODUCT FEATURES

Datasheet

General Description

The EMC1704 is a combination high-side current sensing device with precision temperature measurement. It measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. It also measures the source voltage and uses these measured values to present a proportional power calculation. The EMC1704 contains additional bi-directional peak detection circuitry to flag instantaneous current spikes with programmable time duration and magnitude threshold. Finally, the EMC1704 includes up to three (3) external diode channels and an internal temperature sensor for temperature measurement.

The temperature measurement includes advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm and 65nm processors), and automatic diode type detection.

Both current sensing and temperature monitoring include two tiers of protection: one that can be masked and causes the ALERT pin to be asserted, and the other that cannot be masked and causes the THERM pin to be asserted.

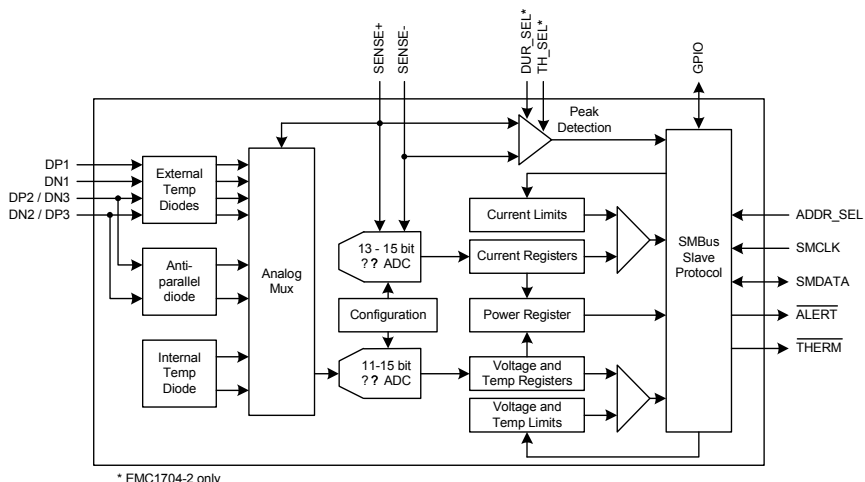
Applications

- Notebook and Desktop Computers
- Industrial
- Power Management Systems
- Embedded Applications

Features

- High-side current sensor
 - Bi-directional current measurement
 - Measures source voltage and indicates power ratio
 - 1% current measurement accuracy
 - Integrated over 82ms to 2.6sec with 11-bit resolution
 - 3V to 24V bus voltage range
- Independent hardware set instantaneous current peak detector (EMC1704-2 only)
 - Software controls to program time duration and magnitude threshold
- Power supply options
 - Bus or separately powered for low voltage operation
- Wide temperature operating range: -40°C to +85°C
- Up to three external temperature monitors
 - 1°C accuracy ($20^{\circ}\text{C} < T_{\text{DIODE}} < 110^{\circ}\text{C}$) with 0.125°C resolution
 - Ideality factor setting
 - Support for 45nm and 65nm CPU diodes requiring the BJT/transistor model w/ beta compensation
 - Determines external diode type and optimal settings
 - Resistance Error Correction
 - Anti-parallel diode support for additional diode options
- Internal temperature monitor
 - $\pm 1^{\circ}\text{C}$ accuracy ($-5^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
- ALERT and THERM outputs for temperature, voltage, and out-of-current limit reporting
- SMBus 2.0 interface
 - Pin-selectable SMBus Address
 - Block Read and Write
- General Purpose I/O
- Available in a RoHS Compliant Package: 14-pin SOIC (EMC1704-1) or 16-pin 4mm x 4mm QFN (EMC1704-2)

Block Diagram



Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES
EMC1704-1-YZT-TR	14-pin SOIC (Lead-free ROHS compliant)	Up to three external diodes, current sensor, software set peak detector
EMC1704-2-AP-TR	16-pin 4mm x 4mm QFN (Lead-free ROHS compliant)	Up to three external diodes, current sensor, hardware/software set peak detector

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smcs.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Pin Description

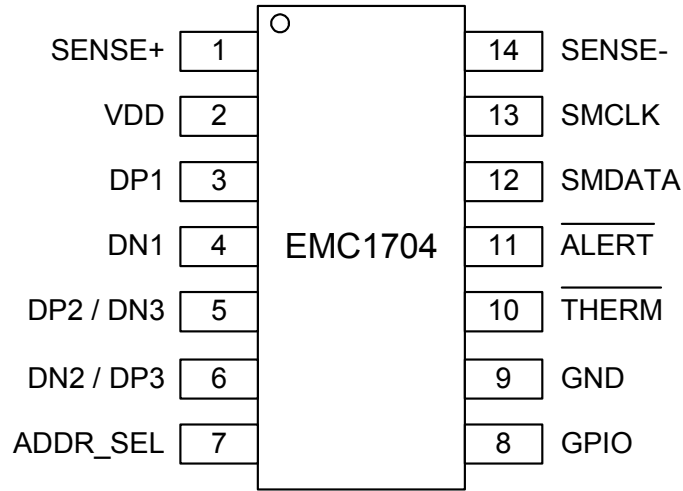


Figure 1.1 EMC1704-1 Pin Diagram 14-Pin SOIC

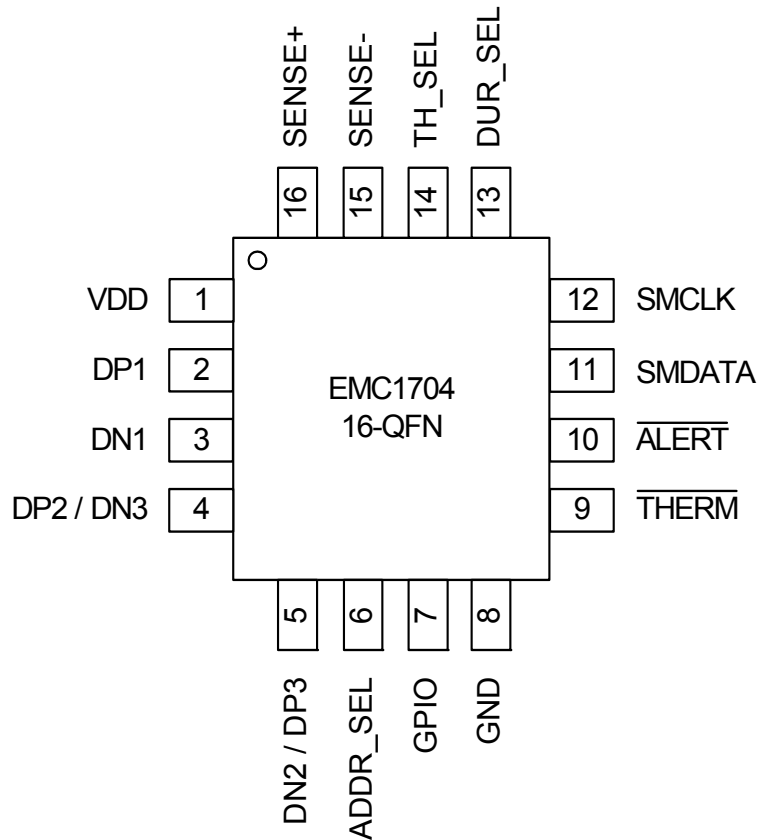


Figure 1.2 EMC1704-2 Pin Diagram 16-Pin QFN 4mm x 4mm

Table 1.1 Pin Description for EMC1704-X

PIN NUMBER EMC1704-1	PIN NUMBER EMC1704-2	PIN NAME	PIN FUNCTION	PIN TYPE
2	1	VDD	Positive power supply voltage	Power (24V)
3	2	DP1	External Diode 1 positive (anode) connection	AIO (2V)
4	3	DN1	External Diode 1 negative (cathode) connection	AIO (2V)
5	4	DP2 / DN3	External Diode 2 positive (anode) connection and External Diode 3 negative (cathode) connection	AIO (2V)
6	5	DN2 / DP3	External Diode 2 negative (cathode) connection and External Diode 3 positive (anode) connection	AIO (2V)
7	6	ADDR_SEL	Selects SMBus Address	AI

Table 1.1 Pin Description for EMC1704-X (continued)

PIN NUMBER EMC1704-1	PIN NUMBER EMC1704-2	PIN NAME	PIN FUNCTION	PIN TYPE
8	7	GPIO	GPI - General Purpose Input	DI (5V)
			GPO - Open Drain General Purpose output	OD (5V)
9	8	GND	Ground	Power
10	9	$\overline{\text{THERM}}$	Active low output - requires pull-up resistor	OD (5V)
11	10	$\overline{\text{ALERT}}$	Active low output - requires pull-up resistor	OD (5V)
12	11	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
13	12	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
n/a	13	DUR_SEL	Selects peak detector duration	AI
n/a	14	TH_SEL	Selects peak detector threshold	AI
14	15	SENSE-	Negative current sense measurement point	AI (24V)
1	16	SENSE+	Positive current sense measurement point	AI (24V)

The pin types are described in [Table 1.2](#). All pins labeled with (5V) are 5V tolerant. All pins labeled with (24V) are 24V tolerant.

Table 1.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
AI	Analog Input - this pin is used as an input for analog signals.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DI	Digital Input - this pin is used for digital inputs. This pin is 5V tolerant.
DIOD	Open Drain Digital Input / Output - this pin is bi-directional. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 2 Electrical Characteristics

Table 2.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins	-0.3 to 5.5	V
Voltage on 2V tolerant pins	-0.3 to 2	V
Voltage on VDD, SENSE- and SENSE+ pins	-0.3 to 26	V
Voltage on any other pin to GND	-0.3 to 4	V
Voltage between Sense pins ((SENSE+ - SENSE-))	< 6	V
Package Power Dissipation	0.5W up to $T_A = 85^\circ\text{C}$	W
Junction to Ambient (θ_{JA}) (SOIC package)	78	$^\circ\text{C/W}$
Junction to Ambient (θ_{JA}) (QFN16 package)	58	$^\circ\text{C/W}$
Operating Ambient Temperature Range	-40 to 85	$^\circ\text{C}$
Storage Temperature Range	-55 to 150	$^\circ\text{C}$
ESD Rating - SMCLK, SMDATA, $\overline{\text{ALERT}}$, $\overline{\text{THERM}}$ pins - HBM	4000	V
ESD Rating - All other pins - HBM	2000	V

Note 2.1 Stresses at or above those values listed could cause permanent damage to the device. This is a stress rating only, and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. Prolonged stresses above the stated operating levels and below the Absolute Maximum Ratings may degrade device performance and lead to permanent damage.

Note 2.2 All voltages are relative to ground.

Note 2.3 The Package Power Dissipation specification assumes a thermal via design with the thermal landing be soldered to the PCB ground plane with four 12 mil vias (where applicable).

Note 2.4 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W (EMC1704-2) including localized PCB temperature increase.

2.1 Electrical Specifications

Table 2.2 Electrical Specifications

$V_{DD} = V_{BUS} = 3V \text{ TO } 24V$, $V_{PULLUP} = 3V \text{ TO } 5.5V$, $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$, ALL TYPICAL VALUES AT $V_{DD} = V_{PULLUP} = 3.3V$, $V_{BUS} = 12V$, AND $T_A = 27^\circ\text{C}$ UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
DC POWER						
Supply Voltage	V_{DD}	3		24	V	
VDD Pin Supply Current	I_{DD}		610	750	μA	Temp conversions at 0.0625 conversions / second, dynamic averaging disabled current sense active
			650	950	μA	Temp conversions at 4 conversions / second, dynamic averaging disabled current sense active
			950	1100	μA	Temp conversions at 8 conversions / second, dynamic averaging enabled current sense active
VDD Pin Supply Current	$I_{DD_T_STANDBY}$			750	μA	Temp conversions disabled (TMEAS / STOP = '1') current sense active
VDD Pin Supply Current	$I_{DD_ALL_STANDBY}$		470	580	μA	Temp conversions disabled (TMEAS / STOP = '1') Current sense disabled (IMEAS / STOP = '1')
SENSE+ Pin Bias Current	I_{SENSE+}		90		μA	$V_{SENSE} = 0V$, $V_{DD} = 3V \text{ to } 24V$, Current sense active
			15		μA	$V_{SENSE} = 0V$, $V_{DD} = 3V \text{ to } 24V$, current sense disabled
			10	20	μA	$V_{DD} = 0V$
SENSE- Pin Bias Current	I_{SENSE-}		10		μA	$V_{SENSE} = 0V$, $V_{DD} = 3V \text{ to } 24V$, Current sense active
			10		μA	$V_{SENSE} = 0V$, $V_{DD} = 3V \text{ to } 24V$, current sense disabled
			0		μA	$V_{DD} = 0V$
Pull-up Voltage	V_{PULLUP}	3		5.5	V	Pull-up voltage for SMBus, GPIO, ALERT, and THERM pins
Leakage Current (\pm)	I_{LEAK}			5	μA	ALERT, THERM, and GPIO pins, SMDATA and SMCLK pins powered or unpowered, $T_A < 85^\circ\text{C}$

Table 2.2 Electrical Specifications (continued)

$V_{DD} = V_{BUS} = 3V \text{ TO } 24V$, $V_{PULLUP} = 3V \text{ TO } 5.5V$, $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$, ALL TYPICAL VALUES AT $V_{DD} = V_{PULLUP} = 3.3V$, $V_{BUS} = 12V$, AND $T_A = 27^\circ\text{C}$ UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
CURRENT SENSE						
Common Mode Voltage	V_{CM}	3		24	V	Voltage on SENSE+ and/or SENSE- pins, referenced to Ground
Differential Mode Voltage	V_{DIFF}	-6		+6	V	Voltage between SENSE+ and SENSE- pins
Full Scale Range (\pm) (see Section 5.20)	FSR	0		10	mV	1 LSB = 4.885uV
		0		20	mV	1 LSB = 9.77uV
		0		40	mV	1 LSB = 19.54uV
		0		80	mV	1 LSB = 39.08uV
Total Measurement Error (\pm)	V_{SENSE_ERR}		0.5	1	%	Total Error, FSR = 80mV
				3	%	Total Error, FSR = 10mV to 40mV
Offset Error (\pm)	V_{SENSE_OFF}			3	LSB	Offset Error, FSR = 80mV
Power Supply Rejection	V_{SENSE_PSR}		-120		dB	FSR = 10mV to 80mV, 3V < V_{DD} < 24V
Common Mode Rejection	V_{SENSE_CMR}		-110		dB	FSR = 10mV to 80mV, 3V < V_{BUS} < 24V
SOURCE VOLTAGE						
Full Scale Voltage	FSV	3		23.9883	V	Voltage on SENSE+ pin
Total Measurement Error (\pm) (see Section 4.1.2)	V_{SOURCE_ERR}		0.2	0.5	%	
POWER RATIO						
Full Scale Range		0		100	%	1 LSB = 1.53m%
Total Measurement Error (\pm)	P_{RATIO_ERR}			1.6	%	FSR = 80mV
				3	%	FSR = 10mV to 40mV
CURRENT SENSE PEAK DETECTION						
Peak Detector Threshold Range	V_{TH}	10		85	mV	Programmable via TH_SEL pin (EMC1704-2 only)
Peak Detector Duration Range	T_{DUR}	1		4096	ms	Programmable via DUR_SEL pin (EMC1704-2 only)
V_{SENSE} Peak Detection	t_{FILTER}		5		us	

Table 2.2 Electrical Specifications (continued)

$V_{DD} = V_{BUS} = 3V \text{ TO } 24V$, $V_{PULLUP} = 3V \text{ TO } 5.5V$, $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$, ALL TYPICAL VALUES AT $V_{DD} = V_{PULLUP} = 3.3V$, $V_{BUS} = 12V$, AND $T_A = 27^\circ\text{C}$ UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Threshold Accuracy (±)	V_{TH_ERR}		2	5	%	$V_{TH} = 80\text{mV}$
EXTERNAL TEMPERATURE MONITORS						
Temperature Accuracy (±)			0.25	1	°C	$+20^\circ\text{C} < T_{DIODE} < +110^\circ\text{C}$ $0^\circ\text{C} < T_A < 85^\circ\text{C}$
			0.5	2	°C	$-40^\circ\text{C} < T_{DIODE} < 127^\circ\text{C}$
Temperature Resolution			0.125		°C	
Diode Decoupling Capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Series Resistance Canceled	R_{SERIES}			100	Ohm	Sum of series resistance in both DP and DN lines
INTERNAL TEMPERATURE MONITOR						
Temperature Accuracy (±)			0.25	1	°C	$-5^\circ\text{C} < T_A < 85^\circ\text{C}$
				2	°C	$-40^\circ\text{C} < T_A < 85^\circ\text{C}$
Temperature Resolution			0.125		°C	
CONVERSION TIMES						
First Conversion Ready	t_{CONV_T}		180	300	ms	Time after power up before temperature and voltage measurements updated and P_{RATIO} updated
SMBus Delay	t_{SMB_D}			25	ms	Time before SMBus communications should be sent by host
DIGITAL I/O PINS (SMCLK, SMDATA, THERM, ALERT, GPIO)						
Input High Voltage	V_{IH}	2.0			V	SMCLK, SMDATA, and GPIO pins, OD pins pulled up to V_{PULLUP}
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	OD pin pulled to V_{PULLUP} 4 mA current sink

APPLICATION NOTE: The EMC1704 is trimmed at the 80mV range for best accuracy.

2.2 SMBus Electrical Specifications

Table 2.3 SMBus Electrical Specifications

V _{DD} = V _{BUS} = 3V to 24V, V _{PULLUP} = 3V to 5.5V, T _A = -40°C to 85°C Typical values are at T _A = 27°C unless otherwise noted.						
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
SMBUS INTERFACE						
Input Capacitance	C _{IN}		4	10	pF	
SMBUS TIMING						
Clock Frequency	f _{SMB}	10		400	kHz	
Spike Suppression	t _{SP}			50	ns	
Bus Free Time Start to Stop	t _{BUF}	1.3			us	
Setup Time: Start	t _{SU:STA}	0.6			us	
Setup Time: Stop	t _{SU:STO}	0.6			us	
Data Hold Time	t _{HD:DAT}	0			us	
Data Setup Time	t _{SU:DAT}	0.6			us	
Clock Low Period	t _{LOW}	1.3			us	
Clock High Period	t _{HIGH}	0.6			us	
Clock/Data Fall time	t _{FALL}			300	ns	Min = 20+0.1C _{LOAD} ns
Clock/Data Rise time	t _{RISE}			300	ns	Min = 20+0.1C _{LOAD} ns
Capacitive Load	C _{LOAD}			400	pF	Total per bus line

Chapter 3 Communications

3.1 System Management Bus Interface Protocol

The EMC1704 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the EMC1704 will not stretch the clock signal.

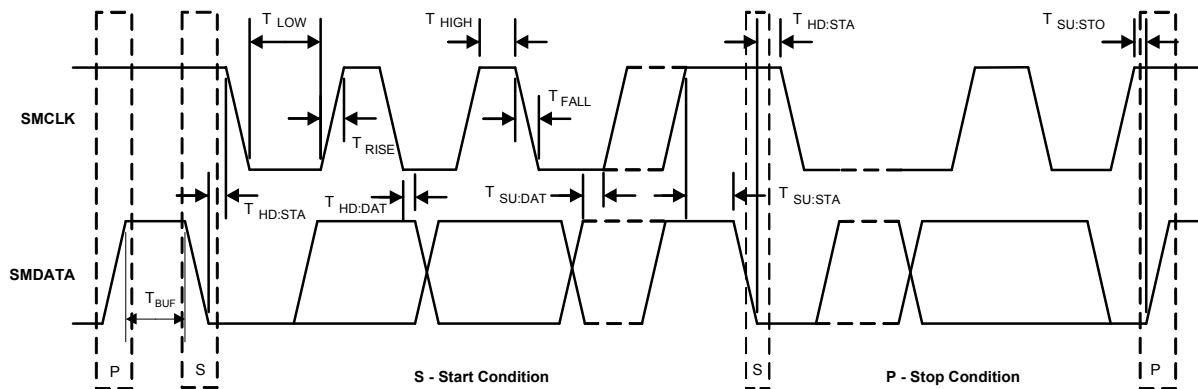


Figure 3.1 SMBus Timing Diagram

3.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

3.1.2 SMBus Address and RD / $\overline{\text{WR}}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a 1-bit RD / $\overline{\text{WR}}$ indicator. If this RD / $\overline{\text{WR}}$ bit is a logic '0', the SMBus host is writing data to the client device. If this RD / $\overline{\text{WR}}$ bit is a logic '1', the SMBus host is reading data from the client device.

The EMC1704 SMBus address is determined by a single resistor connected between ground and the ADDR_SEL pin as shown in Table 3.1.

Table 3.1 ADDR_SEL Resistor Setting

RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)	1600	0101_000(r/w)
100	1001_101(r/w)	2000	0101_001(r/w)
180	1001_110(r/w)	2700	0101_010(r/w)
300	1001_111(r/w)	3600	0101_011(r/w)
430	1001_000(r/w)	5600	0101_100(r/w)

Table 3.1 ADDR_SEL Resistor Setting (continued)

RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
560	1001_001(r/w)	9100	0101_100(r/w)
750	1001_010(r/w)	20000	0101_101(r/w)
1270	1001_011(r/w)	Open	0011_000(r/w)

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.1.3 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the **ALERT** pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

3.1.4 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC1704 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.1.5 SMBus Time-out

The EMC1704 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The time-out functionality defaults to disabled and can be enabled by writing to the TIMEOUT bit (see [Section 5.12](#)).

3.1.6 SMBus and I²C Compliance

The major differences between SMBus and I²C devices are highlighted here. For complete compliance information, refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held at a logic '0' for longer than 30ms. This time-out functionality is disabled by default.
3. The client protocol will reset if both the clock and data lines are held at a logic '1' for longer than 150us. This function is disabled by default.
4. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).

3.2 SMBus Protocols

The EMC1704 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte, Write Byte, Block Read, and Block Write as valid protocols. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the protocols listed below use the convention in [Table 3.2](#).

Table 3.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

3.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers, as shown in [Table 3.3](#):

Table 3.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

3.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers, as shown in [Table 3.4](#).

Table 3.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1	YYYY_YYY	1	0	XXh	1	0 -> 1

3.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in [Table 3.5](#).

Table 3.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1

3.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads

of the same register, as shown in [Table 3.6](#).

Table 3.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

3.2.5 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in [Table 3.7](#). It is an extension of the Write Byte Protocol.

Table 3.7 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
REGISTER DATA	ACK	REGISTER DATA	ACK	...	REGISTER DATA	ACK	STOP
XXh	0	XXh	0	...	XXh	0	0 -> 1

3.2.6 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in [Table 3.8](#). It is an extension of the Read Byte Protocol.

Table 3.8 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	REGISTER DATA	ACK	REGISTER DATA	ACK	REGISTER DATA	ACK	...	REGISTER DATA	NACK	STOP
0	XXh	0	XXh	0	XXh	0	...	XXh	1	0 -> 1

3.2.7 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address, as shown in [Table 3.9](#).

Table 3.9 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP

Table 3.9 Alert Response Address Protocol

1 -> 0	0001_100	1	0	YYYY_YYY	1	0 -> 1
--------	----------	---	---	----------	---	--------

The EMC1704 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

Chapter 4 General Description

The EMC1704 is a combination high-side current sensing device with precision voltage and temperature measurement capabilities. It measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The EMC1704 also measures the source voltage and uses these measured values to present a proportional power calculation. The EMC1704 contains additional bi-directional peak detection circuitry to flag instantaneous current spikes with programmable time duration and magnitude thresholds. Finally, the EMC1704 includes up to three (3) external diode channels and an internal diode for temperature measurement.

The EMC1704 current-sense measurement converts differential input voltage measured across an external sense resistor to a proportional output voltage. This voltage is digitized using a variable resolution (13-bit to 15-bit) Sigma-Delta ADC and transmitted via the SMBus or I²C protocol. The current range allows for large variations in measured current with high accuracy and low voltage drop across the resistor.

The supply voltage is also measured and stored. When combined with the sense resistor voltage measurement the power provided from the source can be determined. Programmable limits on both voltage and current levels are used to generate an interrupt.

The EMC1704 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures or voltages meet or exceed user programmable limits. This allows the EMC1704 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a non maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured values meet or exceed a second programmable limit.

The temperature measurement includes advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm and 65nm processors) and automatic diode type detection. These features combine to provide a robust solution for complex environmental monitoring applications.

A system diagram is shown in [Figure 4.1](#).

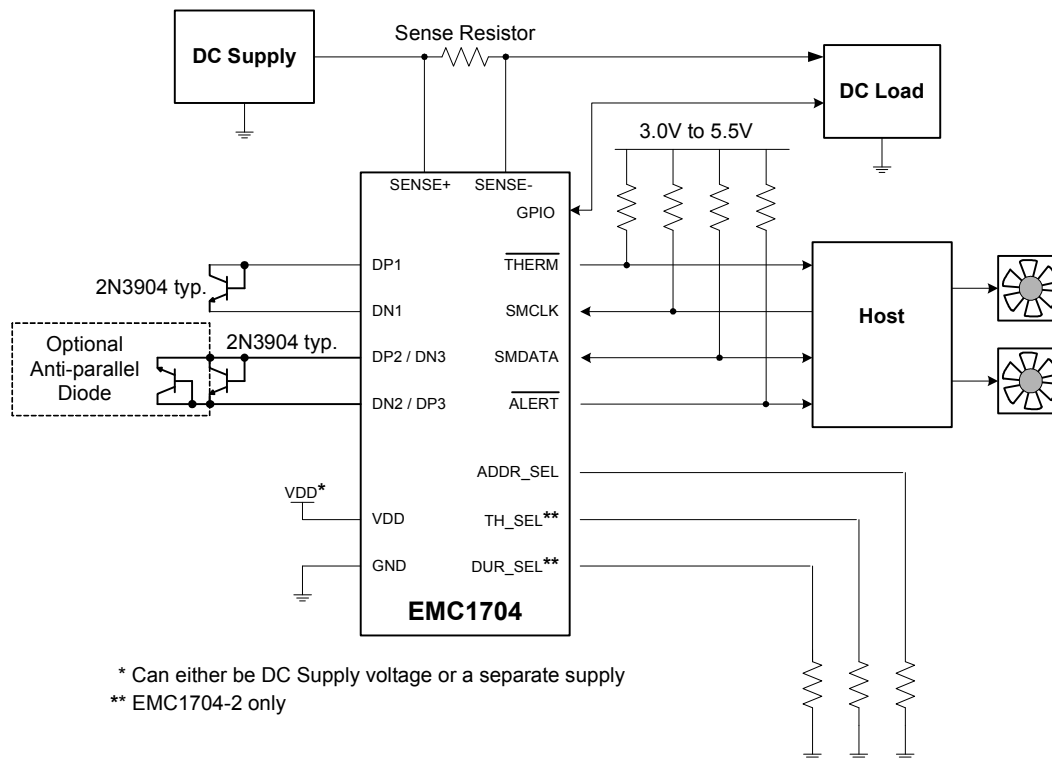


Figure 4.1 EMC1704 System Diagram

4.1 Source Monitoring

The EMC1704 includes circuitry for both source current sensing and source voltage measurement. From these measurements, a ratiometric value corresponding to the power delivered at the SENSE+ pin is provided.

4.1.1 Current Measurement

The EMC1704 includes a high-side current sensing circuit. This circuit measures the voltage, V_{SENSE} , induced across a fixed external current sense resistor, R_{SENSE} , and stores a representative voltage as a signed 11-bit number in the Sense Voltage Registers (see Section 5.22).

This circuitry is able to measure the direction of current flow (from SENSE+ to SENSE- or from SENSE- to SENSE+). Current flowing from SENSE+ to SENSE- is defined as positive current. Current flowing from SENSE- to SENSE+ is defined as negative.

The EMC1704 contains user programmable bipolar Full Scale Sense Ranges (FSSR) of $\pm 10\text{mV}$, $\pm 20\text{mV}$, $\pm 40\text{mV}$, or $\pm 80\text{mV}$ (see Section 5.20). The default for this setting is $\pm 80\text{mV}$.

Each V_{SENSE} measurement is averaged over a user programmable time (see Section 5.20). It is compared against programmable high and low limits (see Section 5.25). If V_{SENSE} exceeds (or drops below) the respective limits, the $\overline{\text{ALERT}}$ pin may be asserted (the default operation is to enable current sense interrupts on the $\overline{\text{ALERT}}$ pin).

The EMC1704 also contains user programmable current peak detection circuitry (see Section 4.1.4) that will assert the $\overline{\text{THERM}}$ pin if a current spike is detected larger than the programmed threshold and of longer duration than the programmed time. This circuitry is independent of V_{SENSE} .

Full Scale Current (FSC) can be calculated from:

$FSC = \frac{FSR}{R_{SENSE}}$	where:	[1]
	FSC is the Full-Scale Current	
	FSR, the Full Scale Range, is either 10mV, 20mV, 40mV or 80mV (see Section 5.20)	
	R _{SENSE} is the external sense resistor value	

Actual source current through R_{SENSE} can then be calculated using:

$I_{SOURCE} = FSC \times \frac{V_{SENSE}}{2,047}$	where:	[2]
	I _{SOURCE} is the actual source current	
	FSC is the Full-Scale Current value (from Equation [1])	
	V _{SENSE} is the value read from the Sense Voltage Registers, ignoring the four lowest bits which are always zero (see Section 5.22)	

For example: Suppose the system is drawing 1.65A through a 10mΩ resistor and the FSR is set for 20mV. Therefore, by [Equation \[1\]](#), the FSC is 2A.

For a positive voltage the Sense Voltage Registers are read, ignoring the lower four bits since they are always zero, as 69_8h (0110_1001_1000b or 1688d) which is 82.5% of the full scale source current. This results in a calculated source current of 1.649A using [Equation \[2\]](#).

For a negative voltage the Sense Voltage Registers are read as 96_8h, also ignoring the lower four bits since they are always zero. To calculate source current the binary value is first converted from two's complement by inverting the bits and adding one:

96_8h = 1001_0110_1000b. Inverting equals 0110_1001_0111b (69_7h) and adding one gives 0110_1001_1000b (69_8h).

This results in the same calculated value as in the positive voltage case.

4.1.2 Voltage Measurement

Source voltage is measured on the supply side of the R_{SENSE} resistor (SENSE+) and stored as an unsigned 11-bit number in the Source Voltage Registers as V_{SOURCE} (see [Section 5.23](#)).

Each V_{SOURCE} measurement is averaged over a user programmable time (see [Section 5.6](#) and [Section 5.19](#)). The measurement is delayed by the programmed conversion rate. V_{SOURCE} is compared against programmable high, low, and critical limits (see [Section 5.15](#), [Section 5.16](#), and [Section 5.17](#)). If the value meets or exceeds the high limits or drops below the low limits, the ALERT pin may be asserted (default is to enable this function). If the value meets or exceeds the critical limit, the THERM pin will be asserted (see [Section 5.27](#)).

Full Scale Voltage (FSV) is given by the maximum value of the Source Voltage Registers:

$FSV = 23.9883V$	where:	[3]
	FSV is the Full-Scale Voltage (a constant)	

Actual source voltage at the SENSE+ pin can be calculated using:

$\text{Source Voltage} = FSV \times \frac{V_{SOURCE}}{4,094}$	where:	[4]
	Source Voltage is the voltage at the SENSE+ pin	
	FSV is the Full-Scale Voltage (from Equation [3])	
	V_{SOURCE} is the digital value read from the Source Voltage Registers. Note that the lowest five bits are always zero (see Section 5.23)	

For example: Suppose that the actual source voltage is 10.65V. The Source Voltage Registers are read as $V_{SOURCE} = 71_{Ah}$ (0111_0001_1010b or 1818d) which is 44.4% of the full scale source voltage. This results in a calculated source voltage of 10.65V using [Equation \[4\]](#).

Note that the actual source voltage may also be determined by scaling each bit set by the indicated bit weighting as described in [Section 5.23](#).

4.1.3 Power Calculation

The EMC1704 may be used to determine the average power provided at the source side of R_{SENSE} (SENSE+) using the value, P_{RATIO} , contained in the Power Ratio Registers (see [Section 5.24](#)). The value represents the % of maximum calculable power.

P_{RATIO} is mathematically generated by multiplying the absolute values of V_{SENSE} and V_{SOURCE} (see [Section 4.1.1](#) and [Section 4.1.2](#)) and stored as a shifted 16-bit unsigned number. P_{RATIO} is updated whenever either V_{SENSE} or V_{SOURCE} is updated.

Full Scale Power can be calculated from:

$FSP = FSC \times FSV$	where:	[5]
	FSP is the Full-Scale Power	
	FSC is the Full-Scale Current (from Equation [1])	
	FSV is the Full-Scale Voltage (from Equation [3])	

Actual power drawn from the source can be calculated using:

$P_{SOURCE} = FSP \times \frac{P_{RATIO}}{65,535}$	where:	[6]
	P_{SOURCE} is the actual power provided by the source measured at SENSE+	
	FSP is the Full-Scale Power (from Equation [5])	
	P_{RATIO} is the value read from the Power Ratio Registers (see Section 5.24)	