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EMC2101

SMBus Fan Control with 1°C Accurate Temperature Monitoring

PRODUCT FEATURES

Datasheet

General Description

The EMC2101 is an SMBus 2.0 compliant, integrated fan control solution complete with two temperature monitors, one external and one internal. Each temperature channel has programmable high limits that can assert an interrupt.

The fan drive is selectable as a Pulse Width Modulator (PWM) or Linear (DAC) output. The fan control output, whether the PWM or DAC drive circuit, uses an eight position look-up table to allow the user to program the fan speed profile based on temperature. The DAC output ranges from 0V to V_{DD} with up to 6 bit resolution while the PWM output has a range of 0% to 100% with up to 64 steps.

The EMC2101 has an option to automatically upload the contents of an attached SMBus compatible EEPROM for auto-programming upon power up.

Advanced thermal sensing enables reduced validation and characterization time as well as accurately operating with smaller-geometry processors. Resistance Error Correction (REC) automatically corrects the offset errors of board trace and device resistance, up to 100Ω. Automatic Beta Compensation allows the user the flexibility to design applications that include processor substrate transistors.

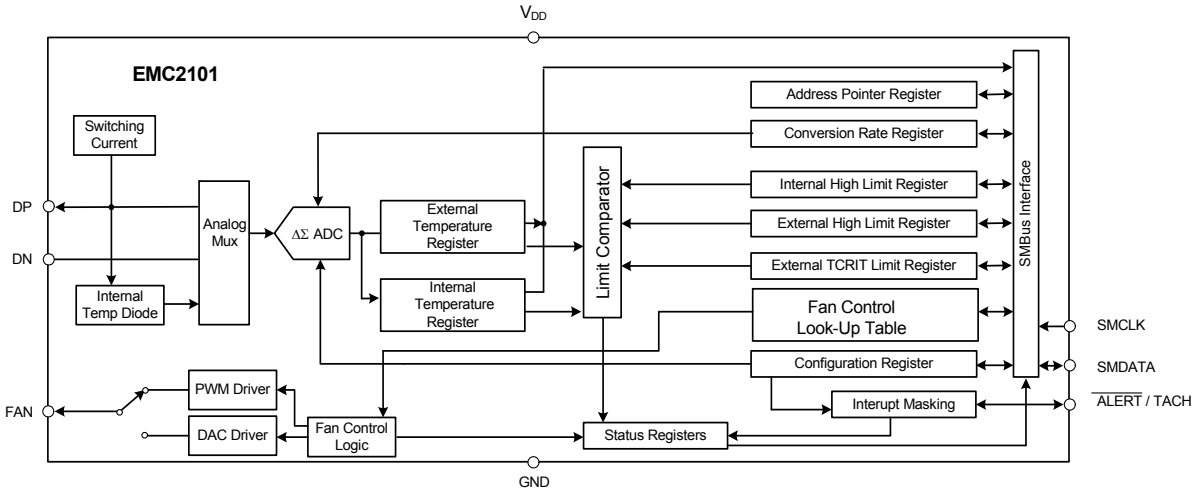
Features

- Automatic Beta Compensation
- Resistance Error Correction
- Self-programming with available SMBus compatible EEPROM
- Selectable PWM or DAC fan driver output
- Temperature Monitors
  - — External channel ±1°C accuracy
  - — Internal channel ±2°C accuracy
- 3.3 Volt Operation (5 Volt Tolerant Input Buffers)
- SMBus 2.0 Compliant Interface, supports TIMEOUT
- 8-Pin MSOP Lead-free RoHS Compliant Packages
- 8-Pin SOIC Lead-free RoHS Compliant Package

Applications

- Graphics Processors
- Embedded Application Fan Drive
- PWM Controller + Temp Sensor

Block Diagram



ORDER NUMBERS:

EMC2101-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE

EMC2101-R-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE

EMC2101-ACZT-TR FOR 8-PIN, SOIC LEAD-FREE ROHS COMPLIANT PACKAGE

REEL SIZE IS 4,000 PIECES

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 Device Selection

The EMC2101 is available with the following options and configurations as shown in Table 1.1.

Table 1.1 Device Selection

PART NUMBER	FAN OPERATION	COMMUNICATIONS	PACKAGE	PRODUCT ID
EMC2101	PWM Drive, 0% drive	SMBus	8 pin SOIC and 8 pin MSOP	16h
EMC2101-R	Selected via pull-up	Selected via pull-up	8 pin MSOP	28h

Chapter 2 Pin Layout

2.1 Pin Diagram for EMC2101

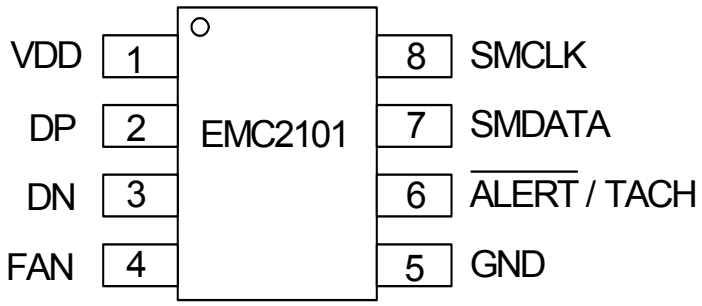

Figure 2.1 EMC2101 Pinout

2.2 Pin Description for EMC2101

Table 2.1 Pin Description

PIN	NAME	FUNCTION	TYPE
1	VDD	3.3V Power supply	Power
2	DP	External diode positive (anode) connection	AI
3	DN	External diode negative (cathode) connection	AI
4	FAN	PWM Output (default - software programmed)	OD (5V)
		DAC Output software programmed	AO
5	GND	Ground	Power
6	$\overline{\text{ALERT}}$ / TACH	$\overline{\text{ALERT}}$ - Open drain I/O operates as active low interrupt or TACH input - requires pull-up resistor, which defines auto-configuration mode (see Table 5.1)	OD (5V)
		TACH - TACH input	DI (5V)
7	SMDATA	SMBus Data input/output	DIOD Output (5V)
8	SMCLK	SMBus Clock input	DIOD Output (5V)

The pin types are described below. All pins labelled with (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AI	Analog Input - this pin is used as an input for analog signals.
AO	Analog Output - this pin is used as an output for analog signals.
DIOD	Digital Input / Open Drain Output - this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 5.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_pin} - V_{DD}\|$) (see Note 3.1)	-0.3 to 3.6	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for MSOP-8		
Thermal Resistance	140.8	°C/W
Package Thermal Characteristics for SOIC-8		
Thermal Resistance	135.9	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the EMC2101 is unpowered.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

Table 3.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current	I_{DD}		0.6	1	mA	16 conversion / second - PWM or DAC driver operational
Supply Current	I_{DD}		200		uA	1 conversion / 16 seconds - PWM driver operational
Supply Current	I_{DD}		300		uA	1 conversion / 16 seconds - DAC Driver, no load
Supply Current	I_{DD}		300	400	uA	Temp monitoring Disabled, DAC Driver enabled, no load
Standby Current	$I_{STANDBY}$			270	µA	PWM disabled, Monitoring disabled
Internal Temperature Monitor						
Temperature Accuracy			±1	±2	°C	
Temperature Resolution			±1		°C	8 bit resolution
Conversion Time Internal Channel	t_{CONV}		3		ms	
External Temperature Monitor						
Temperature Accuracy			±0.5	±1	°C	60°C < T_{DIODE} < 100°C, 10°C < T_A < 70°C
			±1	±3	°C	0°C < T_{DIODE} < 125°C
Temperature Resolution			0.125		°C	11 bit resolution
Conversion Time External Channel	t_{CONV}		21		ms	
Diode Decoupling Capacitor	C_{FILTER}			2.2	nF	Connected across External Diode (2N3904)
Diode Decoupling Capacitor	C_{FILTER}			470	pF	Connected across Substrate Transistor (CPU diode)
Resistance Error Correction	R_{SERIES}		100		Ω	Series resistance in DP and DN lines
TACH Measurement						
TACH Accuracy				10	%	TACH valid
Fan Counter Clock Frequency			90		kHz	
Pulse Width Modulator Fan Driver						
PWM Resolution			64		steps	
PWM Frequency	f_{PWM}	22		5k	Hz	For 64 steps, higher frequencies are possible with reduced resolution (see Appendix A "Advanced PWM Options").

Table 3.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
PWM Duty cycle	D_{PWM}	0		100	%	
DAC Fan Driver						
Output Voltage Drive	V_{DAC}	0.2		V_{DD} - 0.2	V	Current Load = ±1mA
Total Unadjusted Error	TUE		5		%	Measured at 3/4 full scale
DAC Resolution			6		bits	
Settling Time to within 1%	t_{SETTLE}		40		us	Capacitive Load = 100pF
Digital I/O pins (PWM, SMDATA, SMCLK, $\overline{\text{ALERT}}$ / TACH)						
Output High Voltage	V_{OH}	V_{DD} - 0.3			V	8mA Current Source
Output Low Voltage	V_{OL}			0.3	V	8mA Current Sink
Output Leakage Current	I_{LEAK}			10	uA	Device powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V

3.3 SMBus Client Electrical Specifications

Table 3.3 SMBus Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			500		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			8		mA	V_{OL} = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	

Table 3.3 SMBus Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns (Note 3.2)
Capacitive Load	C_{LOAD}			400	pF	per bus line

Note 3.2 300ns rise time max is required for 400kHz bus operation. For lower clock frequencies the maximum rise time is (0.1 / f_{SMB})+ 50ns.

3.4 EEPROM Loader Electrical Specifications (EMC2101-R only)

Table 3.4 EEPROM Loader Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Interface						
Input High Voltage	V_{IH}	2.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			500		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			8		mA	V_{OL} = 0.4V
Timing						
Loading Delay	t_{DLY}		10		ms	Delay after power-up until EEPROM loading begins. (See Section 4.9.)
Loading Time	t_{LOAD}		50		ms	
Clock Frequency	f_{SMB}		50		kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	

Table 3.4 EEPROM Loader Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC2101 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2101 will not stretch the clock signal.

The EMC2101 powers up as an SMBus client (after loading from EEPROM as applicable).

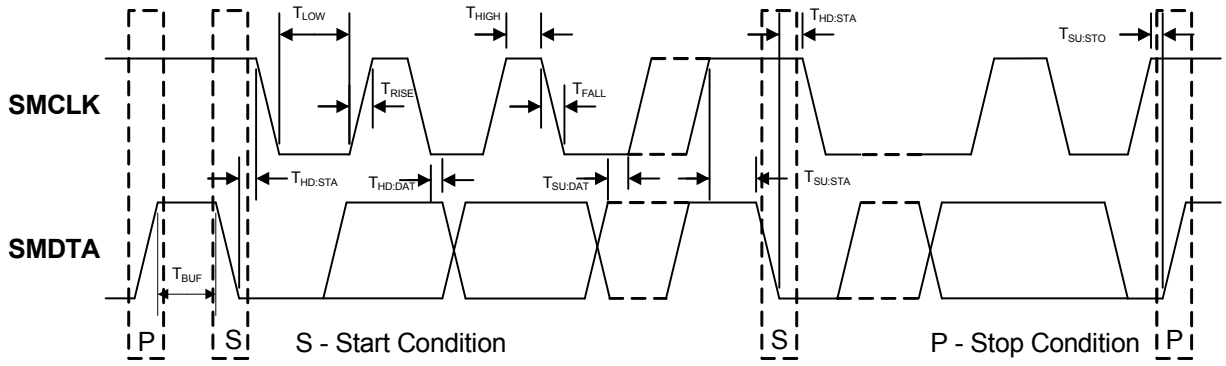

Figure 4.1 SMBus Timing Diagram

The EMC2101 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2.

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1	7	1	1	8	1	1

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1	7	1	1	8	1	1

4.6 Alert Response Address

The $\overline{\text{ALERT}}$ / TACH output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ / TACH pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 000_1100b. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1	7	1	1	8	1	1

The EMC2101 will respond to the ARA in the following way when the $\overline{\text{ALERT}}$ / TACH pin is configured as an Interrupt:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ / TACH pin only if there are no bits set in the Status Register. If there are error condition bits set in the Status Register, it must be read before the MASK bit will be set.

When the $\overline{\text{ALERT}}$ / TACH pin is configured to operate in Comparator Mode, or as a TACH input, (see Section 5.4.1), it will not respond to the ARA command. Additionally, the EMC2101 will not respond to the ARA command if the $\overline{\text{ALERT}}$ / TACH pin is not asserted.

4.7 SMBus Address

The EMC2101 is addressed on the SMBus as 100_1100b.

Attempting to communicate with the EMC2101 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.8 SMBus Time-out

The EMC2101 includes an SMBus time-out feature. Following a 25ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

4.9 Programming from EEPROM

The EMC2101-R acts as a simple SMBus Master to read data from a connected EEPROM using the following procedure:

1. After power-up the EMC2101-R waits for 10ms with the SMDATA and SMCLK pins tri-stated.
2. Once the wait period has elapsed, the EMC2101-R sends a START signal followed by the 7 bit client address 101_0000b followed by a ‘1b’ and waits for an ACK signal from the EEPROM.
3. When the EEPROM sends the ACK signal, the EMC2101-R will send a second start signal and continue sending the Block Read Command (see Table 4.7) to the same slave address. It reads 256 data bytes from the EEPROM sending an ACK between each data byte. When 256 data bytes have been received, it sends a NACK signal followed by a STOP bit.
4. Resets the device as an SMBus Client.

If the EMC2101-R does not receive an acknowledge bit from the EEPROM then the following will occur:

1. The $\overline{\text{ALERT}}$ / TACH pin will be asserted and will remain asserted until a Host device initiates communication with the EMC2101 and reads the Status Register at offset 0x02. The $\overline{\text{ALERT}}$ / TACH pin will be de-asserted after a single Status Register read, i.e. it is not sticky.
2. The EMC2101-R will reset its SMBus protocol as a slave interface and start operating from the default conditions.

Table 4.7 Block Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	SLAVE ADDRESS	RD	ACK	Register Data	. . .
1	7	1	1	8	1	1	7	1	1	8	. . .
ACK	Register Data (00h)	ACK	Register Data (01h)	ACK	Register Data (02h)	. . .	ACK	Register Data (FFh)		NACK	STOP
1	8	1	8	1	8	. . .	1	8		1	1

Note: The shaded columns represent data sent from the EMC2101 to the EEPROM device.

APPLICATION NOTE: It is recommended that the EEPROM that is used be an AT24C02B or equivalent device. The EEPROM slave address must be 101_0000b. The device must support a block-read command, 8-bit addressing, and 8-bit data formatting using a 2-wire bus. The device must support 3.3V digital switching logic and may not pull the SMCLK and SMDATA pins above 5V. Data must be transmitted MSB first.

APPLICATION NOTE: No other SMBus Master should exist on the SMDATA and SMCLK lines. The presence of another SMBus Master will cause errors in reading from the EEPROM.

The EEPROM should be loaded to mirror the register set of the EMC2101 with the desired configuration set. All undefined registers in the EMC2101 register set should be loaded with 00h in the EEPROM. Likewise, all registers that are read-only in the EMC2101 register set should be loaded with 00h in the EEPROM.

Because of the interaction between the Fan Control Look-up Table and the Fan Configuration Register, the EEPROM Loader stores the contents of the Fan Configuration Register and updates this register at the end of the EEPROM loading cycle. (See Section 6.16 and Section 6.22).

Chapter 5 General Description

The EMC2101 is an environmental monitoring device with a selectable PWM or DAC fan driver output, one external temperature monitoring channel and one internal temperature monitor. It contains advanced circuitry to remove errors induced by series resistance and CPU thermal diode process differences to provide accurate temperature measurements and accurate fan control.

Thermal management is performed automatically. The EMC2101 reads the temperature from both the external and internal temperature diodes and uses the external temperature data to control the fan speed.

The FAN output can be configured as a PWM (default) or DAC output. The PWM fan driver uses an eight entry look up table to create a programmable temperature response. The DAC output provides a linear drive for the system fan circuit using this same look up table.

Each temperature measurement channel is continuously compared against programmed high limits. The external diode channel is compared against a programmed low limit. $\overline{\text{ALERT}}$ / TACH interrupt pin is asserted if the measured value exceeds the high limit or drops below the low limit. In addition, the external diode contains a programmable critical temperature, TCRIT. If the measured temperature exceeds this T_{CRIT} an interrupt is asserted on the $\overline{\text{ALERT}}$ / TACH pin and the fan is set to full on.

Finally, the EMC2101-R (only) has two configuration modes and two default fan settings based on the value of the pull-up-resistor on the $\overline{\text{ALERT}}$ / TACH pin. In the Manual Configuration Mode, the device acts as an SMBus client and waits to be configured by the system SMBus host. In the Automatic Configuration mode, the device automatically queries the SMBus for an EEPROM device and uploads configuration information from the EEPROM into its internal registers.

Figure 5.1 shows a system level block diagram of the EMC2101. Figure 5.2 shows a system level block diagram of the EMC2101-R.

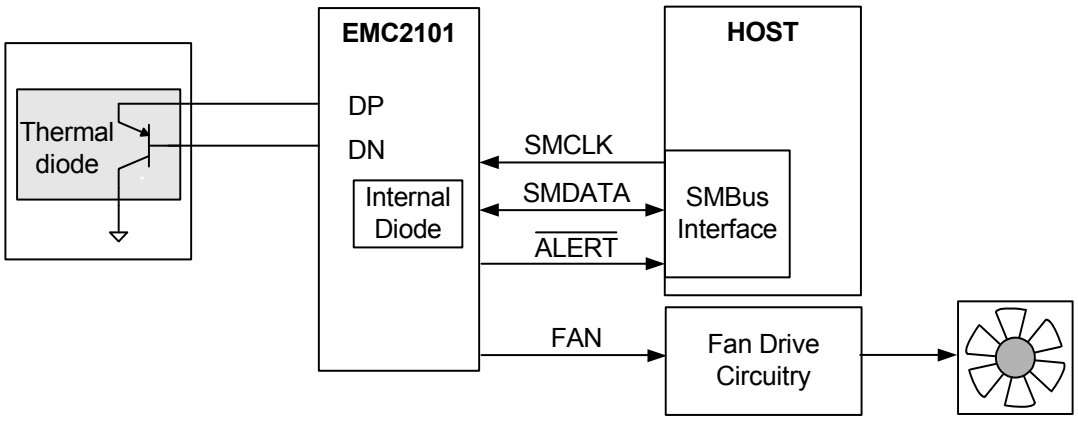

Figure 5.1 System Diagram for EMC2101

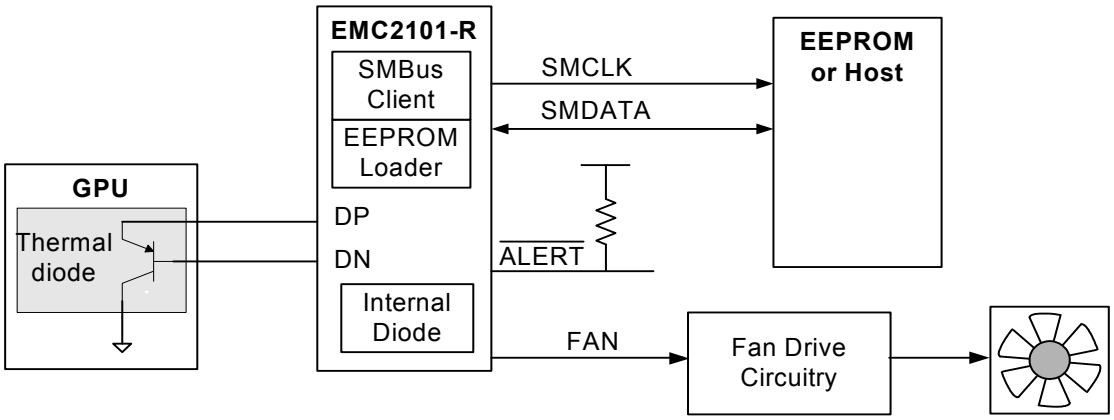

Figure 5.2 System Diagram for EMC2101-R

5.1 Modes of Operation (EMC2101-R Only)

The EMC2101-R has two modes of operation based on the pull-up resistor on the $\overline{\text{ALERT}}$ pin (see Table 5.1). The modes of operation are:

1. Host Configuration Mode - An SMBus Host configures the EMC2101-R upon startup to allow for polling for temperature or fan information or the user can use the $\overline{\text{ALERT}}$ pin interrupt to determine which action is required.
2. Automatic Configuration Mode - The EMC2101-R queries an SMBus compatible EEPROM located at a known address (see Section 4.9) and automatically loads its registers with the contents of the EEPROM. This mode does not require host intervention but a host can poll the device for temperature and fan information.

5.2 Power Up (EMC2101-R Only)

The EMC2101-R (only) will power up with the fan driver set to either 100% duty cycle or 0% duty cycle, depending on the value of the pull-up resistor on the $\overline{\text{ALERT}}$ / TACH pin. (See Table 5.1.) It will remain in this state until either the Fan Setting Register is written or until the following activities have occurred:

1. The Fan Control Look-Up Table is loaded and the PROG bit is set to ‘0’
2. The temperature monitoring block performs its first comparison against the Look-Up Table.

If the Fan Control Look-Up Table is used, the EMC2101-R Fan Driver will be immediately set to the appropriate setting in the table based on the measured temperature.

5.3 Power Modes

The EMC2101 supports multiple power modes that are user configurable. The temperature monitoring and fan control functions of the device are independent. The power modes are:

1. Normal - the temperature monitoring and fan driver circuits are both active. The device updates all temperature channels at the user programmed conversion rate (see Table 6.6). Every time the temperature is updated, the limits are checked and the fan driver is updated based on the values in the Fan Control Look-Up Table (if the Fan Control Look-Up Table is enabled).
2. Standby - the temperature monitoring and fan driver circuits are both disabled. The device will not update temperature data automatically and the fan output will be set to default drive. A one-shot

command can be issued that will refresh the temperature data. The limits are only checked when the temperature data is updated.

3. Mixed - the temperature monitoring block is disabled, but the fan driver block is active. The device will not update temperature data automatically and the fan driver output will not be updated automatically based on temperature. A one-shot command can be issued that will refresh the temperature data and update the fan driver based on the values in the Fan Control Look-Up Table (if the Fan Control Look-Up Table is enabled).

5.4 $\overline{\text{ALERT}}$ / TACH Output

The $\overline{\text{ALERT}}$ / TACH pin (Pin 6) is an open drain output and requires a pull-up resistor to V_{DD} when configured as an ALERT output.

APPLICATION NOTE: When configured as a TACH input, the $\overline{\text{ALERT}}$ / TACH pin will not function as an ALERT output. Error conditions will not trigger an interrupt (though will be updated in the Status Registers as normal) and the MASK bits will do nothing. Likewise, the device will not respond to the ARA command.

For the EMC2101-R, the value of this pull-up resistor determines the initial FAN output mode of operation as well as whether the device auto loads from an EEPROM or via an SMBus host per Table 5.1.

After power-up, the EMC2101-R requires 10ms to initialize and determine the operating mode.

When configured as an interrupt, the $\overline{\text{ALERT}}$ / TACH pin is maskable for each alert condition. If the $\overline{\text{ALERT}}$ / TACH pin is masked, then it will not respond to the corresponding condition (though the Alert Status Register will update normally). This pin has multiple functions described below and is controlled by ALERT_COMP bit (bit 0) in the Averaging Filter Register (BFh) (see Section 6.23).

Table 5.1 $\overline{\text{ALERT}}$/ TACH Pull-up Resistors - SMBus / FAN MODE for EMC2101-R

$\overline{\text{ALERT}}$ / TACH PULL-UP RESISTOR	SMBUS MODE	FAN MODE	POLARITY BIT SETTING (SEE Section 6.16)
5.6k Ohm ±5%	Host Load via SMBus	FAN output initialize to 100% Duty Cycle	1
10k Ohm ±5%	Host Load via SMBus	FAN output initialize to 0% Duty Cycle	0
18k Ohm ±5%	Auto Load via EEPROM	FAN output initialize to 100% Duty Cycle	1
33k Ohm ±5%	Auto Load via EEPROM	FAN output initialize to 0% Duty Cycle	0

5.4.1 $\overline{\text{ALERT}}$ / TACH as a Temperature Comparator

When the $\overline{\text{ALERT}}$ / TACH pin is used as a temperature comparator, the $\overline{\text{ALERT}}$ / TACH output is asserted when an out of limit measurement (> high limit, < low limit, or > TCRIT limit) is detected on any diode (low limits only apply to the external diode channel) or when the external diode connections are open. When the condition is no longer true, the $\overline{\text{ALERT}}$ / TACH output will de-assert. Reading from the Status Register will cause the $\overline{\text{ALERT}}$ / TACH pin to be released however it will not prevent it from being re-asserted based on the temperature comparisons.

Setting the MASK bit will not affect the $\overline{\text{ALERT}}$ / TACH pin when it is configured as a temperature comparator, however the individual channel mask bits will block the $\overline{\text{ALERT}}$ / TACH pin from being asserted.

5.4.2 $\overline{\text{ALERT}}$ / TACH as an Interrupt

When the $\overline{\text{ALERT}}$ / TACH pin is used as an interrupt signal the pin is asserted whenever an out-of-limit condition is detected. The $\overline{\text{ALERT}}$ / TACH pin will remain asserted until it is cleared even if the error condition is removed.

5.4.3 Mask Bit

The MASK bit behaves differently depending on which mode the $\overline{\text{ALERT}}$ / TACH pin is configured to operate in.

If the EMC2101 is configured with the $\overline{\text{ALERT}}$ / TACH pin operating in Interrupt Mode, the MASK bit will be set in the following cases:

1. Automatically after the Status Register has been read if any bits in the Status Register have been set (except BUSY and FAULT) (See Table 6.3).
2. Automatically when the EMC2101 responds to an Alert Response Address (ARA) command on an SMBus and the $\overline{\text{ALERT}}$ / TACH pin is asserted. The ARA command does not clear the Status Register. If the MASK bit is cleared prior to reading and clearing the Status Register, then the $\overline{\text{ALERT}}$ / TACH pin will be asserted.
3. Directly via the SMBus.

In Interrupt Mode, the MASK bit will block the $\overline{\text{ALERT}}$ / TACH pin from being asserted in response to an error condition.

If the EMC2101 is configured with the $\overline{\text{ALERT}}$ / TACH pin operating in Comparator Mode, the MASK bit can only be set via the SMBus. In this mode, setting the MASK bit willl not affect the $\overline{\text{ALERT}}$ / TACH pin.

In either mode, setting the individual channel mask bits will block the appropriate channel from asserting the $\overline{\text{ALERT}}$ / TACH pin.

5.5 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. The change in forward bias voltage is proportional to absolute temperature (T).

$$\Delta V_{BE} = V_{BE\_HIGH} - V_{BE\_LOW} = \frac{\eta k T}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \quad \textbf{Eq: [1]}$$

Where:

k = Boltzmann's constant

T = Absolute Temperature in Kelvin

q = electron charge

η = Diode Ideality Factor

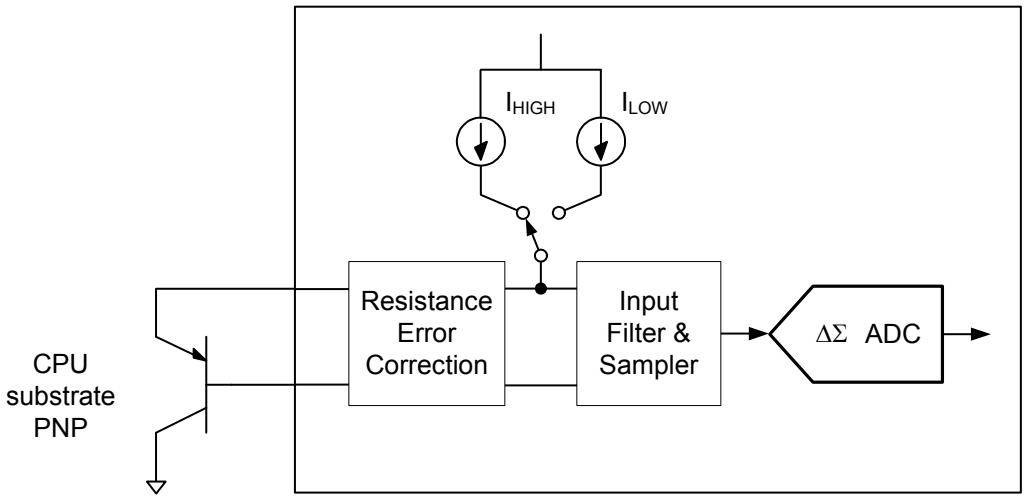

Figure 5.3 Block Diagram of Temperature Monitoring Circuit

Figure 5.3 shows a block diagram of the temperature measurement circuit. As shown, the EMC2101 incorporates a delta-sigma analog to digital converter that integrates the temperature diode voltage from multiple bias currents.

The external temperature diodes can be connected as shown in Figure 5.4.

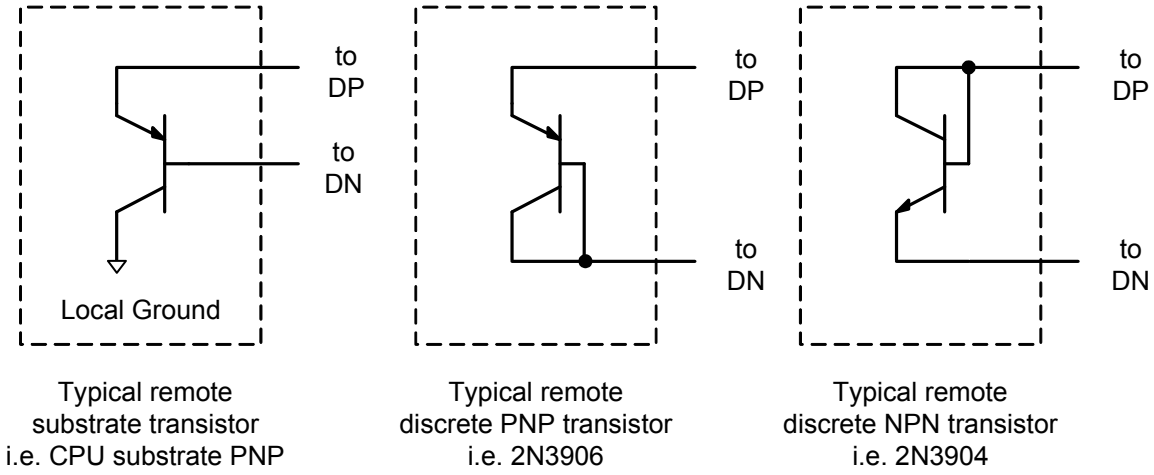

Figure 5.4 External Diode configurations

5.5.1 Temperature Measurement Results and Data

The results of the internal and external temperature measurements are stored in the internal and external temperature registers respectively. These are then compared with the values stored in the High Limit Registers. The internal temperature measurements are stored in 8-bit format while the external temperature measurements are stored in 11-bit format.

The EMC2101 measures temperatures from -64°C to 127°C represented as a binary two's complement number. Internal temperatures are in 1°C steps, external temperatures are in 0.125°C steps.

Table 5.2 shows the temperature format for the external diode and Table 5.3 shows the temperature format for the internal diode.

Table 5.2 EMC2101 External Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)
<= -64	1 1 0 0 0 0 0 0 0 0 0
-55	1 1 0 0 1 0 0 1 0 0 0
-1	1 1 1 1 1 1 1 1 0 0 0
-0.125	1 1 1 1 1 1 1 1 1 1 1
0	0 0 0 0 0 0 0 0 0 0 0
0.125	0 0 0 0 0 0 0 0 0 0 1
1	0 0 0 0 0 0 0 1 0 0 0
25	0 0 0 1 1 0 0 1 0 0 0
125	0 1 1 1 1 1 0 1 0 0 0
>= 127.875	0 1 1 1 1 1 1 1 1 1 0
Diode Fault (Open condition)	0 1 1 1 1 1 1 1 0 0 0
Diode Fault (Short condition)	0 1 1 1 1 1 1 1 1 1 1

Table 5.3 EMC2101 Internal Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)
<= -64	1 1 0 0 0 0 0 0
-55	1 1 0 0 1 0 0 1
-1	1 1 1 1 1 1 1 1
0	0 0 0 0 0 0 0 0
1	0 0 0 0 0 0 0 1
25	0 0 0 1 1 0 0 1
125	0 1 1 1 1 1 0 1
126	0 1 1 1 1 1 1 0
>= 127	0 1 1 1 1 1 1 1

5.5.2 Temperature Filter

The EMC2101 contains variable filtering options to suppress thermally or electrically noisy signals on the External Diode lines. This filter can be configured as Level 1, Level 2, or Disabled (see Section 6.23). The typical filter performance is shown in Figure 5.5 and Figure 5.6.

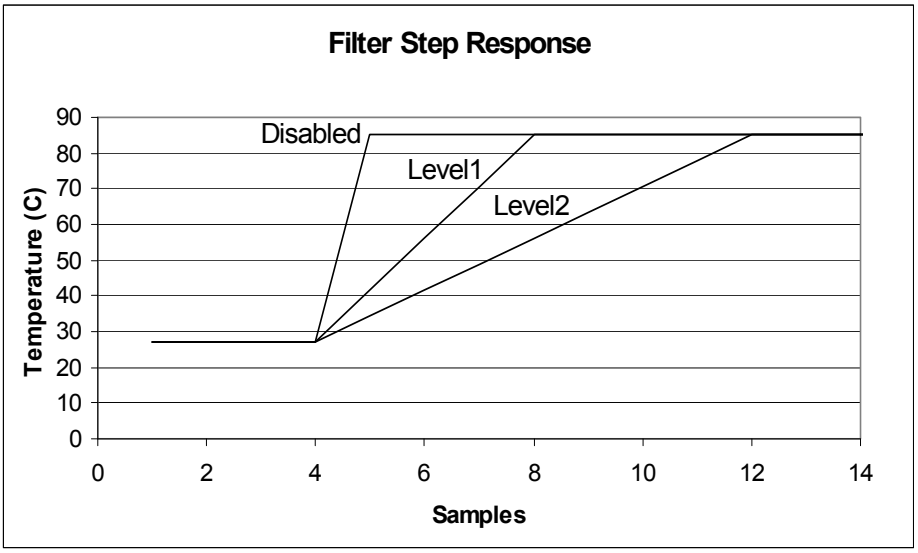

Figure 5.5 Temperature Filter Step Response

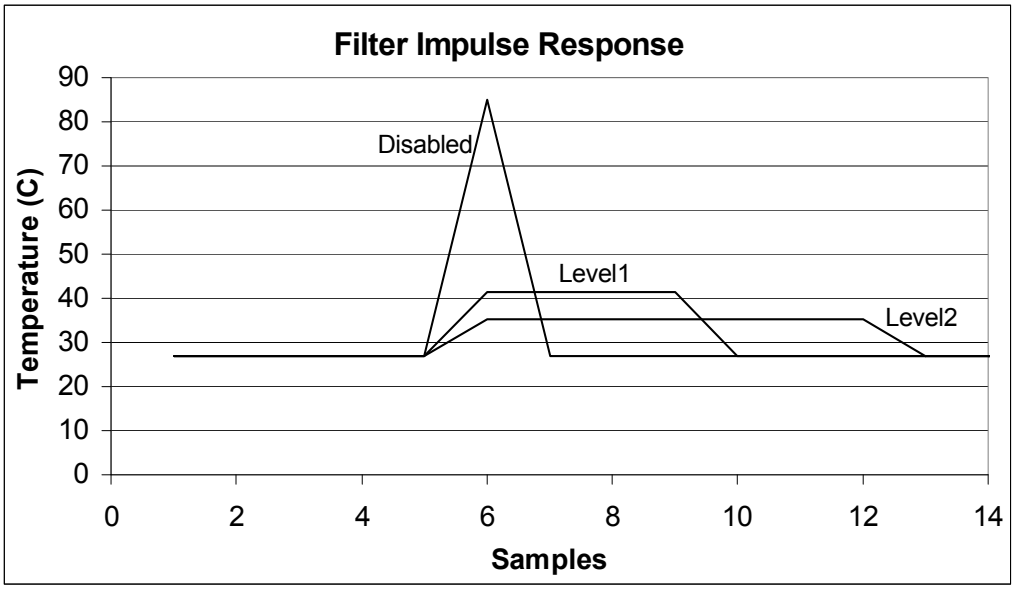

Figure 5.6 Temperature Filter Impulse Response