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EMC2102

RPM-Based Fan Controller with HW Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2102 is an SMBus, closed-loop, RPM-based fan controller/driver with hardware (HW) thermal shutdown and reset controller. The EMC2102 is packaged in a thermally enhanced, compact, 5x5, 28-pin lead-free RoHS compliant QFN package.

The EMC2102 utilizes Beta Compensation (an implementation of the BJT or transistor model for thermal diodes) and Resistance Error Correction (REC) to accurately monitor three external temperature zones. These features allow great accuracy for CPU substrate thermal diodes on multiple process geometries as well as with discrete diode-connected transistors. Both Beta Compensation and REC can be disabled on the EMC2102 to maintain accuracy when monitoring AMD thermal diodes.

The EMC2102 includes a closed-loop RPM based Fan Control Algorithm that integrates a linear fan driver capable of sourcing 600mA of current. The fan control algorithm is designed to work with fans that operate up to 16,000 RPMs.

The EMC2102 provides a stand-alone HW thermal shutdown block. The HW thermal shutdown logic can be configured for a few common configurations based on the strapping level of the SHDN_SEL pin on the PCB. The HW thermal shutdown point can be set in 1°C increments by using a discrete resistor divider implemented on the TRIP_SET pin.

The EMC2102 also provides 5V supply 'power good' function with a threshold of 4.5V. This function is provided on the RESET# pin.

Features

- Designed to support 45nm, 65nm, and 90nm CPU Diodes
- Supports BJT and transistor models for diode channels
- Closed-Loop RPM Based Fan Controller
  - Accepts External Clock Source To Achieve 2% Accuracy
- Integrated Linear Fan Driver
  - 600mA Drive Capability
- HW Thermal Shutdown (SYS_SHDN#)
  - 1°C Incremental Set Points For Thermal Shutdown
  - Cannot be disabled by software
- Provides Reset Function (RESET#) On 5V Supply
- Three Remote Thermal Zones
  - ±1°C Accuracy (60°C to 100°C)
  - 1°C Resolution
- Resistance Error Correction On Thermal Diode Channels
  - Eliminates Temperature Offset Due To Series Resistance From PCB Traces And Thermal 'Diode'
- Thermally Enhanced, 28-pin, 5x5 QFN Lead-free RoHS Compliant Package
- Operates From Single 3.0 - 3.6V Supply
  - 5V Supply For Linear Fan Driver
- Software Configurable ALERT# Signal For Diode Fault, Fan Stall Or System Warning

Applications

- Notebook Computers
- Desktop Computers
- Embedded Applications

ORDER NUMBER:

EMC2102-DZK FOR 28-PIN QFN LEAD-FREE ROHS COMPLIANT PACKAGE (ADDRESS - 011_1101)

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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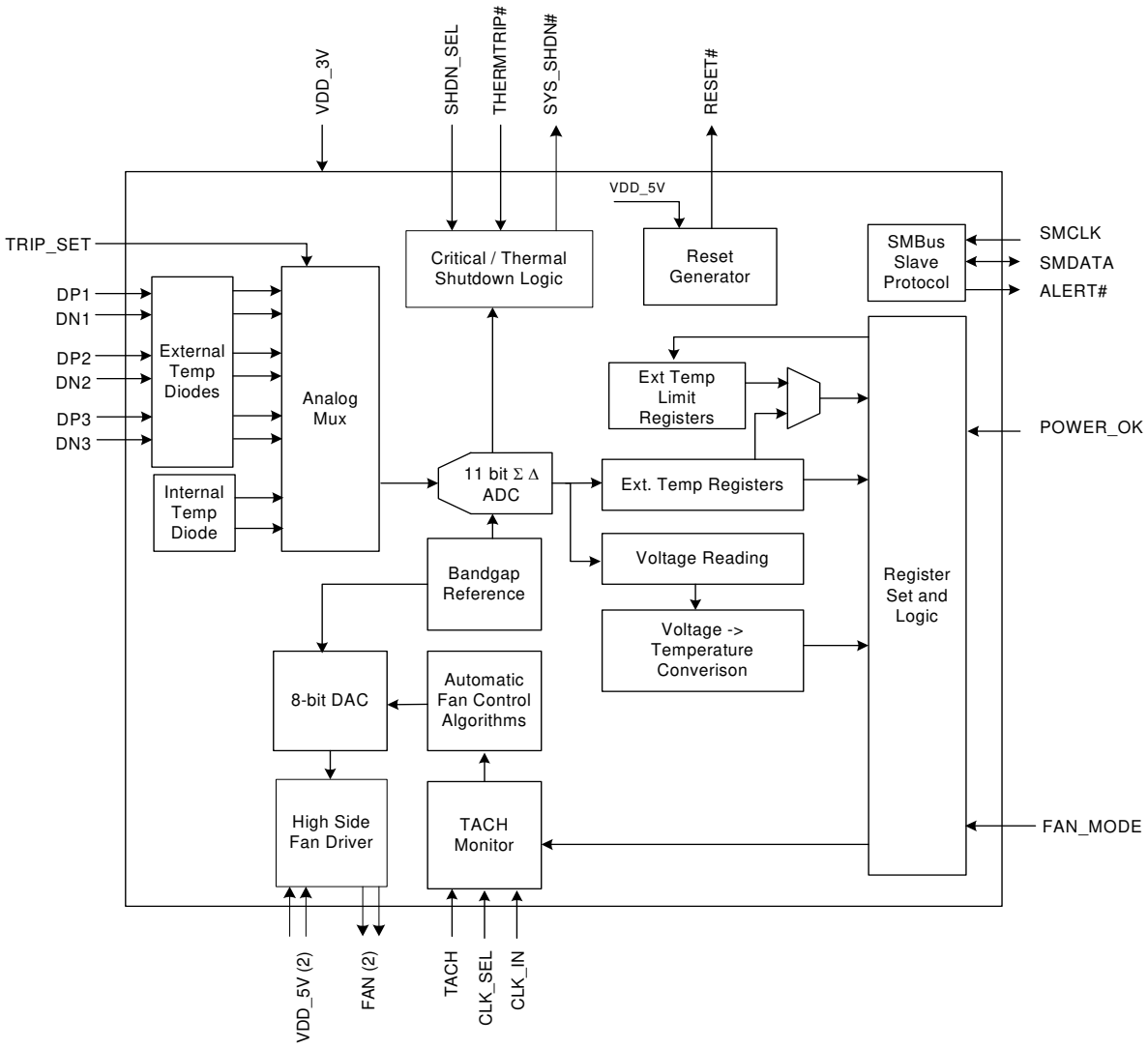

Figure 1.1 EMC2102 Block Diagram

Chapter 2 Pinout

2.1 Pin Layout for EMC2102

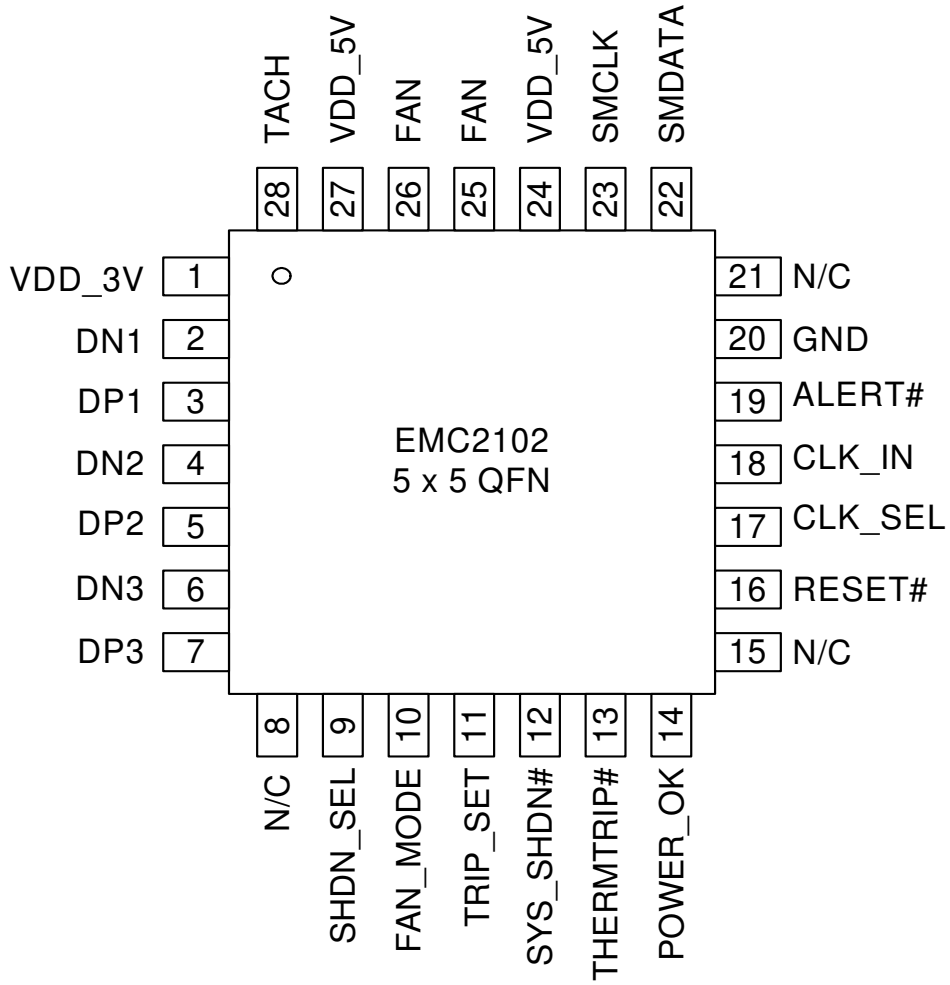

Figure 2.1 EMC2102 Pin Diagram

2.2 Pin Description for EMC2102

Table 2.1 Pin Description

PIN	NAME	FUNCTION	TYPE
1	VDD_3V	Supply Connection of 3.3V.	Power
2	DN1	Negative (cathode) Analog Input for External Diode 1.	AIO
3	DP1	Positive (anode) Analog Input for External Diode 1.	AIO
4	DN2	Negative (cathode) Analog Input for External Diode 2.	AIO
5	DP2	Positive (anode) Analog Input for External Diode 2.	AIO
6	DN3	Negative (cathode) Analog Input for External Diode 3.	AIO
7	DP3	Positive (anode) Analog Input for External Diode 3.	AIO
8	N/C	Not internally connected.	N/A
9	SHDN_SEL	Determines HW Shutdown temperature channel (see Table 5.4, "SHDN_SEL Pin Configuration".)	DIT
10	FAN_MODE	Selects power-up default for fan drive setting.	DIT
11	TRIP_SET	Voltage input to determine HW Shutdown threshold temperature	AI
12	SYS_SHDN#	Active low Critical System Shutdown output	OD (5V)
13	THERMTRIP#	Active low Critical temperature limit signal from the CPU or chipset.	IP
14	POWER_OK	Active high power good input.	DI (5V)
15	N/C	Not internally connected.	N/A
16	RESET#	Active low reset output.	DO
17	CLK_SEL	Selects internal oscillator or external clock.	DI (5V)
18	CLK_IN	32.768KHz clock input.	DI (5V)
19	ALERT#	Active low interrupt.	OD (5V)
20	GND	GND connection.	Power
21	N/C	Not internally connected.	N/A
22	SMDATA	SMBus data input/output.	DIOD (5V) - requires external upll-up resistor
23	SMCLK	SMBus clock input.	DI (5V) - requires external pull-up resistor

Table 2.1 Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
24	VDD_5V	5V supply input for the linear fan driver. Both VDD_5V pins should be connected to same 5V supply.	Power
25	FAN	Linear fan drive signal. Both FAN pins should be connected together.	AO
26	FAN	Linear fan drive signal. Both FAN pins should be connected together.	AO
27	VDD_5V	5V supply input for the linear fan driver. Both VDD_5V pins should be connected to same 5V supply.	Power
28	TACH	Input from the tachometer pin of the fan.	DI (5V)

The pin type are described in detail below. All pins labelled with (5V) are 5V tolerant.:

Power - this pin is used to supply power to the device.

DI - Digital Input - this pin is used as a digital input. This pin is 5V tolerant.

AI - Analog Input - this pin is used as an input for analog signals.

AO - Analog Output - this pin is used as an output for analog signals.

AIO - Analog Input / Output - this pin is used as an I/O for analog signals.

DO - Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current and doesn't require a pull-up resistor.

DIOD - Open Drain Digital Input / Output - this pin is used as an digital I/O. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

OD - Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor.

DIT - Tri-stated Digital Input - this pin is a digital input that supports 3 logic levels at the input: logic high, logic low, or high impedance (open).

IP - Digital Input - this pin has an internal 30uA pull-up current to VDD_3V.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Voltage on VDD_5V Pins and 5V tolerant pins (see Table 2.1, "Pin Description")	-0.3 to 6.5	V
Voltage on VDD_3V pin	-0.3 to 4	V
Voltage on FAN pins	-0.3 to VDD_5V + 0.3	V
Voltage on any other pin to GND	-0.3 to VDD_3V + 0.3	V
Package Power Dissipation	0.9 up to T_A = 85°C Note 3.2	W
Junction to Ambient (θ_{JA}) Note 3.3	37	°C/W
Operating Ambient Temperature Range	0 to 85	°C
Operating Die Temperature Range	0 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

These ratings are absolute maximum values. Exceeding these values or operating at these values for an extended period of time may cause permanent damage to the device.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a thermal via design consisting of four 20mil vias connected to the ground plane with a 3.1mm x 3.1mm thermal landing.

Note 3.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
3.3V Supply Voltage	V_{DD_3V}	3	3.3	3.6	V	
5V Supply Voltage	V_{DD_5V}	4.6	5	5.5	V	
Supply Current from VDD_3V pin	I_{DD3}		500	750	uA	Fan Driver enabled
Supply Current from VDD_5V pin	I_{DD5}		200		uA	Fan Driver enabled

Table 3.2 Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
External Temperature Monitors						
Temperature Accuracy			±1	±1.5	°C	60°C < T_{DIODE} < 100°C 30°C < T_{DIE} < 85°C (Note 3.4)
			±1	±3	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{DIE} < 115°C (Note 3.4)
Temperature Resolution			1		°C	
Diode decoupling capacitor	C_{FILTER}			2200	pF	Connected across external 2N3904 diode or AMD diode (Note 3.5)
				470	pF	Connected across CPU or GPU thermal diode (Note 3.5)
Resistance Error Corrected	R_{SERIES}			100	Ohm	Series resistance in DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy			±3		°C	(Note 3.4)
Temperature Resolution			1		°C	
Reset Generator						
Reset Voltage	V_{RESET}	4.3	4.4	4.5	V	V_{DD_5V} rising edge 3V < V_{DD_3V} < 3.6V
Hysteresis	ΔV_{RESET}		100		mV	
Time Delay	t_{RESET}		220		ms	
High Side Fan Driver						
Output High Voltage from 5V supply	V_{OH_5V}			VDD_5 V - 0.4	V	I_{SOURCE} = 600mA, VDD_5V = 5V
Fan Drive Current	I_{SOURCE}			600	mA	
Overcurrent Limit	I_{OVER}		1500		mA	Momentary Current drive at startup for < 2 seconds
DC Short Circuit Current Limit	I_{SHORT}		800		mA	Sourcing current, Thermal shutdown not triggered, FAN_OUT = 0V
Short circuit delay	t_{DFS}		2		s	
Output Capacitive Load	C_{LOAD}			100	uF	
ESR on C_{LOAD}	R_{ESR}	0		2	Ohm	
RPM Based Fan Controller						

Table 3.2 Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
TACH Range	TACH	480		16000	RPM	
TACH Setting Accuracy	Δ_{TACH}		±1	±2	%	External oscillator 32.768kHz
	Δ_{TACH}		±5	±7.5	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Thermal Shutdown						
Thermal Shutdown Threshold	TSD_{TH}		150		°C	
Thermal Shutdown Hysteresis	TSD_{HYST}		50		°C	
SMBus and Digital I/O pins						
Output High Voltage	V_{OH}	VDD _3V 0.4			V	2 mA current drive
Output Low Voltage	V_{OL}			0.5	V	4mA current sink

Note 3.4 T_{DIE} refers to the internal die temperature and may not match T_A due to self heating of the device. The internal temperature sensor will return T_{DIE}.

Note 3.5 Contact SMSC for Application Notes and guidelines when measuring GPU processor diodes and CPU processor diodes.

3.3 SMBus Electrical Specifications

Table 3.3 SMBus Electrical Specifications

VDD_3V = 3V to 3.6V, VDD_5V = 4.6 to 5.5V, T_A = 0°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			4		mA	SMDATA = 0.5V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	

Table 3.3 SMBus Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6 to 5.5V, T_A = 0°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

The EMC2102 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2102 will not stretch the clock signal.

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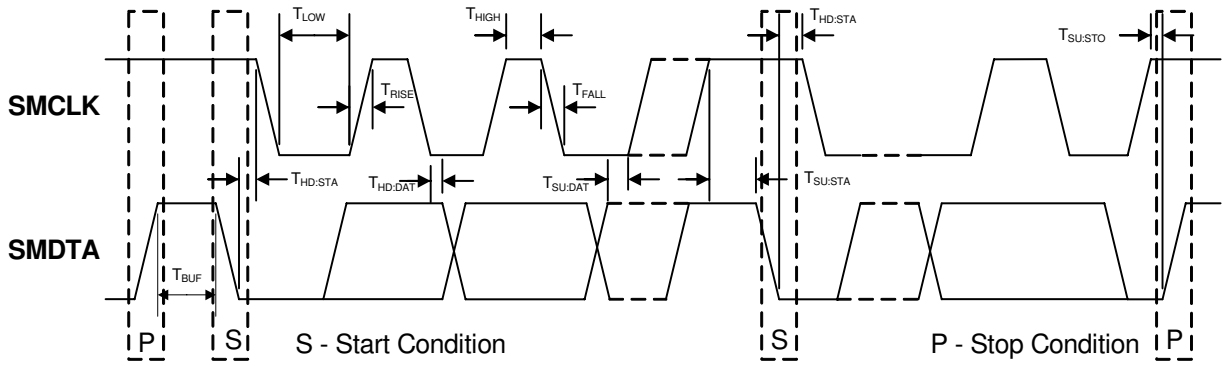

Figure 4.1 SMBus Timing Diagram

The EMC2102 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and Write Byte as valid protocols as shown below. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

4.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	W R	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

4.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1	7	1	1	8	1	1

4.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1	7	1	1	8	1	1

4.5 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an $\overline{\text{SMBALERT}}$.

When it detects that the $\overline{\text{SMBALERT}}$ pin is asserted, the host will send the Alert Response Address (general address of 000_1100b) on the bus. All devices with active interrupts will respond with their client address as shown in Table 4.6.

..

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1	7	1	1	8	1	1

The EMC2102 will respond to the ARA command if the ALERT# pin has been asserted but will not immediately release the ALERT# pin. The ALERT# pin is released under the following conditions.

1. The Interrupt Status Registers are read and the error condition has been removed.
2. The specific error condition is masked from asserting the ALERT# pin.

4.6 SMBus Address

The EMC2102-1 is addressed on the SMBus as 011_1101b.

Attempting to communicate with the EMC2102 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.7 SMBus Time-out

The EMC2102 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

Chapter 5 General Description

The EMC2102 monitors three external temperature channels. Two of the external temperature channels can employ both Beta Compensation (an implementation of the BJT or transistor model for thermal diodes) and Resistance Error Correction for use with thermal diodes while the third channel is hardwired to measure a discrete diode connected NPN or PNP transistor. The temperature data is available over a standard 2-wire serial interface using SMBus read commands. The temperature monitoring is described in more detail in Section 5.1, "Temperature Monitoring".

The EMC2102 integrates a closed-loop RPM based Fan Control Algorithm. A host writes the desired fan speed into a register of the EMC2102 via the SMBus and the integrated fan controller will maintain the fan at the desired speed using fan speed feedback from the TACH output from a 3-wire fan. The fan control algorithm controls an integrated 5V, 600mA, linear fan driver. The fan control algorithm functionality is described in more detail in Section 5.3, "RPM based Fan Control Algorithm"

The EMC2102 provides the system with a hardware based critical/thermal shutdown function. This critical/thermal shutdown function integrates critical signals from both the CPU and power supply and the analog circuitry to monitor a specific temperature channel based on the system configuration. The critical/thermal shutdown temperature threshold is configured on the PCB through a simple discrete resistor divider. The Critical/Thermal Shutdown function is described in more detail in Section 5.7, "Critical/Thermal Shutdown".

An example of a typical system configuration for the EMC2102 is provided in Figure 5.1.

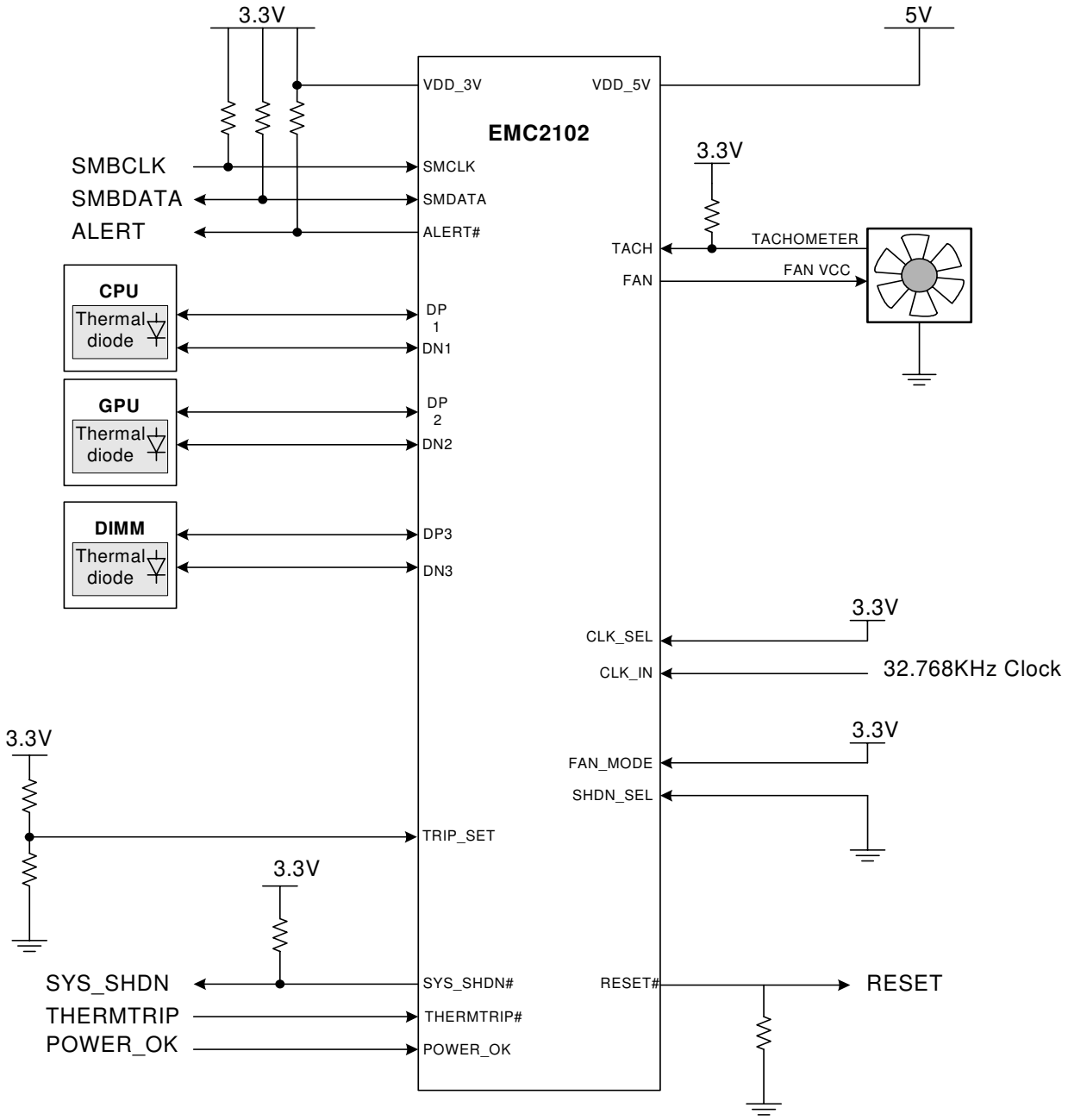

Figure 5.1 EMC2102 System Diagram

5.1 Temperature Monitoring

External diode channels one and two can be configured to monitor either discrete thermal diodes or a CPU / GPU thermal diode. External diode channel three is always configured to monitor a discrete diode-connected transistor (such as a 2N3904) or an AMD thermal diode. Each channel can enable the Resistance Error Correction functionality and external diode channels one and two can adjust the Beta Compensation settings (disabling it if desired). The disabling of these features is only recommended in two situations:

1. An AMD thermal diode is being monitored. The AMD thermal diode is physically a 2-terminal diode and will not function with either Beta Compensation or Resistance Error Correction. Because of this, when an EMC2102 temperature channel is interfacing an AMD thermal diode, both Beta Compensation and Resistance Error Correction must be disabled.
2. A discrete diode connected transistor (such as 2N3904) is used. In this configuration, Beta Compensation must be disabled, but Resistance Error Correction should remain enabled.

5.1.1 Resistance Error Correction

The EMC2102 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of parasitic resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC2102 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

5.1.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. This correction is done by implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC2102 corrects for this beta variation to eliminate any error which would normally be induced.

5.1.3 Fault Queue

To avoid spurious interrupts and Critical/Thermal Trip events induced by thermal spikes and noise injection, the selected Thermal / Critical Shutdown Temperature channel (see Section 5.7.2) is filtered through a fault queue. This fault queue requires that a user-defined number of consecutive out-of-limit errors be recorded before it will cause an interrupt or trigger the Critical/Thermal trip event.

The fault queue only applies to the measurement channels that will cause the SYS_SHDN# pin to be asserted including any software configured channels (see Section 5.7). In addition, the fault queue applies to all enabled channels simultaneously and will trigger the SYS_SHDN# pin if there are the desired number of consecutive measurements with any or all channels exceeding their corresponding limits.

5.2 Fan Control Modes of Operation

The EMC2102 has two modes of operation for the High Side Fan Driver. They are:

1. Manual Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 6.12) will instantly update the fan drive.

- The Manual Mode is enabled by clearing the EN bit in the Fan Configuration Register (see Section 6.13).
- Whenever the Manual Mode is enabled the current drive will be changed to what was last written into the Fan Driver Setting Register.
- Setting the drive value to 00h will disable the High Side Fan Driver for lower power operation.

2. Using RPM based Fan Control Algorithm - in this mode of operation, the user determines a target TACH count and the drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.

Table 5.1 Fan Controls Active for Operating Mode

MANUAL MODE	ALGORITHM
Fan Driver Setting (read / write)	Fan Driver Setting (read only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)
-	UPDATE[2:0] (Fan Configuration)
-	LEVEL (Spin Up Configuration)
-	SPINUP_TIME[1:0] (Spin Up Configuration)
-	Fan Step
-	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
-	TACH Target
TACH Reading	TACH Reading

5.3 RPM based Fan Control Algorithm

The EMC2102 includes a RPM based Fan Control Algorithm that controls an integrated linear High Side Fan Driver. This fan control algorithm automatically approaches and maintains the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source. Figure 5.2, "RPM based Fan Control Algorithm" shows a simple flow diagram of the RPM based Fan Control Algorithm operation.

The desired TACH count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000RPMs, then the user would input the hexidecimal equivalent of 655 (29h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs (see Equation [4] in Section 6.19).

The EMC2102's RPM based Fan Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the ALERT# pin. The EMC2102 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal. The fan controller will function either with an externally supplied 32.768KHz clock source or with it's own internal 32.768KHz oscillator depending on the required accuracy.

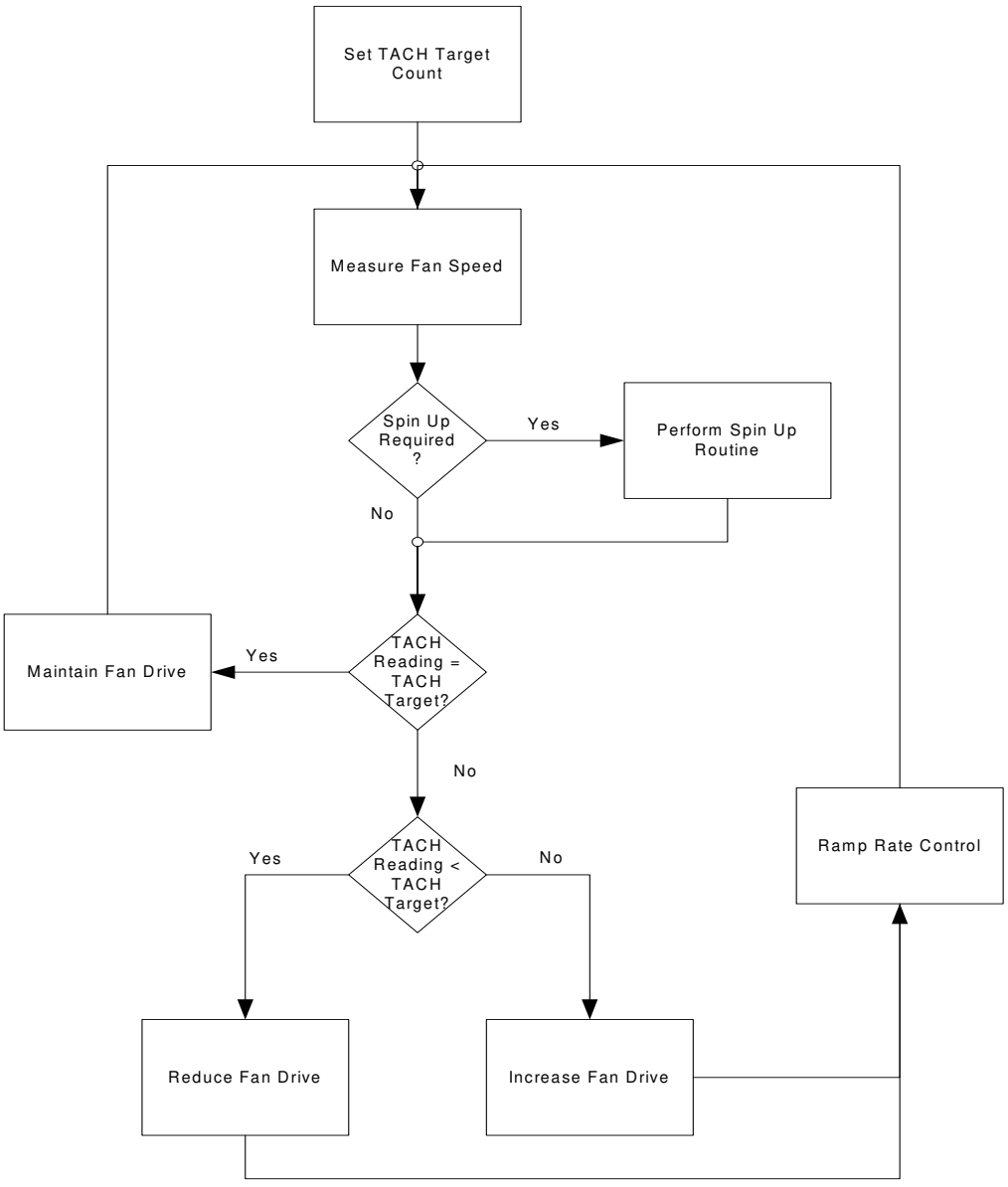

Figure 5.2 RPM based Fan Control Algorithm

5.3.1 Programming the RPM based Fan Control Algorithm

The RPM based Fan Control Algorithm powers-up enabled and active. The following registers control the algorithm. The EMC2102 fan control registers are preloaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

1. Set the Valid TACH Count Register to the minimum TACH count that indicates the fan is spinning.
2. Set the Spin Up Configuration Register to the spin up level and Spin Time desired.
3. Set the Fan Step Register to the desired step size.
4. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
5. Set the Update Time, and Edges options in the Fan Configuration Register.
6. Set the TACH Target Register to the desired TACH count.

5.3.2 TACH Measurement

In both modes of operation, the TACH measurement will work normally. Any TACH count that is higher than the Valid TACH Count (see Section 6.17) will flag a stalled fan and trigger an interrupt.

The EMC2102 includes a TACH measurement circuit. The TACH signal must be valid at all times to ensure proper operation. The TACH measurement circuitry is programmable to detect the fan speed of a variety of fan configurations and architectures including 1-pole, 2-pole (default), 3-pole, and 4-pole fans.

APPLICATION NOTE: The TACH measurement works independently of the drive settings. If the device is put into manual mode and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the TACH measurement may signal a Stalled Fan condition and assert an interrupt.

5.3.2.1 Stalled Fan

If the TACH counter exceeds the user-programmable Valid TACH Count setting then it will flag the fan as stalled and trigger an interrupt. If the RPM based Fan Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid TACH level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Manual Mode is enabled, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 6.21, "Spin Time") to allow the fan opportunity to reach a valid speed without generating unnecessary interrupts.
- In Manual Mode, whenever the drive value is changed from 00h, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time to allow the fan opportunity to reach a valid speed without generating unnecessary interrupts.
- In Manual Mode, whenever the TACH count exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When the RPM based Fan Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

5.3.3 Spin Up Routine

The EMC2102 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation. During Manual Mode, the Spin Up Routine will not control the fan drive settings under any conditions.

When the RPM based Fan Control Algorithm is running, the Spin Up Routine is initiated under the following conditions:

APPLICATION NOTE: When the device is operating in manual mode, the FAN_SPIN status bit may be set if the fan drive is set at a level that is lower than the fan can operate (including zero drive). If the FAN_SPIN interrupt is unmasked, then this condition will trigger an errant interrupt.

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 6.18, "TACH Target Register" and Section 6.17, "Valid TACH Count Register").
2. At power-up if the FAN_MODE setting is '1' or 'open' indicating 75% drive or 60% drive respectively. If the FAN_MODE setting is '0' indicating 0% drive, then the Spin Up Routine is not initiated until another condition is met.
3. The RPM based Fan Control Algorithm is started and the FAN_MODE setting is '0' indicating 0% drive prior to algorithm control.
4. The RPM based Fan Control Algorithm's measured TACH count is greater than the Valid TACH Count.

When the Spin Up Routine is operating, the fan driver is set to full scale for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (60% or 75% drive).

After the Spin Up Routine has finished, the EMC2102 measures the TACH. If the measured TACH count is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 5.3 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

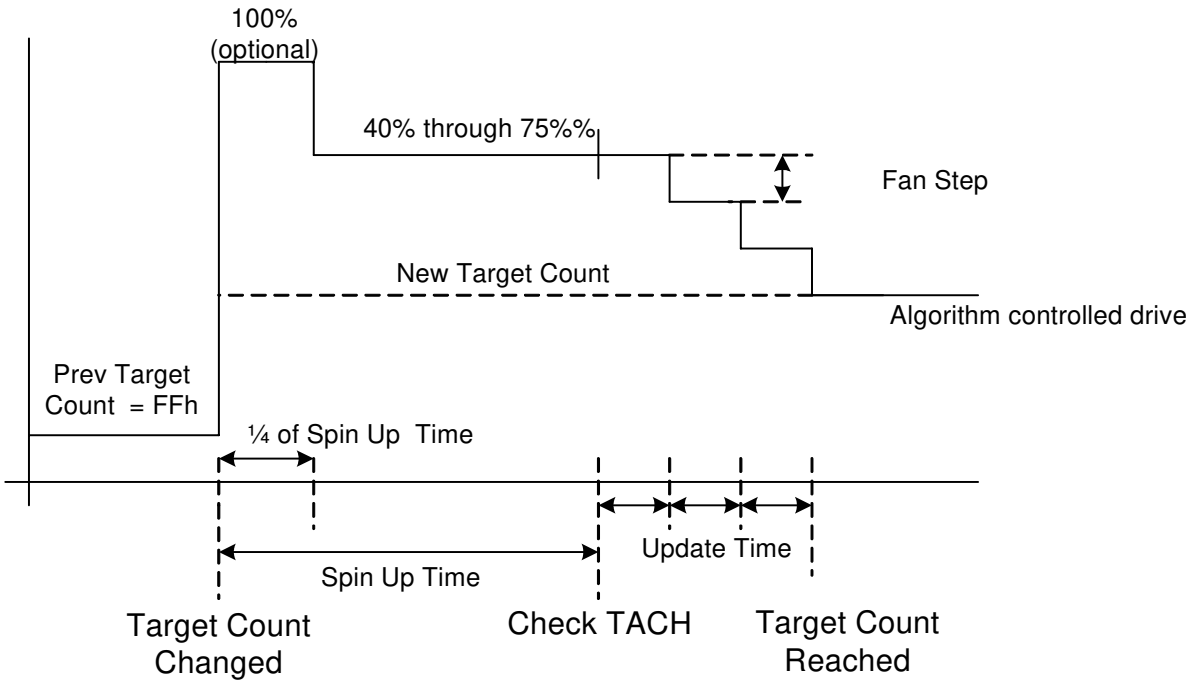

Figure 5.3 Spin Up Routine

5.3.4 FAN_MODE Pin

The FAN_MODE pin is used to determine the fan driver output levels at power-up before the EMC2102 has been programmed. After power-up, the fan driver will be set at the selected drive until the RPM based Fan Control Algorithm is started or disabled.

The level on the pin determines the function as shown in Table 5.2, "FAN_MODE Pin Functions".

Table 5.2 FAN_MODE Pin Functions

FAN_MODE	FUNCTION
0	Fan Driver set at 0% drive
open	Fan Driver set at 60% drive after Spin Up Routine
1	Fan Driver set at 75% drive after Spin Up Routine

5.3.5 32.768KHz Clock Source

The EMC2102 allows the user to choose between supplying an external 32.768KHz clock or use of the internal 32.768KHz oscillator to measure the TACH signal. This clock source is used by the RPM based Fan Control Algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

To enable the external clock source, the CLK_SEL pin must be pulled to VDD_3V at power-up (see Table 5.3). The CLK_SEL pin is must be in a known state at all times (either pulled high or pulled low) and is latched upon power-up.

Table 5.3 CLK_SEL Pin Functions

CLK_SEL	FUNCTION
0	Internal oscillator used
1	External clock used

5.4 Watchdog Timer

The EMC2102 contains an internal Watchdog Timer. Once the device has powered up the watchdog timer monitors the bus traffic for signs of activity. The Watchdog Timer starts when the VDD_5V supply has reached its operating point. The Watchdog Timer only starts immediately after power-up and once it has been triggered or deactivated will not restart.

If four (4) seconds elapse without the system host programming the device, then the following will occur:

1. The WATCH status bit will be set.
2. The High Side Fan Driver will be set to full scale drive. It will remain at full scale drive until one of the two conditions listed below are met.

If the Watchdog Timer is triggered, the following two operations will disable the timer and return the device to normal operation.

1. Writing the RPM based Fan Control Algorithm TACH Target Register will disable the Watchdog Timer regardless of the value. If a value is written that is greater than the Valid TACH Count Register setting (other than FFh), the fan drive setting will be set based on the FAN_MODE pin