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EMC2104

Dual RPM-Based PWM Fan Controller with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2104 is an SMBus compliant fan controller with up to five (up to 4 external and 1 internal) temperature channels. The fan drivers can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors.

The EMC2104 also includes a hardware programmable temperature limits and dedicated system shutdown output for thermal protection of critical circuitry.

Applications

- Notebook Computers
- Embedded Applications
- Projectors
- Industrial and Networking Equipment

Features

- Two Programmable Fan Control circuits
  - 4-wire fan compatible
  - High speed PWM (26khz)
  - Low speed PWM (9.5Hz - 2240Hz)
  - Optional detection of aging fans
- RPM based fan control algorithm
  - 2% accuracy from 500RPM to 16k RPM
- Temperature Look-Up Table
  - Allows programmed fan response to temperature
  - 1 to 4 thermal zones to control each fan driver
  - Controls fan speed or drive setting
  - Allows externally generated temperature data to control fan drivers including two DTS channels
- Up to Four External Temperature Channels
  - Designed to support 45nm, 60nm, and 90nm CPUs
  - Automatically detects and supports CPUs requiring the BJT or Transistor models
  - Resistance error correction
  - 1°C accurate (60°C to 100°C)
  - 0.125°C resolution
  - Detects fan aging and variation
- Up to three thermistor compatible voltage inputs
- Hardware Programmable Thermal Shutdown Temperature
  - Cannot be altered by software
  - 60°C to 122°C Range or 92°C to 154°C Range
- Programmable High and Low Limits for all channels
- 3.3V Supply Voltage
- SMBus 2.0 Compliant
  - SMBus Alert compatible
- Available in 20-pin QFN Package - Lead Free RoHS compliant (4mm x 4mm)

Order Number(s):

ORDERING NUMBER	PACKAGE	FEATURES
EMC2104-BP-TR	20 pin QFN Lead-Free RoHS compliant	Two PWM fan drivers, up to 4 external diode measurement channels, one Critical / Thermal Shutdown inputs.

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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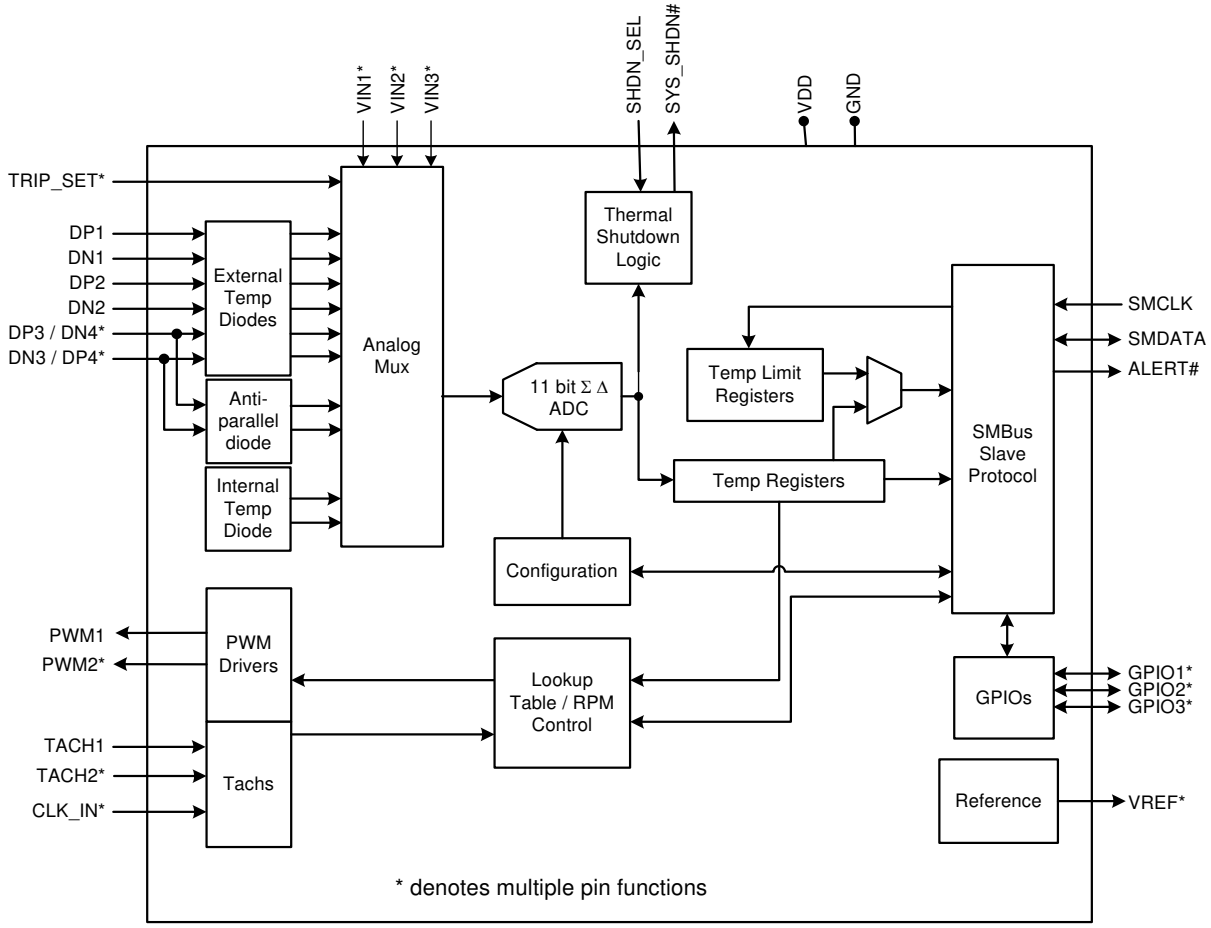

Figure 1.1 EMC2104 Block Diagram

Chapter 2 Pin Description

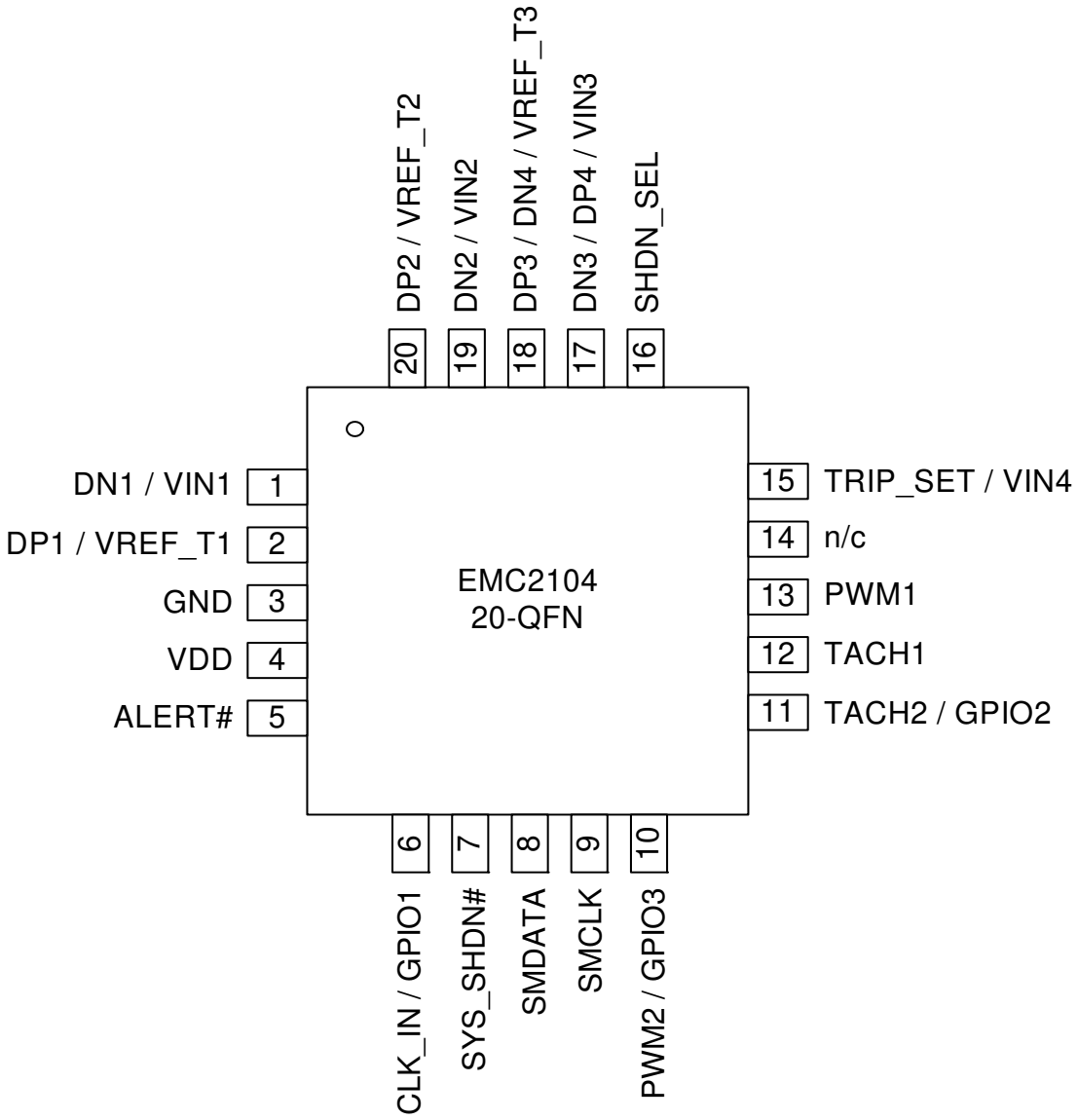

Figure 2.1 EMC2104 Pin Diagram (20 Pin QFN)

Table 2.1 Pin Description for EMC2104

PIN NUMBER EMC2104	PIN NAME	PIN FUNCTION	PIN TYPE
1	DN1 / VIN1	DN1 - Negative (cathode) analog input for External Diode 1 (default)	AIO (2V)
		VIN1 - General voltage input for use with a thermistor	AI (2V)
2	DP1 / VREF_T1	DP1 - Positive (anode) analog input for External Diode 1 (default)	AIO (2V)
		VREF_T1 - Reference output for use with a thermistor and to drive VIN1	AO (2V)
3	GND	Ground connection	Power
4	VDD	Power Supply	Power
5	ALERT#	Active low interrupt - requires external pull-up resistor.	OD (5V)
6	CLK_IN / GPIO1	CLK_IN - 32.768KHz clock input.	DI (5V)
		GPI1 - General Purpose Input (default)	DI (5V)
		GPO1 - General Purpose push/ pull Output	DI (5V)
		GPO1 - General Purpose open drain Output.	DI (5V)
7	SYS_SHDN#	Active low Critical System Shutdown output	OD (5V)
8	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
9	SMCLK	SMBus clock input - requires external pull-up resistor	DIOD (5V)
10	PWM2 / GPIO3	PWM2 - Open Drain PWM drive output for Fan 2 (default)	OD (5V)
		PWM2 - Push-Pull PWM drive output for Fan 2	DO
		GPI3 - General Purpose Input (software programmed)	DI (5V)
		GPO3 - General Purpose push-pull Output	DO
		GPO3 - General Purpose open drain Output	OD (5V)

Table 2.1 Pin Description for EMC2104 (continued)

PIN NUMBER EMC2104	PIN NAME	PIN FUNCTION	PIN TYPE
11	TACH2 / GPIO2	TACH2 - Tachometer input for Fan 2 (default)	DI (5V)
		GPI2 - General Purpose Input	DI (5V)
		GPO2 - General Purpose push-pull Output	DO
		GPO2 - General Purpose open drain Output	OD (5V)
12	TACH1	Tachometer input for Fan 1	DI (5V)
13	PWM1	PWM1 - Open Drain PWM drive output for Fan 1 (default)	OD (5V)
		PWM1 - Push-Pull PWM drive output for Fan 1	DO
14	n/c	Not Internally Connected	N/A
15	TRIP_SET / VIN4	TRIP_SET - Determines HW Shutdown temperature features for the hardware shutdown channel	AI (2V)
		VIN4 - General voltage input when Thermal / Critical shutdown disabled	AI (2V)
16	SHDN_SEL	Determines HW Shutdown temperature features and measurement channel	AIO
17	DN3 / DP4 / VIN3	DN3 / DP4 - Negative (cathode) analog input for External Diode 3 and positive (anode) Analog Input for External Diode 4 (default)	AIO (2V)
		VIN3 - General voltage input for use with a thermistor	AI (2V)
18	DP3 / DN4 / VREF_T3	DP3 / DN4 - Positive (anode) analog input for External Diode 3 and negative (cathode) analog input for External Diode 4 (default)	AIO (2V)
		VREF_T3 - Reference output for use with a thermistor and to drive VIN3	AO (2V)
19	DN2 / VIN2	DN2 - Negative (cathode) analog input for External Diode 2 (default)	AIO (2V)
		VIN2 - General voltage input for use with a thermistor	AI (2V)
20	DP2 / VREF_T2	DP2 - Positive (anode) analog input for External Diode 2 (default)	AIO (2V)
		VREF_T2 - Reference output for use with a thermistor and to drive VIN2	AO (2V)

The pin type are described in detail below. All pins labelled with (5V) are 5V tolerant.

All pin labelled with (2V) should not be exposed to any voltage level greater than 2V.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AI	Analog Input - this pin is used as an input for analog signals.
AO	Analog Output - this pin is used as an output for analog signals.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output this pin is used as an digital I/O. When it is used as an output, It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

Table 3.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins	-0.3 to 6.5	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on 2V tolerant pins	-0.3 to 2.5	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation See Note 3.1	1 up to T_A = 85°C	W
Junction to Ambient (θ_{JA}) See Note 3.2	40	°C/W
Operating Ambient Temperature Range	-40 to 85°C	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a recommended thermal via design consisting of four 12mil vias connected to the ground plane with a 2x2mm thermal landing.

3.1 Electrical Specifications

Table 3.2 Electrical Specifications

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current (active)	I_{DD}		2	3	mA	4 Conversions / second - Dynamic Averaging Enabled Fan Driver enabled at max PWM frequency
Supply Current	I_{DD}		500	750	uA	1 Conversions / second- Dynamic Averaging disabled, Fan Driver disabled.

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current from VDD_5V	I_{DD_5}		100		uA	Fan Driver enabled, No load current
SMBus Delay	t_{SMB}			15	ms	Delay from power to first SMBus communication
Time to First Round Robin				300	ms	
External Temperature Monitors						
Temperature Accuracy			±0.25	±1	°C	60°C < T_{DIODE} < 110°C 30°C < T_{DIE} < 85°C
			±0.5	±2	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{DIE} < 115°C
Temperature Resolution			0.125		°C	
Diode decoupling capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Resistance Error Corrected	R_{SERIES}			100	Ohm	Sum of series resistance in both DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy	T_{DIE}		±1	±2	°C	
Temperature Resolution			0.125		°C	
Voltage Measurement						
Total Unadjusted Error	TUE			1	%	Measured at 3/4 full scale
Reference Voltage	V_{REF}		800		mV	
Reference Accuracy	ΔV_{REF}		1		%	
PWM Fan Driver						
PWM Resolution	PWM		256		Steps	
PWM Duty Cycle	DUTY	0		100	%	
RPM Based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}		±1	±2	%	External oscillator 32.768kHz
	Δ_{TACH}		±2.5	±5	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Digital I/O pins						
Input High Voltage	V_{IH}	2.0			V	

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	4 mA current drive
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Leakage current	I_{LEAK}			±5	uA	$\overline{ALERT}$ and $\overline{SYS\_SHDN}$ pins Powered and unpowered

3.2 SMBus Electrical Specifications (client mode)

Table 3.3 SMBus Electrical Specifications

VDD= 3V to 3.6V, T_A = -40°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered and unpowered
Input Capacitance	C_{IN}		5		pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	

Table 3.3 SMBus Electrical Specifications (continued)

VDD= 3V to 3.6V, T_A = -40°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 Communications

4.1 System Management Bus Interface Protocol

The EMC2104 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2104 will not stretch the clock signal.

The EMC2104 powers up as an SMBus client.

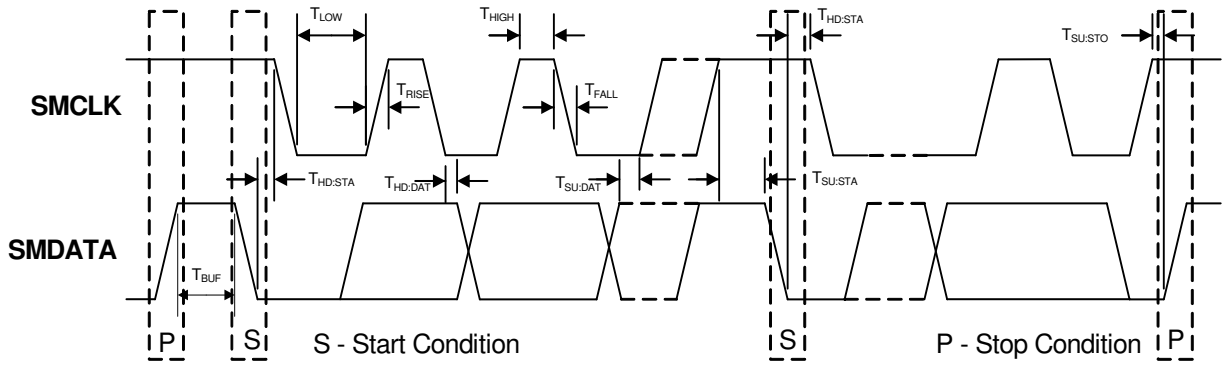

Figure 4.1 SMBus Timing Diagram

The EMC2104 contains a single SMBus interface. The EMC2104 client interfaces are SMBus 2.0 compatible and support Send Byte, Read Byte, Receive Byte and the Alert Response Address as valid protocols. These protocols are used as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
0 -> 1	0101_111	0	0	XXh	0	XXh	0	1 -> 0

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
0 -> 1	0101_111	0	0	XXh	0	0 -> 1	0101_111	1	0	XXh	1	1 -> 0

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
0 -> 1	0101_111	0	0	XXh	0	1 -> 0

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	0101_111	1	0	XXh	1	1 -> 0

4.6 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the ALERT# pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	0001_100	1	0	0101_111	1	1 -> 0

The EMC2104 will respond to the ARA in the following way if the ALERT# pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the ALERT# pin.

4.7 SMBus Address

The EMC2104 SMBus Address is fixed at 0101_111xb.

Attempting to communicate with the EMC2104 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.8 SMBus Time-out

The EMC2104 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface. The SMBus Timeout defaults to enabled and can be disabled by setting the DIS_TO bit in the Configuration 2 register.

Chapter 5 Product Description

The EMC2104 is an SMBus compliant fan controller with up to five (up to 4 external and 1 internal) temperature channels. It contains two fan drivers, both PWM outputs with programmable frequencies. The fan drivers can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct PWM drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors (including support for BJT or transistor model for CPU diodes).

The EMC2104 also includes a hardware programmable temperature limit and dedicated system shutdown output for thermal protection of critical circuitry. Any of the three temperature channels can be configured to measure a thermistor or voltage channel using a precision reference voltage for reduced system complexity.

Figure 5.1 shows a system diagram of the EMC2104.

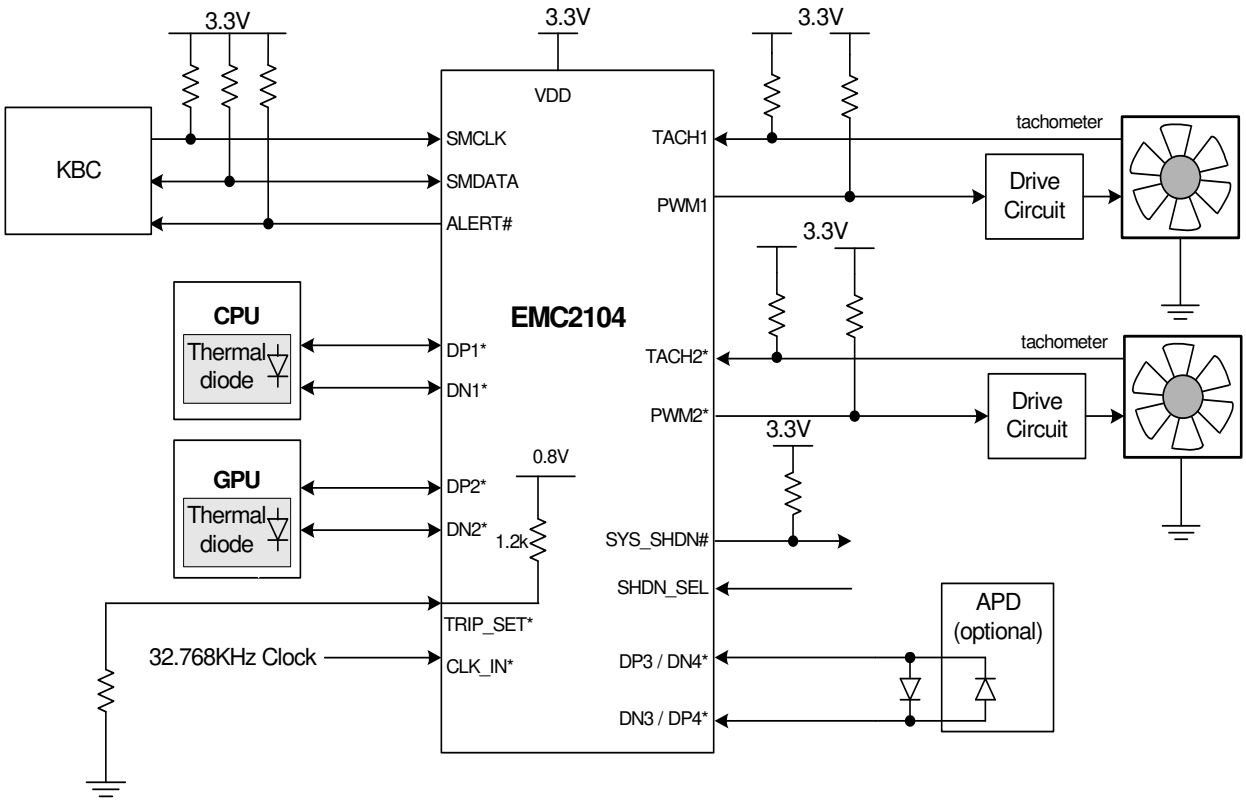

Figure 5.1 System Diagram of EMC2104

5.1 Critical/Thermal Shutdown

The EMC2104 provides a hardware Critical/Thermal Shutdown function for systems. Figure 5.2 is a block diagram of this Critical/Thermal Shutdown function. The Critical/Thermal Shutdown function in the EMC2104 accepts configuration information from the fixed states of the SHDN_SEL pin as described in Section 5.1.1.

Each of the software programmed temperature limits can be optionally configured to act as inputs to the Critical / Thermal Shutdown independent of the hardware shutdown operation. When configured to operate this way, the SYS_SHDN# pin will be asserted when the temperature meets or exceeds the limit. The pin will be released when the temperature drops below the limit however the individual status bits will not be cleared if set (see Section 6.13).

The analog portion of the Critical/Thermal Shutdown function monitors the hardware determined temperature channel (see Section 5.1.1). This measured temperature is then compared with TRIP_SET point. This TRIP_SET point is set by the system designer with a single external resistor divider as described in Section 5.1.2.

The SYS_SHDN# is asserted when the indicated temperature exceeds the temperature threshold established by the TRIP_SET input pin for a number of consecutive measurements defined by the fault queue. If the HW_SHDN output is asserted and the temperature drops below the Thermal / Critical Shutdown threshold then it will be set to a logic ‘0’ state.

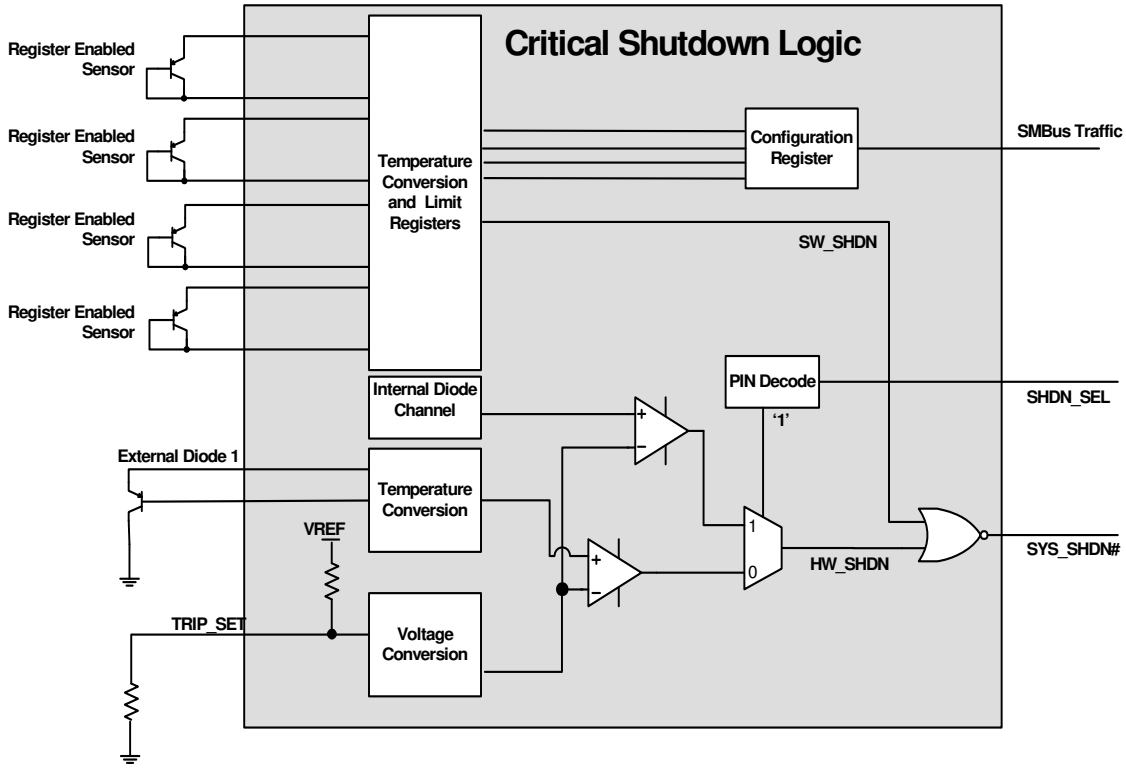

Figure 5.2 EMC2104 Critical/Thermal Shutdown Block Diagram

5.1.1 SHDN_SEL Pin

The EMC2104 has a 'strappable' input (SHDN_SEL) allowing for configuration of the hardware Critical/Thermal Shutdown input channels. This pin has 3 possible states and is monitored and decoded by the EMC2104 at power-up. The three possible states are 0 (tied to GND), 1 (tied to 3.3V) or High-Z (open). The state of this pin determines which external diode configuration is used for the Critical / Thermal shutdown function.

The different configurations of the SHDN_SEL pin are described in Table 5.1. SHDN_SEL applies only to the selected temperature channel.

Table 5.1 SHDN_SEL Pin Configuration

SHDN_SEL	FUNCTION NAME	TEMPERATURE MONITORING FEATURES	CRITICAL / THERMAL SHUTDOWN RANGE
0	Intel Transistor Mode (substrate PNP)	The external diode 1 channel is configured with Beta Compensation enabled and Resistance Error Correction enabled. This mode is ideal for monitoring a substrate transistor such as an Intel CPU thermal diode.	High - 92°C to 154°C
High-Z (open)	AMD CPU / Diode Mode	The external diode 1 channel is configured with Beta Compensation disabled and Resistance Error Correction disabled. This mode is ideal for monitoring an AMD processor diode or a 2N3904 diode.	Low - 60°C to 122°C
1	Internal	The internal diode is linked to the Hardware set Thermal / Critical shutdown circuitry and the SYS_SHDN# pin.	Low - 60°C to 122°C

5.1.2 TRIP_SET / VIN4 Pin

The EMC2104's TRIP_SET / VIN4 pin is an analog input to the Critical/Thermal Shutdown block which sets the Thermal Shutdown temperature. The system designer creates a voltage level at the input through a simple resistor connected to GND as shown in Figure 5.1. The value of this resistor is used to create an input voltage on the TRIP_SET / VIN4 pin which is translated into a temperature ranging from 60°C to 122°C or 90°C to 152°C as enumerated in Table 5.2.

When the SHDN_SEL pin is pulled to '1' at power up, then the TRIP_SET / VIN4 pin is configured to measure VIN4 as its primary function. The circuitry will still calculate the thermal / critical shutdown threshold based on the voltage and compare this temperature against the Internal Diode temperature. This will cause the SYS_SHDN# pin to assert if the measured temperature exceeds this threshold. The device will also compare the measured voltage against the VIN4 High and Low limits. This function is not available if SHDN_SEL is set to '0' or 'High-Z' at power up.

APPLICATION NOTE: If the SHDN_SEL pin is pulled to '1' at power up and the TRIP_SET / VIN4 pin is intended for use as a voltage input then the SYS_SHDN# pin should be ignored.

APPLICATION NOTE: If the SHDN_SEL pin is pulled to '1' at power up and the TRIP_SET / VIN4 pin is intended to be used to set a threshold level then the VIN4 channel should be masked. Furthermore, the voltage on the pin must be externally generated based on Equation [1]. Do not use Table 5.2.

APPLICATION NOTE: When used in its TRIP_SET mode (i.e. the SHDN_SEL pin is not set to a logic '1'), current only flows when the TRIP_SET / VIN4 pin is being monitored. At all other times, the internal reference voltage is removed and the TRIP_SET / VIN4 pin will be pulled down to ground.

APPLICATION NOTE: The TRIP_SET / VIN4 pin circuitry is designed to use a 1% resistor externally. Using a 1% resistor will result in the Thermal / Critical Shutdown temperature being decoded correctly. If a 5% resistor is used, then the Thermal / Critical Shutdown temperature may be decoded with as much as ±1°C error.

$$V_{TRIP} = \frac{T_{TRIP} - T_{MIN}}{80} \quad [1]$$

V_{TRIP} is the TRIP_SET voltage

T_{MIN} is the minimum temperature based on the range

Table 5.2 TRIP_SET Resistor Setting

T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)	T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)
60	92	0.0	92	124	1240
61	93	28.7	93	125	1330
62	94	48.7	94	126	1400
63	95	69.8	95	127	1500
64	96	90.9	96	128	1580
65	97	113	97	129	1690
66	98	137	98	130	1820
67	99	158	99	131	1960
68	100	182	100	132	2050
69	101	210	101	133	2210
70	102	237	102	134	2370
71	103	261	103	135	2550
72	104	294	104	136	2740
73	105	324	105	137	2940
74	106	348	106	138	3160
75	107	383	107	139	3480
76	108	412	108	140	3740
77	109	453	109	141	4120
78	110	487	110	142	4530
79	111	523	111	143	4990
80	112	562	112	144	5490
81	113	604	113	145	6040
82	114	649	114	146	6810

Table 5.2 TRIP_SET Resistor Setting (continued)

T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)	T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)
83	115	698	115	147	7870
84	116	750	116	148	9090
85	117	787	117	149	10700
86	118	845	118	150	12700
87	119	909	119	151	15800
88	120	953	120	152	20500
89	121	1020	121	153	29400
90	122	1100	122	154	49900
91	123	1150	60	92	Open

5.2 Fan Control Modes of Operation

The EMC2104 has four modes of operation for each fan driver. Each mode of operation uses the Ramp Rate control and Spin Up Routine.

1. Direct Setting Mode- in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 6.20) will instantly update the fan drive. Ramp Rate control is optional and enabled via the EN_RRC bits.
   - This is the default mode. The Direct Setting Mode is enabled by clearing the LUT_LOCK bit in the Look Up Table Configuration Register (see Section 6.32) while the TACH / DRIVE bit is set to '0'.
   - Whenever the Direct Setting Mode is enabled the current drive will be changed to what was last written into the Fan Driver Setting Register.
2. Fan Speed Control Mode (FSC) - in this mode of operation, the user determines a target tachometer count and the drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.
   - This mode is enabled by clearing the LUT_LOCK bit in the Look Up Table (LUT) Configuration Register and setting the EN_ALGO bit in the Fan Configuration Register.
3. Using the Look Up Table with Fan Drive Settings (Direct Setting w/ LUT Mode) - In this mode of operation, the user programs the Look Up Table with fan drive settings and corresponding temperature thresholds. The fan drive is set based on the measured temperatures and the corresponding drive settings. Ramp Rate control is optional and enabled via the EN_RRC bits.
   - This mode is enabled by programming the Look Up Table then setting the LUT_LOCK bit while the TACH / DRIVE bit is set to '1'.
   - The TACH / DRIVE bit in the Look Up Table Configuration Register MUST be set to '1' or the fan drive settings will be incorrectly set. Setting this bit to '1' ensures the settings will be PWM settings.
4. Using the Look Up Table with RPM Target Settings (FSC w/ LUT Mode) - In this mode of operation, the user programs the Look Up Table with TACH Target values and corresponding temperature thresholds. The TACH Target will be set based on the measured temperatures and the corresponding target settings. The fan drive settings will be determined automatically based on the RPM based Fan Speed Control Algorithm.
   - This mode is enabled by programming the Look Up Table then setting the LUT_LOCK bit while the TACH / DRIVE bit is set to '0'.