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EMC2106

Dual RPM-Based Linear Fan Controller with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2106 is an SMBus compliant fan controller with up to five (up to 4 external and 1 internal) temperature channels. The fan drivers can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors.

The EMC2106 also includes a hardware programmable temperature limits and dedicated system shutdown output for thermal protection of critical circuitry.

Applications

- Notebook Computers
- Embedded Applications
- Projectors
- Industrial and Networking Equipment

Features

- Two Programmable Fan Control circuits
  - 4-wire fan compatible
  - High speed PWM (26khz)
  - Low speed PWM (9.5Hz - 2240Hz)
  - 600mA, 5V, High Side Fan Driver
  - Optional detection of aging fans
  - 1mA Linear DAC Fan Driver
- RPM based fan control algorithm
  - 2% accuracy from 500RPM to 16k RPM
- Temperature Look-Up Table
  - Allows programmed fan response to temperature
  - 1 to 4 thermal zones to control each fan driver
  - Controls fan speed or drive setting
  - Allows externally generated temperature data to control fan drivers including two DTS channels
- Up to Four External Temperature Channels
  - Designed to support 45nm, 60nm, and 90nm CPUs
  - Automatically detects and supports CPUs requiring the BJT or Transistor models
  - Resistance error correction
  - 1°C accurate (60°C to 100°C)
  - 0.125°C resolution
  - Detects fan aging and variation
- Three dedicated comparator outputs for External Diode 1, External Diode 2, and External Diode 3 (OVERT1#, OVERT2#, OVERT3#)
- Up to three thermistor compatible voltage inputs
- Hardware Programmable Thermal Shutdown Temperature
  - Cannot be altered by software
  - 60°C to 122°C Range or 92°C to 154°C Range
- Programmable High and Low Limits for all channels
- 3.3V Supply Voltage
- SMBus 2.0 Compliant
  - 2 selectable SMBus addresses
  - SMBus Alert compatible
  - Option to load register set from external EEPROM
- Available in 28-pin QFN package - Lead Free RoHS compliant (5mm x 5mm)

ORDER NUMBER:

ORDERING NUMBER	PACKAGE	FEATURES
EMC2106-DZK	28 pin QFN Lead-Free RoHS compliant	Two independent fan drivers (one High Side, one Linear), up to 4 external diode measurement channels, one Critical / Thermal Shutdown input

REEL SIZE IS 4,000 PIECES

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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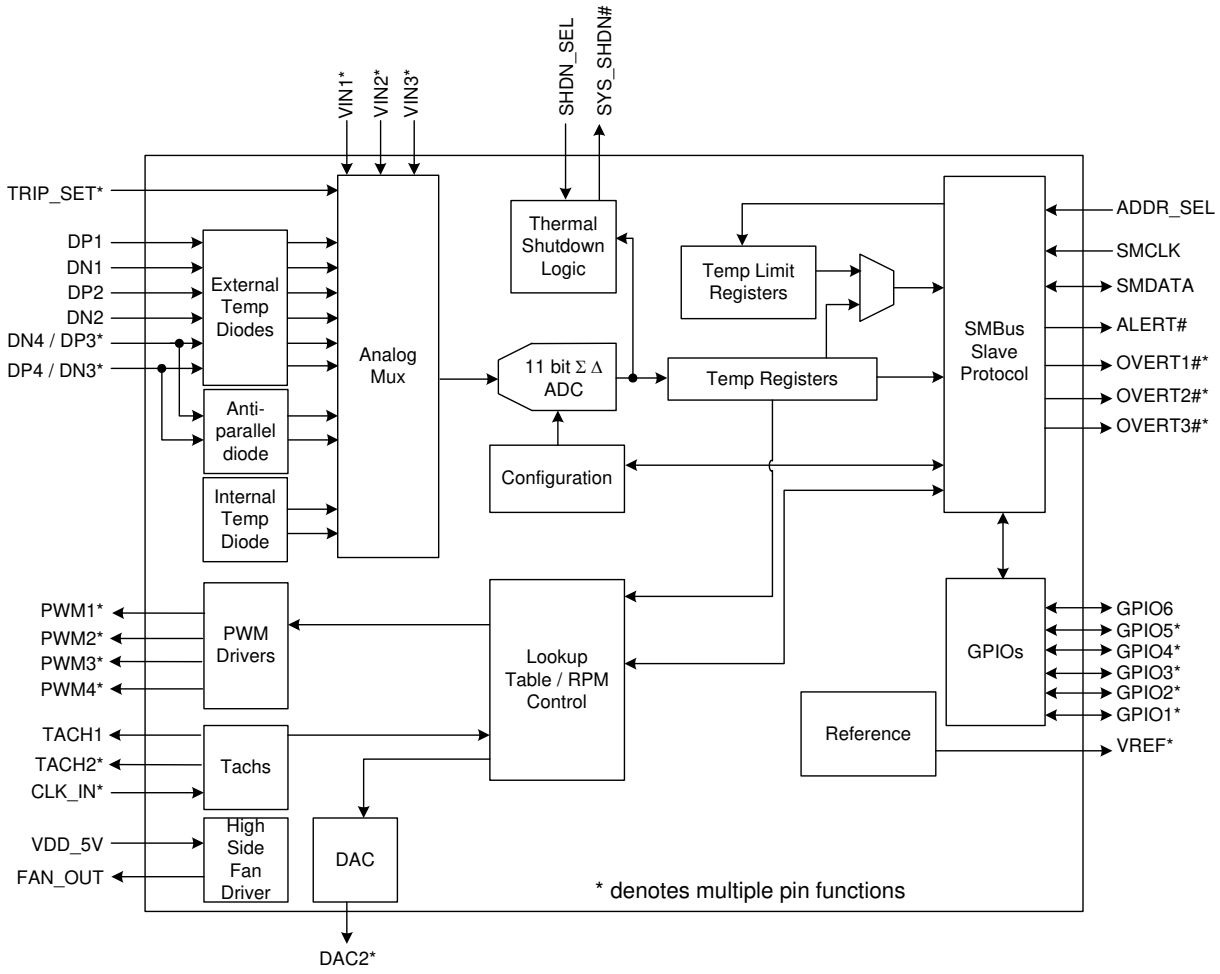

Figure 1.1 EMC2106 Block Diagram

Chapter 2 Pin Description

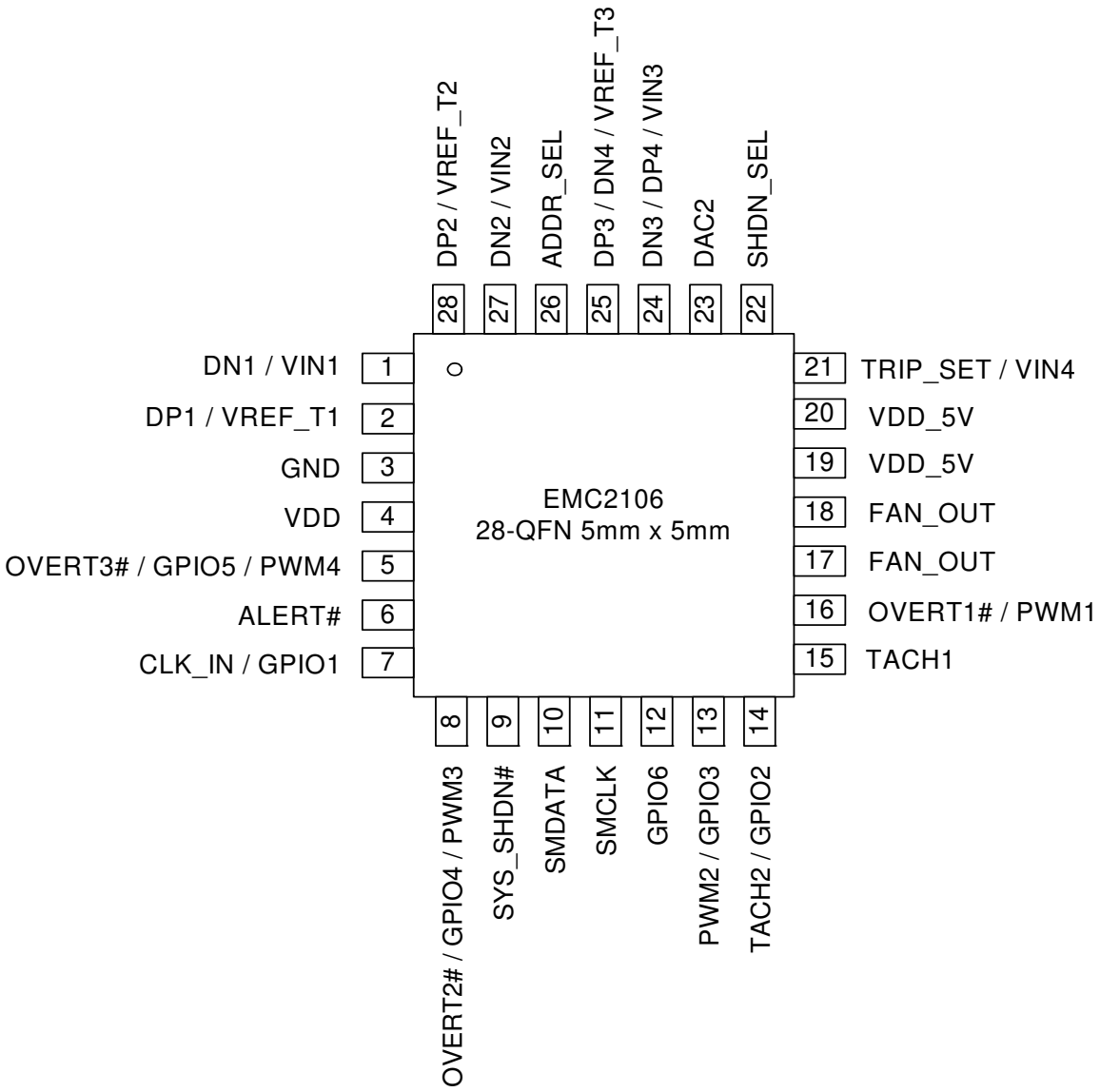

Figure 2.1 EMC2106 Pin Diagram (28 Pin QFN)

Table 2.1 Pin Description for EMC2106

PIN NUMBER EMC2106	PIN NAME	PIN FUNCTION	PIN TYPE
1	DN1 / VIN1	DN1 - Negative (cathode) analog input for External Diode 1 (default)	AIO (2V)
		VIN1 - General Voltage input to be used with a thermistor	AI (2V)
2	DP1 / VREF_T1	DP1 - Positive (anode) analog input for External Diode 1 (default)	AIO (2V)
		VREF_T1 - Reference output for use with a thermistor and to drive VIN1	AO (2V)
3	GND	Ground Connection	Power
4	VDD	Power Supply	Power
5	OVERT3#/ GPIO5/ PWM4	OVERT3# - Active low interrupt for the External Diode 3 channel (default)	OD (5V)
		GPI5 - General Purpose Input	DI (5V)
		GPO5 - General Purpose push/ pull Output	DO
		GPO5 - General Purpose open drain Output.	OD (5V)
		PWM4 - Open Drain PWM driver	OD (5V)
		PWM4 - Push-Pull PWM driver	DO
6	ALERT#	Active low interrupt - requires external pull-up resistor.	OD (5V)
7	CLK_IN / GPIO1	CLK_IN - 32.768KHz clock input.	DI (5V)
		GPI1 - General Purpose Input (default)	DI (5V)
		GPO1 - General Purpose push/ pull Output	DO
		GPO1 - General Purpose open drain Output.	OD (5V)
8	OVERT2# / GPIO4 / PWM3	OVERT2# - Active low Interrupt for the External Diode 2 channel (default)	OD (5V)
		GPI4 - General Purpose Input	DI (5V)
		GPO4 - General Purpose push/ pull Output	DO
		GPO4 - General Purpose open drain Output.	OD (5V)
		PWM3 - Open Drain PWM driver	OD (5V)
		PWM3 - Push-Pull PWM driver	DO

Table 2.1 Pin Description for EMC2106 (continued)

PIN NUMBER EMC2106	PIN NAME	PIN FUNCTION	PIN TYPE
9	SYS_SHDN#	Active low Critical System Shutdown output	OD (5V)
10	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
11	SMCLK	SMBus clock input - requires external pull-up resistor	DIOD (5V)
12	GPIO6	GPI6 - General Purpose Input (default)	DI (5V)
		GPO6 - General Purpose push/ pull Output	OD (5V)
		GPO6 - General Purpose open drain Output.)	DO
13	PWM2 / GPIO3	PWM2 - Open Drain PWM drive output for Fan 2 (default)	OD (5V)
		PWM2 - Push-Pull PWM drive output for Fan 2	DO
		GPI3 - General Purpose Input	DI (5V)
		GPO3 - General Purpose push-pull Output	DO
		GPO3 - General Purpose open drain Output	OD (5V)
14	TACH2 / GPIO2	TACH2 - Tachometer input for Fan 2 (default)	DI (5V)
		GPI2 - General Purpose Input	DI (5V)
		GPO2 - General Purpose push-pull Output	DO
		GPO2 - General Purpose open drain Output	OD (5V)
15	TACH1	Tachometer input for Fan 1	DI (5V)
16	OVERT1# / PWM1	OVERT1# - Active low interrupt for the External Diode 1 channel (default)	OD (5V)
		PWM1 - Open Drain PWM drive output for Fan 1	OD (5V)
		PWM1 - Push-Pull PWM drive output for Fan 1	DO
17	FAN_OUT	High Side Fan Driver Output	Power
18	FAN_OUT	High Side Fan Driver Output	Power
19	VDD_5V	Supply for High Side Fan Driver	Power
20	VDD_5V	Supply for High Side Fan Driver	Power

Table 2.1 Pin Description for EMC2106 (continued)

PIN NUMBER EMC2106	PIN NAME	PIN FUNCTION	PIN TYPE
21	TRIP_SET / VIN4	TRIP_SET - Determines HW Shutdown temperature features for the hardware shutdown channel	AI (2V)
		VIN4 - General voltage input when Thermal / Critical shutdown disabled	AI (2V)
22	SHDN_SEL	Determines HW Shutdown temperature features and measurement channel	AIO
23	DAC2	Linear Fan Driver Output	AO (2V)
24	DN3 / DP4 / VIN3	DN3 / DP4 - Negative (cathode) analog input for External Diode 3 and positive (anode) Analog Input for External Diode 4 (default)	AIO (2V)
		VIN3 - General voltage input for use with a thermistor	AI (2V)
25	DP3 / DN4 / VREF	DP3 / DN4 - Positive (anode) analog input for External Diode 3 and negative (cathode) analog input for External Diode 4 (default)	AIO (2V)
		VREF_T3 - Reference output for use with a thermistor and to drive VIN3	AO (2V)
26	ADDR_SEL	Selects SMBus slave address	DIT
27	DN2 / VIN2	DN2 - Negative (cathode) analog input for External Diode 2 (default)	AIO (2V)
		VIN2 - General voltage input for use with a thermistor	AI (2V)
28	DP2 / VREF_T2	DP2 - Positive (anode) analog input for External Diode 2 (default)	AIO (2V)
		VREF_T2 - Reference output for use with a thermistor and to drive VIN2	AO (2V)
Thermal Slug	GND	Ground	Power

The pin type are described in detail below. All pins labelled with (5V) are 5V tolerant.

All pin labelled with (2V) should not be exposed to any voltage level greater than 2V.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AI	Analog Input - this pin is used as an input for analog signals.

Table 2.2 Pin Types (continued)

PIN TYPE	DESCRIPTION
AO	Analog Output - this pin is used as an output for analog signals.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output this pin is used as an digital I/O. When it is used as an output, It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

Table 3.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins including VDD_5V	-0.3 to 6.5	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on 2V tolerant pins	-0.3 to 2.5	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation See Note 3.1	1 up to T_A = 85°C	W
Junction to Ambient (θ_{JA}) See Note 3.2	40	°C/W
Operating Ambient Temperature Range	-40 to 85°C	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a recommended thermal via design consisting of four 12mil vias connected to the ground plane with a 2x2mm thermal landing.

Note 3.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 52°C/W including localized PCB temperature increase.

3.1 Electrical Specifications

Table 3.2 Electrical Specifications

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current (active)	I_{DD}		2	3	mA	4 Conversions / second - Dynamic Averaging Enabled Fan Drivers enabled at max PWM frequency

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current	I_{DD}		500	750	uA	1 Conversions / second- Dynamic Averaging disabled, Fan Drivers disabled.
Supply Current from VDD_5V	I_{DD_5}		100		uA	Fan Driver enabled, No load current
SMBus Delay	t_{SMB}			15	ms	Delay from power to first SMBus communication
Time to First Round Robin				300	ms	
External Temperature Monitors						
Temperature Accuracy			±0.25	±1	°C	60°C < T_{DIODE} < 110°C 30°C < T_{DIE} < 85°C
			±0.5	±2	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{DIE} < 115°C
Temperature Resolution			0.125		°C	
Diode decoupling capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Resistance Error Corrected	R_{SERIES}			100	Ohm	Sum of series resistance in both DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy	T_{DIE}		±1	±2	°C	Note 3.4
Temperature Resolution			0.125		°C	
Voltage Measurement						
Total Unadjusted Error	TUE			1	%	Measured at 3/4 full scale
Reference Voltage	V_{REF}		800		mV	
Reference Accuracy	ΔV_{REF}		1		%	
PWM Fan Driver						
PWM Resolution	PWM		256		Steps	
PWM Duty Cycle	DUTY	0		100	%	
High Side Fan Driver						
Output High Voltage from 5V supply	V_{OH_5V}	VDD_5V - 0.35	VDD_5 V - 0.3		V	I_{SOURCE} = 600mA, VDD_5V = 5V
Voltage Accuracy	ΔV_{FAN_OUT}		1	2	%	Measured at 3/4 full scale - Direct Setting Mode

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Fan Drive Current	I_{SOURCE}			600	mA	
Overcurrent Limit	I_{OVER}			2800	mA	Momentary Current drive at startup for < 2 seconds 1.5V < FAN_OUT < 3.5V
DC Short Circuit Current Limit	I_{SHORT}		700		mA	Sourcing current, Thermal shutdown not triggered, FAN_OUT = 0V
Short circuit delay	t_{DFS}		2		s	
Output Capacitive Load	C_{LOAD}			100	uF	Z_{ESR} < 100mΩ at 10kHz
Linear DAC Fan Driver						
DAC Output High Voltage	V_{DAC2_OH}	V_{DD} - 0.2			V	I_{DAC2} = 1mA current source
DAC Output Low Voltage	V_{DAC2_OL}			0.3	V	I_{DAC2} = -1mA current sink
Output Voltage Accuracy	ΔV_{DAC2}			2	%	Measured at 3/4 full scale - Direct Setting Mode
Fan Drive Current	I_{DAC2}	-1		1	mA	
RPM Based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}		±1	±2	%	External oscillator 32.768kHz
	Δ_{TACH}		±2.5	±5	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Thermal Shutdown						
Thermal Shutdown Threshold	TSD_{TH}		150		°C	
Thermal Shutdown Hysteresis	TSD_{HYST}		50		°C	
Digital I/O pins						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	4 mA current drive
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Leakage current	I_{LEAK}			±5	uA	$\overline{ALERT}$ and $\overline{SYS\_SHDN}$ pins Powered and unpowered

Note 3.4 T_{DIE} refers to the internal die temperature and may not match T_A due to self heating of the device. The internal temperature sensor will return T_{DIE}.

3.2 SMBus Electrical Specifications (client mode)

Table 3.3 SMBus Electrical Specifications

VDD= 3V to 3.6V, T_A = -40°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered and unpowered
Input Capacitance	C_{IN}		5		pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

3.3 EEPROM Loader Electrical Specifications

Table 3.4 EEPROM Loader Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Interface						
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current		4			mA	V_{OL} = 0.4V
Timing						
Loading Delay	t_{DLY}		10		ms	Delay after power-up until EEPROM loading begins. (See Section 4.9.)
Loading Time	t_{LOAD}		50		ms	
Clock Frequency	f_{SMB}		50		kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 Communications

4.1 System Management Bus Interface Protocol

The EMC2106 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2106 will not stretch the clock signal.

The EMC2106 powers up as an SMBus client (after loading from EEPROM as applicable).

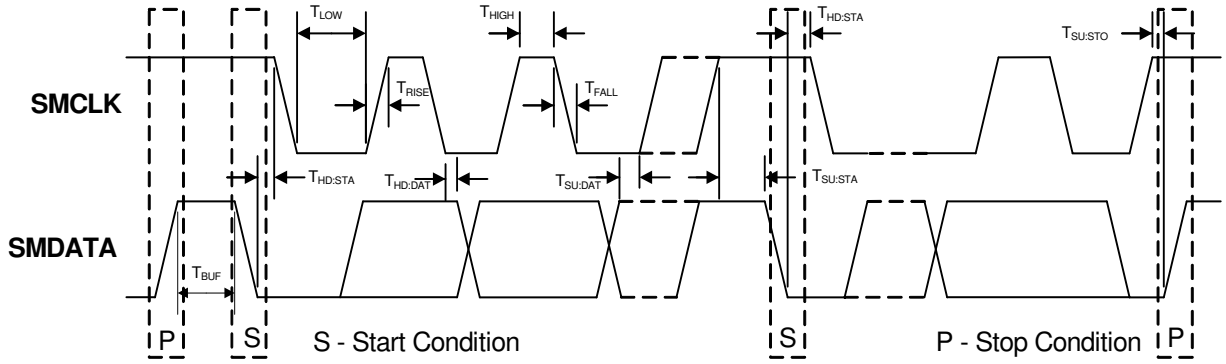

Figure 4.1 SMBus Timing Diagram

The EMC2106 contains a single SMBus interface. The SMBus address is determined by the ADDR_SEL pin (see Section 4.7)The EMC2106 client interfaces are SMBus 2.0 compatible and support Send Byte, Read Byte, Receive Byte and the Alert Response Address as valid protocols. These protocols are used as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
0 -> 1	0101_111	0	0	XXh	0	XXh	0	1 -> 0

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
0 -> 1	0101_111	0	0	XXh	0	0 -> 1	0101_111	1	0	XXh	1	1 -> 0

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
0 -> 1	0101_111	0	0	XXh	0	1 -> 0

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	0101_111	1	0	XXh	1	1 -> 0

4.6 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the ALERT# pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	0001_100	1	0	0101_111	1	1 -> 0

The EMC2106 will respond to the ARA in the following way if the ALERT# pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the ALERT# pin.
3. The ARA will NOT affect the OVERT1#, OVERT2#, and OVERT3# pins. These pins will be asserted as long as the error condition is present. When the error condition is removed, the pins will be cleared.

4.7 SMBus Address

The EMC2106 SMBus Address is determined by the status of the ADDR_SEL pin as shown in Table 4.7.

Table 4.7 ADDR_SEL Pin Decode

ADDR_SEL	SMBUS ADDRESS	FUNCTION
'0' (GND)	0101_111xb	SMBus Client
'Z' (open)	0101_111xb	EEPROM Programming
'1' (VDD)	0101_110xb	SMBus Client

Attempting to communicate with the EMC2106 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.8 SMBus Time-out

The EMC2106 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface. The SMBus Timeout defaults to enabled and can be disabled by setting the DIS_TO bit in the Configuration 2 register.

4.9 Programming from EEPROM

When configured to load from EEPROM (see Section 4.7), the EMC2106 acts as a simple SMBus Master to read data from a connected EEPROM using the following procedure.

1. After power-up the EMC2106 waits for 10ms with the SMDATA and SMCLK pins tri-stated.
2. Once the wait period has elapsed, the EMC2106 sends a START signal followed by the 7 bit client address 1010 _000xb followed by a '0b' and waits for an ACK signal from the EEPROM.
3. When the EEPROM sends the ACK signal, the EMC2106 will send a second start signal and continue sending the Block Read Command (see Table 4.8) to the same slave address. It reads 256 data bytes from the EEPROM sending an ACK between each data byte. When 256 data bytes have been received, it sends a NACK signal followed by a STOP bit.
4. Resets the device as an SMBus Client with slave address 0101_111xb.

If the EMC2106 does not receive an acknowledge bit from the EEPROM then the following will occur:

1. The ALERT# pin will be asserted and will remain asserted until a Host device initiates communication with the EMC2106 and reads the Status Register. The ALERT# pin will be de-asserted after a single Status Register read.
2. The EMC2106 will reset its SMBus protocol as a slave interface and start operating from the default conditions with slave address 0101_111xb.

Table 4.8 Block Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	SLAVE ADDRESS	RD	ACK	Register Data (00h)	. . .
0-> 1	0101_111	0	0	00h	0	0 -> 1	0101_111	1	0	XXh	
ACK	**Register Data (01h)**	**ACK**	**Register Data (02h)**	**ACK**	**Register Data (03h)**	**. . .**	**ACK**	**Register Data (FFh)**		**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	. . .	0	XXh		1	1 -> 0

Note: The shaded columns represent data sent from the EMC2106 to the EEPROM device.

APPLICATION NOTE: It is recommended that the EEPROM that is used be an AT24C02B or equivalent device. The EEPROM slave address must be 1010_000xb. The device must support a block-read command, 8-bit addressing, and 8-bit data formatting using a 2-wire bus. The device must support 3.3V digital switching logic and may not pull the SMCLK and SMDATA pins above 5V. Data must be transmitted MSB first.

APPLICATION NOTE: No other SMBus Master should exist on the SMDATA and SMCLK lines. The presence of another SMBus Master will cause errors in reading from the EEPROM.

The EEPROM should be loaded to mirror the register set of the EMC2106 with the desired configuration set. All undefined registers in the EMC2106 register set should be loaded with 00h in the EEPROM. Likewise, all registers that are read-only in the EMC2106 register set should be loaded with 00h in the EEPROM.

Because of the interaction between the Fan Control Look-up Tables and the Fan Configuration Register, the EEPROM Loader stores the contents of the Fan Configuration Registers and updates these registers at the end of the EEPROM loading cycle.

Chapter 5 Product Description

The EMC2106 is an SMBus compliant fan controller with up to four (up to 4 external) temperature channels. It contains two fan drivers, a High Side fan driver capable of sourcing 600mA from a 5V supply and a linear DAC fan driver. In addition, the EMC2106 contains up to four (4) PWM outputs (two of which can be used with the RPM based Fan Speed Control Algorithm). The fan drivers can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct fan drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors (including support for BJT or transistor model for CPU diodes).

The EMC2106 also includes a hardware programmable temperature limit and dedicated system shutdown output for thermal protection of critical circuitry. Any of the three temperature channels can be configured to measure a thermistor or voltage channel using a precision reference voltage for reduced system complexity.

Figure 5.1 shows a system diagram of the EMC2106.

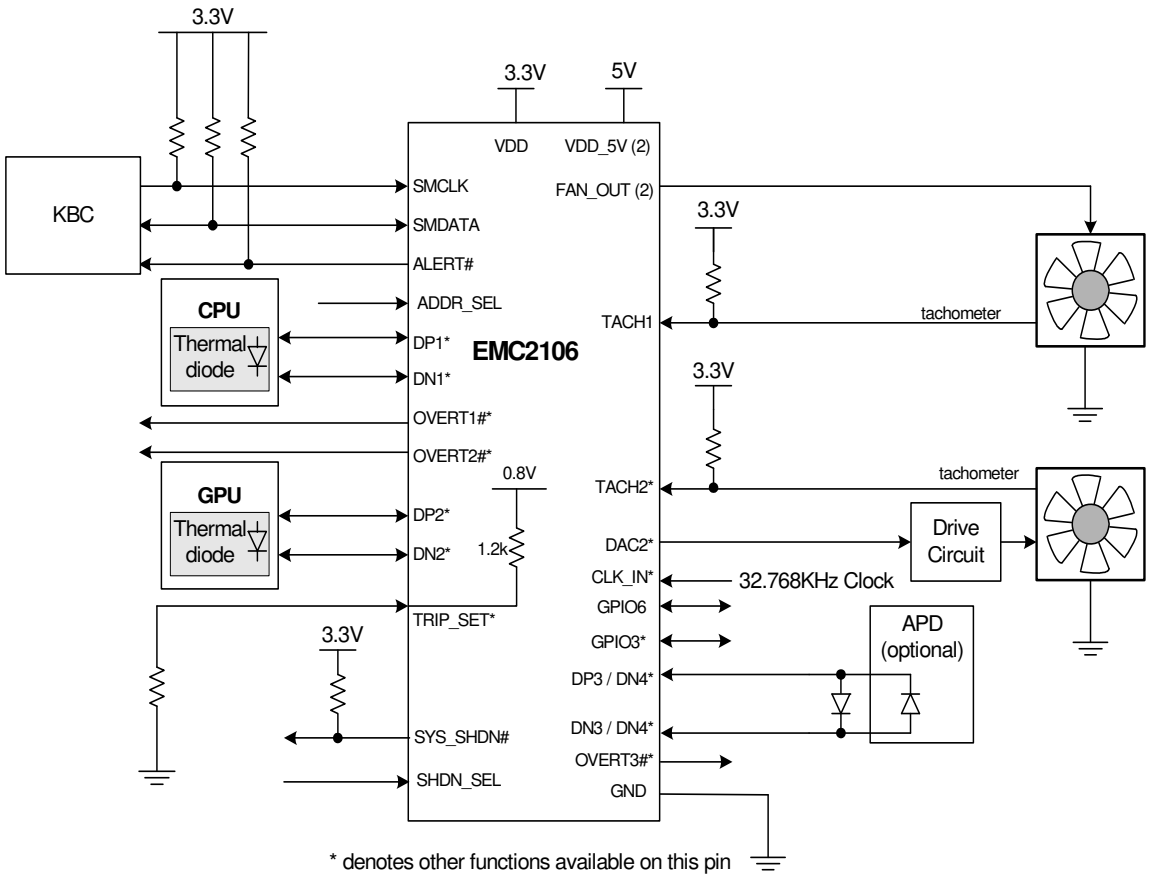

Figure 5.1 System Diagram of EMC2106

5.1 Critical/Thermal Shutdown

The EMC2106 provides a hardware Critical/Thermal Shutdown function for systems. Figure 5.2 is a block diagram of this Critical/Thermal Shutdown function. The Critical/Thermal Shutdown function in the EMC2106 accepts configuration information from the fixed states of the SHDN_SEL pin as described in Section 5.1.1.

Each of the software programmed temperature limits can be optionally configured to act as inputs to the Critical / Thermal Shutdown independent of the hardware shutdown operation. When configured to operate this way, the SYS_SHDN# pin will be asserted when the temperature meets or exceeds the limit. The pin will be released when the temperature drops below the limit however the individual status bits will not be cleared if set (see Section 6.13).

The analog portion of the Critical/Thermal Shutdown function monitors the hardware determined temperature channel (see Section 5.1.1). This measured temperature is then compared with TRIP_SET point. This TRIP_SET point is set by the system designer with a single external resistor divider as described in Section 5.1.2.

The SYS_SHDN# is asserted when the indicated temperature exceeds the temperature threshold established by the TRIP_SET input pin for a number of consecutive measurements defined by the fault queue. If the HW_SHDN output is asserted and the temperature drops below the Thermal / Critical Shutdown threshold then it will be set to a logic ‘0’ state.

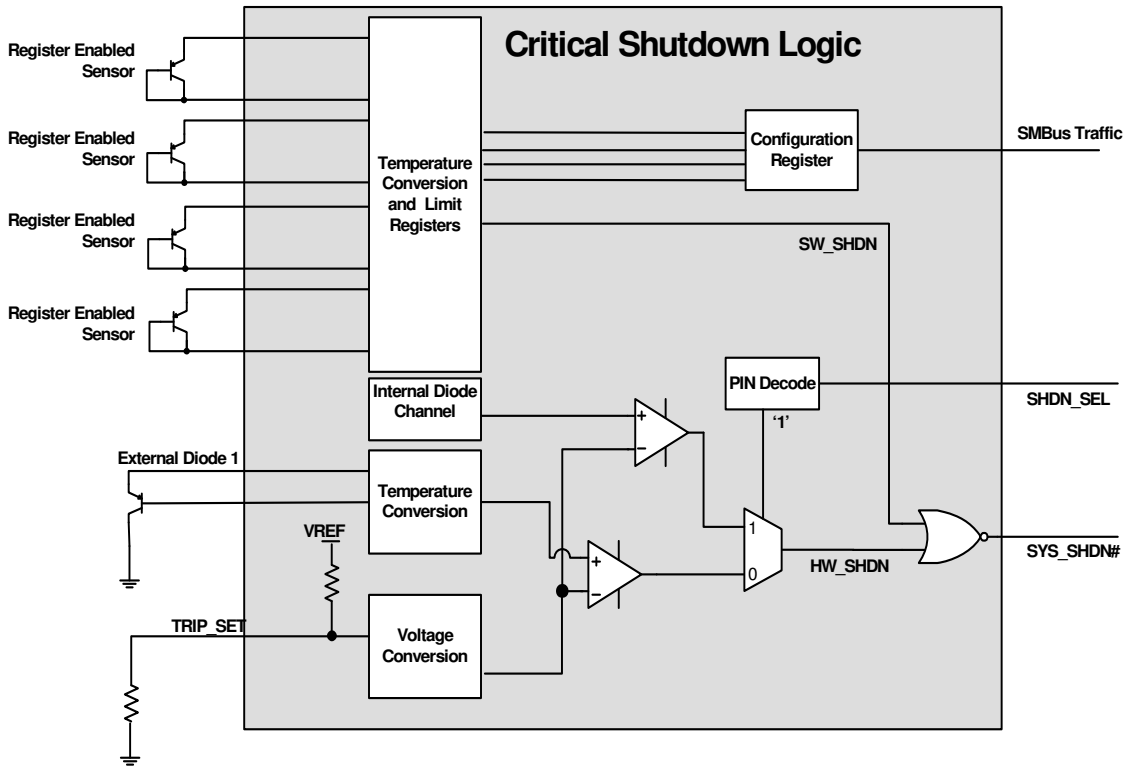

Figure 5.2 EMC2106 Critical/Thermal Shutdown Block Diagram