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EMC2112

RPM-Based Linear Fan Controller with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2112 is an SMBus, closed-loop, RPM-based fan driver with hardware (HW) thermal shutdown and reset controller. The EMC2112 offers a single High Side fan driver capable of sourcing up to 600mA from a 5V supply.

The EMC2112 utilizes Beta Compensation (an implementation of the BJT or transistor model for thermal diodes) and Resistance Error Correction (REC) to accurately monitor up to three (3) external temperature zones. These features allow great accuracy for CPU substrate thermal diodes on multiple process geometries as well as with discrete diode-connected transistors. Both Beta Compensation and REC can be disabled on the EMC2112 to maintain accuracy when monitoring AMD thermal diodes.

The EMC2112 provides a stand-alone HW thermal shutdown block. The HW thermal shutdown logic can be configured for a few common configurations based on the strapping level of the SHDN_SEL pin on the PCB. The HW thermal shutdown point can be set in 1°C increments by using a discrete resistor connected to the TRIP_SET pin.

The EMC2112 also provides 5V supply 'power good' function with a threshold of 4.5V. This function is provided on the $\overline{\text{RESET}}$ pin.

Applications

- Notebook Computers
- Desktop Computers
- Embedded Applications

Features

- Closed-Loop RPM-Based Fan Controller
  - 1% accuracy with external clock input
  - 3% accuracy with internal clock
  - Internal clock can be used as a source
  - Aging fan detection
- Integrated Linear Fan Driver
  - 600mA drive capability
- HW Thermal Shutdown ($\overline{\text{SYS\_SHDN}}$)
  - 1°C incremental set points for thermal shutdown
  - Cannot be disabled by software
- Provides Reset Function ($\overline{\text{RESET}}$) On 5V Supply
- Up to Three (3) Remote Thermal Zones
  - ±1°C accuracy (60°C to 100°C)
  - 0.125°C resolution
  - Designed to support 45nm, 65nm, and 90nm CPU Diodes using BJT and transistor model
  - Eliminates temperature offset due to series resistance from PCB traces and thermal 'Diode'
- Operates From Single 3.0 - 3.6V Supply
  - 5V supply for linear fan driver and reset generator
- SMBus 2.0 and I^2C compatible
  - User selectable SMBus address using pull-up resistor on ADDR_SEL pin
  - Supports Block Read and Write functionality
- Available in 20-pin, 4x4 QFN Lead-free RoHS Compliant package

ORDERING INFORMATION:

ORDERING NUMBER	PACKAGE	FEATURES
EMC2112-BP-TR	20-pin QFN 4mm x 4mm (Lead-Free RoHS compliant)	Three External Diodes. High Side Fan driver w/ RPM based Fan Speed Control algorithm. Reset generator. Hardware set critical temperature limit

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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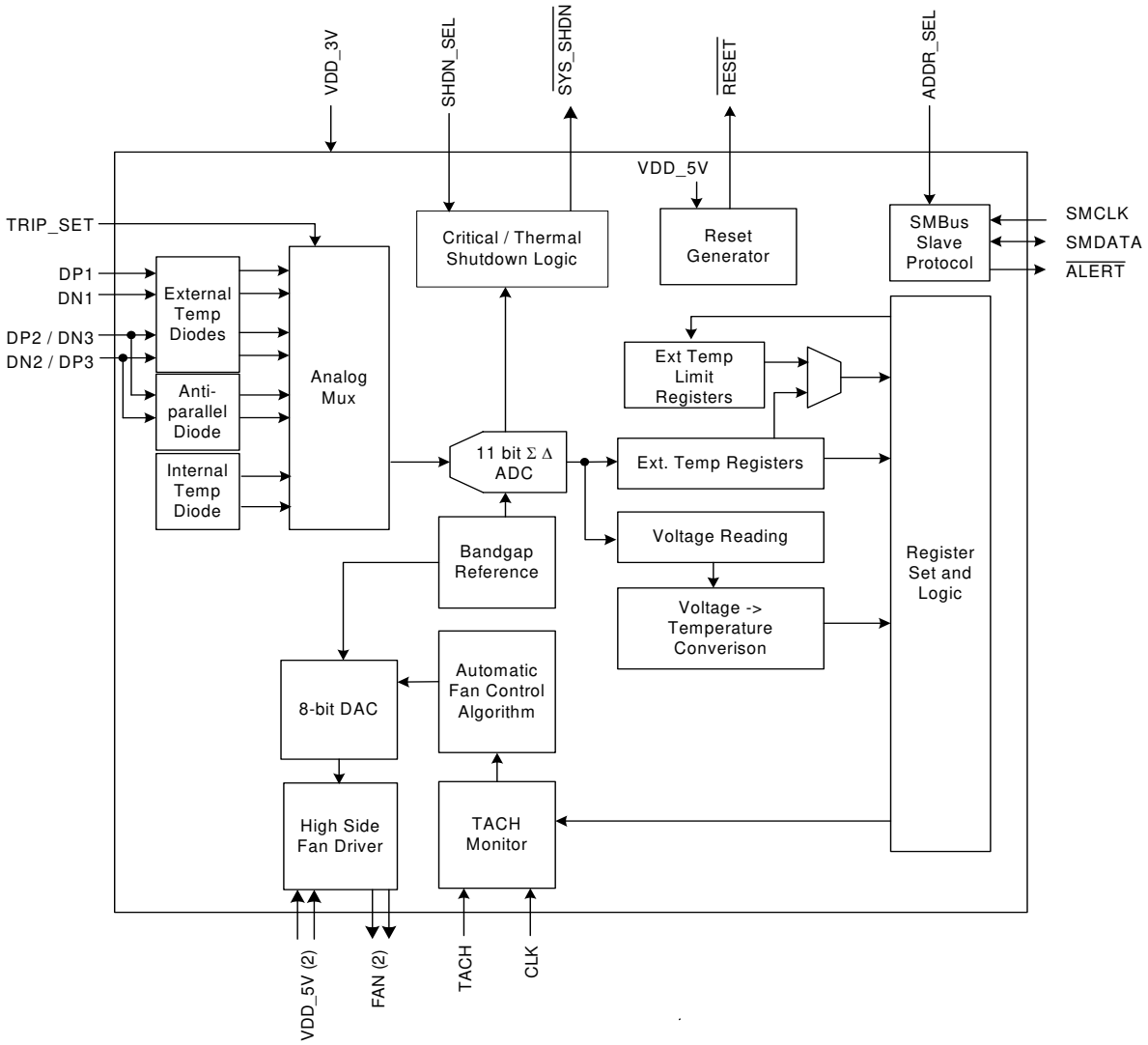

Figure 1.1 EMC2112 Block Diagram

Chapter 2 Pin Layout

2.1 Pin Layout for EMC2112

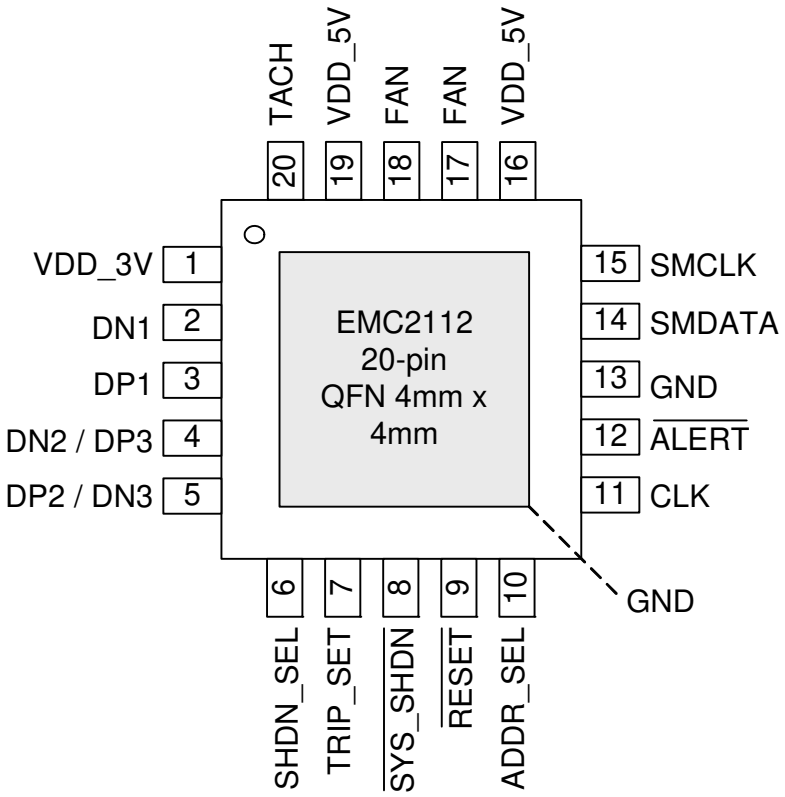

Figure 2.1 EMC2112 Pin Diagram

2.2 Pin Description for EMC2112

Table 2.1 Pin Description

PIN	NAME	FUNCTION	TYPE
1	VDD_3V	3.3V Supply Voltage	Power
2	DN1	Negative (cathode) Analog Input for External Diode 1	AIO
3	DP1	Positive (anode) Analog Input for External Diode 1	AIO
4	DN2 / DP3	Negative (cathode) Analog Input for External Diode 2 and Positive (anode) Analog Input for External Diode 3	AIO

Table 2.1 Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
5	DP2 / DN3	Positive (anode) Analog Input for External Diode 2 and Negative (cathode) Analog Input for External Diode 3	AIO
6	SHDN_SEL	Determines HW Shutdown temperature channel	DIT
7	TRIP_SET	Voltage input to determine HW Shutdown threshold temperature	AIO
8	$\overline{\text{SYS\_SHDN}}$	Active low Critical System Shutdown output	OD (5V)
9	$\overline{\text{RESET}}$	Push-Pull, active low reset output	DO
10	ADDR_SEL	Selects SMBus Address	DIT
11	CLK	Tachometer clock input	DI (5V)
		Tachometer clock output	DO
12	$\overline{\text{ALERT}}$	Open drain, active low interrupt. Requires external pull-up resistor	OD (5V)
13	GND	Ground Connection	Power
14	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
15	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
16	VDD_5V	5V supply input for the linear fan driver. Both VDD_5V pins should be connected to same 5V supply.	Power
17	FAN	Linear fan drive signal. Both FAN pins should be connected together.	AO
18	FAN	Linear fan drive signal. Both FAN pins should be connected together.	AO
19	VDD_5V	5V supply input for the linear fan driver. Both VDD_5V pins should be connected to same 5V supply.	Power
20	TACH	Tachometer input from Fan	DI (5V)

The pin type are described in Table 2.2. All pins labeled with (5V) are 5V tolerant.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AO	Analog Output - this pin is used as an output for analog signals.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.

Table 2.2 Pin Types (continued)

PIN TYPE	DESCRIPTION
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output - this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DIO	Digital Input / Output - this pin is used as a digital I/O. It is push-pull and can sink or source up to 8mA.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DIT	Tri-stated Digital Input - this pin is a digital input that supports 3 logic levels at the input: logic high, logic low, or high impedance (open).

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Voltage on VDD_5V Pins and 5V tolerant pins (see Table 2.1)	-0.3 to 6.5	V
Voltage on VDD_3V pin	-0.3 to 4	V
Voltage on FAN pins	-0.3 to VDD_5V + 0.3	V
Voltage on any other pin to GND	-0.3 to VDD_3V + 0.3	V
Package Power Dissipation	0.9 up to T_A = 85°C Note 3.2	W
Junction to Ambient - 20 pin QFN (θ_{JA}) Note 3.3	40	°C/W
Operating Ambient Temperature Range	0 to 85	°C
Operating Die Temperature Range	0 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

These ratings are absolute maximum values. Exceeding these values or operating at these values for an extended period of time may cause permanent damage to the device.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a thermal via design consisting of four 20mil vias connected to the ground plane with a 2.6mm x 2.6mm thermal landing.

Note 3.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
3.3V Supply Voltage	V_{DD_3V}	3	3.3	3.6	V	
5V Supply Voltage	V_{DD_5V}	4.6	5	5.5	V	
Supply Current from VDD_3V pin	I_{DD3}		0.750	1.6	mA	Fan Driver enabled 4 conversions / sec
Supply Current from VDD_5V pin	I_{DD5}		50		uA	Fan Driver enabled

Table 3.2 Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
External Temperature Monitors						
Temperature Accuracy			±0.25	±1	°C	60°C < T_{DIODE} < 100°C 30°C < T_{DIE} < 85°C (Note 3.4)
			±0.5	±2	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{DIE} < 115°C (Note 3.4)
Temperature Resolution			0.125		°C	
Diode Decoupling Capacitor	C_{FILTER}			2700	pF	Connected across external 2N3904 diode or AMD diode (Note 3.5)
Resistance Error Corrected	R_{SERIES}			100	Ohm	Series resistance in DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy			±1	±2	°C	(Note 3.4)
Temperature Resolution			0.125		°C	
Reset Generator						
Reset Voltage	V_{RESET}	4.3	4.4	4.5	V	V_{DD_5V} rising edge 3V < V_{DD_3V} < 3.6V
Hysteresis	ΔV_{RESET}		100		mV	
Time Delay	t_{RESET}		220		ms	
High Side Fan Driver						
Output High Voltage from 5V Supply	V_{OH_5V}			VDD_5 V - 0.4	V	I_{SOURCE} = 600mA, VDD_5V = 5V
Fan Drive Current	I_{SOURCE}			600	mA	
Overcurrent Limit	I_{OVER}		1500		mA	Momentary Current drive at startup for < 2 seconds
DC Short Circuit Current Limit	I_{SHORT}		800		mA	Sourcing current, Thermal shutdown not triggered, FAN_OUT = 0V
Short Circuit Delay	t_{DFS}		2		s	
Output Capacitive Load	C_{LOAD}			100	uF	
ESR on C_{LOAD}	R_{ESR}	0		2	Ohm	
RPM-Based Fan Controller						
TACH Range	TACH	480		16000	RPM	

Table 3.2 Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
RPM Control Accuracy	Δ_{TACH}		±0.25	±0.5	%	External oscillator 32.768kHz
	Δ_{TACH}		±0.5	±1	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Thermal Shutdown						
Thermal Shutdown Threshold	TSD_{TH}		150		°C	
Thermal Shutdown Hysteresis	TSD_{HYST}		50		°C	
SMBus and Digital I/O pins						
Output High Voltage	V_{OH}	VDD _3V-0.4			V	4 mA current drive
Output Low Voltage	V_{OL}			0.5	V	4 mA current sink

Note 3.4 T_{DIE} refers to the internal die temperature and may not match T_A due to self heating of the device. The internal temperature sensor will return T_{DIE}.

Note 3.5 Contact SMSC for Application Notes and guidelines when measuring GPU processor diodes and CPU processor diodes.

Note 3.6 The $\overline{\text{ALERT}}$, $\overline{\text{SYS\_SHDN}}$, SMDATA, and SMCLK pins will not glitch low upon power up when pulled to VDD or another voltage.

3.3 SMBus Electrical Specifications

Table 3.3 SMBus Electrical Specifications

VDD_3V = 3V to 3.6V, VDD_5V = 4.6 to 5.5V, T_A = 0°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			4		mA	SMDATA = 0.5V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	

Table 3.3 SMBus Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6 to 5.5V, T_A = 0°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Bus Free Time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC2112 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2112 will not stretch the clock signal.

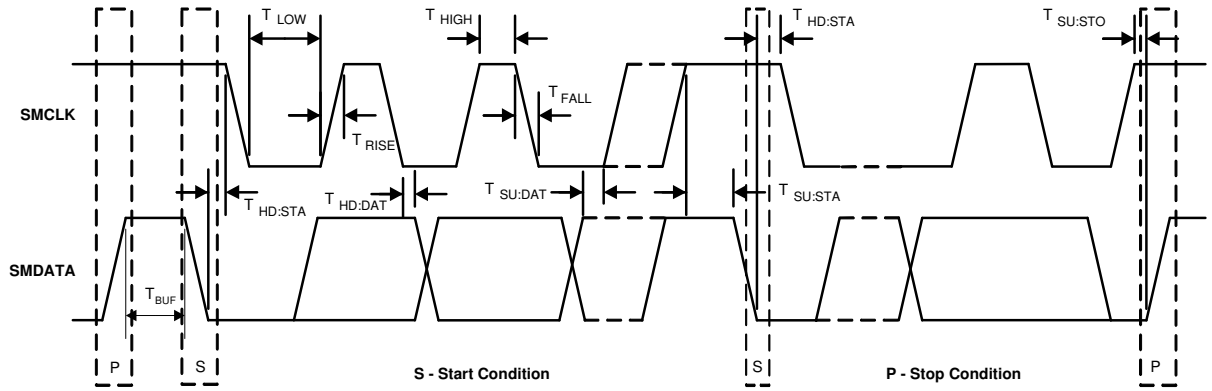

Figure 4.1 SMBus Timing Diagram

4.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state. When the EMC2112 detects an SMBus Start bit, it will disable the BC-Link protocol circuitry and communicate using the SMBus Protocol

4.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a -bit RD / $\overline{WR}$ indicator. If this RD / WR bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The slave address is determined at power up by the pin-state of the ADDR_SEL pin as shown in Table 4.1.

Table 4.1 ADDR_SEL Pin Configuration

ADDR_SEL PIN STATE	SMBUS SLAVE ADDRESS
‘0’	0101_111xb
‘High Z’	0111_101xb
‘1’	0101_110xb

4.1.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

4.1.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the ATF_INT# pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The Host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

4.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC2112 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

4.1.6 SMBus Time-out

The EMC2112 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface. The timeout can be disabled by setting the DIS_TO bit in the Configuration 2 register.

4.1.7 SMBus and I^2C Compliance

The major difference between SMBus and I2C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held for longer than 30ms.
3. The slave protocol will reset if both the clock and data lines are held high for longer than 150us.
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).
5. The Block Read and Block Write protocols are only compliant with I^2C data formatting. They do not support SMBus formatting for Block Read and Block Write protocols.

4.2 SMBus Protocols

The EMC2112 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and Write Byte as valid protocols as shown below. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 4.2.

Table 4.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.3:

Table 4.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	0111_101	0	0	XXh	0	XXh	0	0 -> 1

4.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.4.

Table 4.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 -> 0	0111_101	0	0	XXh	0	0 -> 1	0111_101	1	0	XXh	1	0 -> 1

4.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.5.

Table 4.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	0111_101	0	0	XXh	0	0 -> 1

4.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.6.

Table 4.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	0111_101	1	0	XXh	1	0 -> 1

4.2.5 Block Write Protocol

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 4.7. It is an extension of the Write Byte Protocol.

Table 4.7 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	0111_101	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

4.2.6 Block Read Protocol

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 4.8. It is an extension of the Read Byte Protocol.

Table 4.8 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	0111_101	0	0	XXh	0	1 ->0	0111_101	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

4.2.7 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4.9.

Table 4.9 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	0001_100	1	0	0111_1010b	1	1 -> 0

The EMC2112 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

Chapter 5 General Description

The EMC2112 monitors up to three (3) external temperature channels. Each of the external temperature channels can employ both Beta Compensation (an implementation of the BJT or transistor model for thermal diodes) and Resistance Error Correction for use with thermal diodes while the third channel is hardwired to measure a discrete diode connected NPN or PNP transistor. The temperature data is available over a standard 2-wire serial interface using SMBus read commands. The temperature monitoring is described in more detail in Section 5.11, "Temperature Monitoring".

The EMC2112 includes a closed-loop RPM-based Fan Control Algorithm for each fan driver. The host writes the desired fan speed into a register of the EMC2112 via the SMBus and the integrated fan controller will maintain the fan at the desired speed using fan speed feedback from the TACH output from a 3-wire fan. The fan control algorithm controls an integrated 5V, 600mA, linear fan driver.

The EMC2112 provides the system with a hardware based critical/thermal shutdown function. This critical/thermal shutdown function integrates critical signals from both the CPU and power supply and the analog circuitry to monitor a specific temperature channel based on the system configuration. The critical/thermal shutdown temperature threshold is configured on the PCB through a simple discrete resistor. The Critical/Thermal Shutdown function is described in more detail in Section 5.9, "Critical/Thermal Shutdown".

An example of a typical system configuration for the EMC2112 is provided in Figure 5.1.

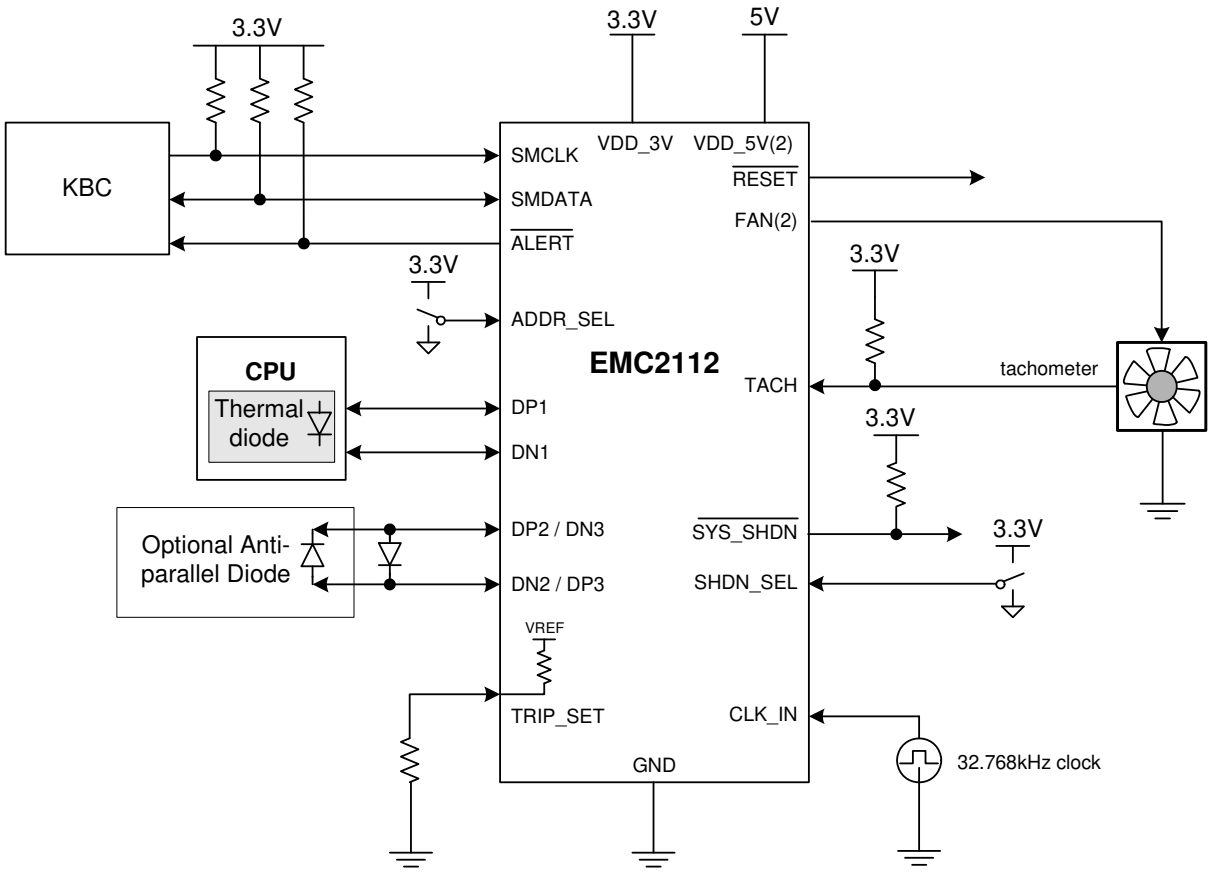

Figure 5.1 EMC2112 System Diagram

5.1 Fan Control Modes of Operation

The EMC2112 has two modes of operation for the fan driver. Each mode of operation uses the Ramp Rate control and Spin Up Routine.

1. Direct Setting Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 6.17) will instantly update the fan drive. Ramp Rate control is optional and enabled via the EN_RRC bits.
   - Whenever the Direct Setting Mode is enabled, the current drive will be changed to what was last written into the Fan Driver Setting Register.
2. Fan Speed Control Mode (FSC) - in this mode of operation, the user determines a target tachometer count and the drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.

Table 5.1 Fan Controls Active for Operating Mode

DIRECT SETTING MODE	FSC MODE
Fan Driver Setting (read / write)	Fan Driver Setting (read only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)
-	RANGE[1:0] (Fan Configuration)
UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Max Step	Fan Max Step
-	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
-	TACH Target (read / write)
TACH Reading	TACH Reading
-	DRIVE_FAIL_CNT[1:0] and Drive Band Fail Registers

5.2 RPM-Based Fan Speed Control Algorithm (FSC)

The EMC2112 includes a RPM-based Fan Speed Control Algorithm for the fan driver.

This fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source.

The desired tachometer count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. This is done by setting the TACH Target Register. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPMs, then the user would input the hexidecimal equivalent of 1296 (51h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs.

The EMC2112's RPM-based Fan Speed Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the $\overline{\text{ALERT}}$ pin. The EMC2112 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal. The fan controller will function either with an externally supplied 32.768KHz clock source or with it's own internal 32kHz oscillator depending on the required accuracy.

5.2.1 Programming the RPM-Based Fan Speed Control Algorithm

The RPM-based Fan Speed Control Algorithm is disabled upon device power up. The following registers control the algorithm. The EMC2112 fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

Note that steps 1 - 6 are optional and need only be performed if the default settings do not provide the desired fan response.

1. Set the Spin Up Configuration Register to the Spin Up Level and Spin Time desired.
2. Set the Fan Step Register to the desired step size.
3. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
4. Set the Update Time, and Edges options in the Fan Configuration Register.
5. Set the Valid TACH Count Register to the highest tach count that indicates the fan is spinning.
6. Set the TACH Target Register to the desired tachometer count.
7. Enable the RPM-based Fan Speed Control Algorithm by setting the EN_ALGO bit.

5.3 Tachometer Measurement

The tachometer measurement circuitry is used in conjunction with the RPM-based Fan Speed Control Algorithm to update the fan driver output. Additionally, it can be used in Direct Setting mode as a diagnostic for host based fan control.

This method monitors the TACH signal in real time. It constantly updates the tachometer measurement by reporting the number of clocks between a user programmed number of edges on the TACH signal.

The tachometer measurement provides fast response times for the RPM-based Fan Speed Control Algorithm and the data is presented as a count value that represents the fan RPM period. When this method is used, all fan target values must be input as a count value for proper operation.

APPLICATION NOTE: The tachometer measurement method works independently of the drive settings. If the device is put into Direct Setting and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

5.3.1 Stalled Fan

A Stalled fan is detected if the tach counter exceeds the user-programmable Valid TACH Count setting then it will flag the fan as stalled and trigger an interrupt.

If the RPM-based Fan Speed Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Direct Setting Mode is enabled or whenever the Spin Up Routine is enabled, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Section 6.21) to allow the fan an opportunity to reach a valid speed without generating unnecessary interrupts.
- In Direct Setting Mode with the tachometer measurement using the Tach Period Measurement method, whenever the TACH Reading Register value exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When using the RPM-based Fan Speed Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

5.3.2 Aging Fan or Invalid Drive Detection

This is useful to detect aging fan conditions (where the fan's natural maximum speed degrades over time) or incorrect fan speed settings. The EMC2112 contains circuitry that detects that the programmed fan speed can be reached by the fan. If the target fan speed cannot be reached within a user defined band of tach counts at maximum drive then the DRIVE_FAIL status bits are set and the $\overline{\text{ALERT}}$ pin is asserted.

5.3.3 Clock Source

The CLK pin can be configured as an input for the EMC2112 or as an output to drive additional devices with the internally generated tachometer clock (see Section 6.9).

When the CLK pin is configured as an input to the EMC2112, then a 32.768kHz clock must be provided. This clock is used to by the Tachometer measurement circuitry and will directly affect the accuracy of this measurement.

When the CLK pin is configured as an output, then it will be driven at the same frequency as the internal tachometer clock.

5.4 Spin Up Routine

The EMC2112 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation.

The Spin Up Routine is initiated in Direct Setting mode when the setting value changes from 00h to anything else.

When the Fan Speed Control Algorithm is enabled, the Spin Up Routine is initiated under the following conditions when the Tach Period Measurement method of tach measurement is used:

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 6.24).
2. The RPM-based Fan Speed Control Algorithm's measured TACH Reading Register value is greater than the Valid TACH Count setting.

When the Spin Up Routine is operating, the fan driver is set to full scale (optional) for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (30% through 65% drive).

After the Spin Up Routine has finished, the EMC2112 measures the TACH signal. If the measured TACH Reading Register value is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 5.2 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

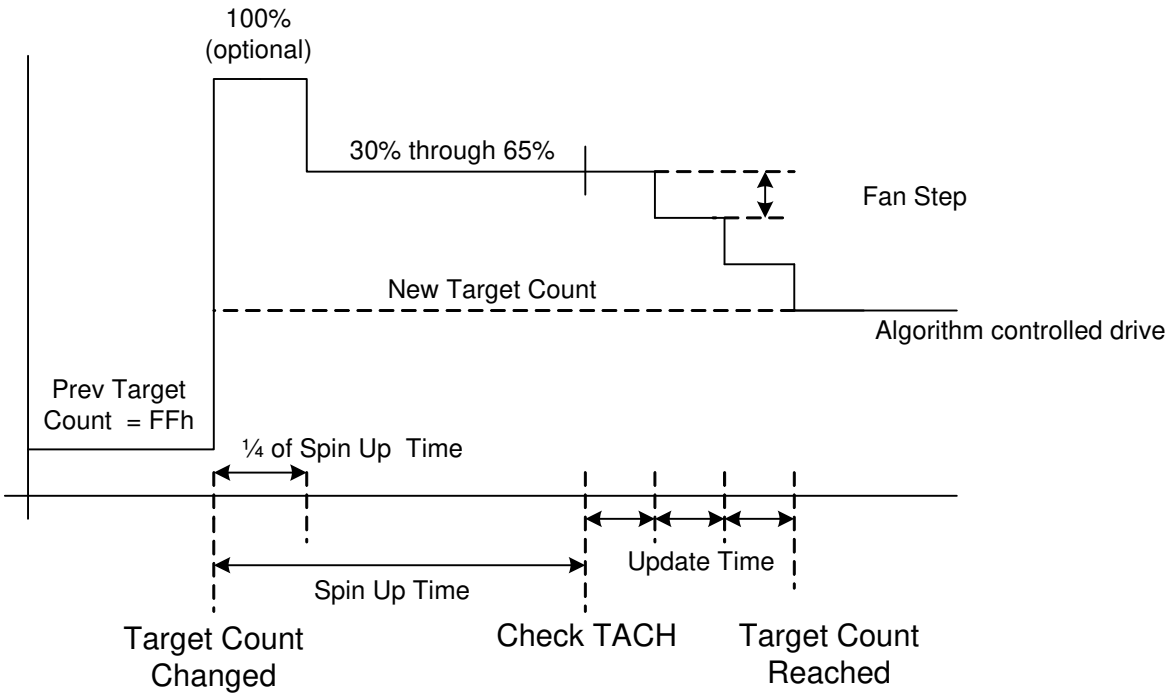

Figure 5.2 Spin Up Routine

5.5 Ramp Rate Control

The Fan Driver can be configured with automatic ramp rate control. Ramp rate control is accomplished by adjusting the drive output settings based on the Maximum Fan Step Register settings and the Update Time settings.

If the RPM-based Fan Speed Control Algorithm is used, then this ramp rate control is automatically used. The user programs a maximum step size for the fan drive setting and an update time. The update time varies from 100ms to 1.6s while the fan drive maximum step can vary from 1 count to 31 counts.

When a new fan drive setting is entered, the delta from the next fan drive setting and the previous fan drive setting is determined. If this delta is greater than the Max Step settings, then the fan drive setting is incrementally adjusted every 100ms to 1.6s as determined by the Update Time until the target fan drive setting is reached. See Figure 5.3.

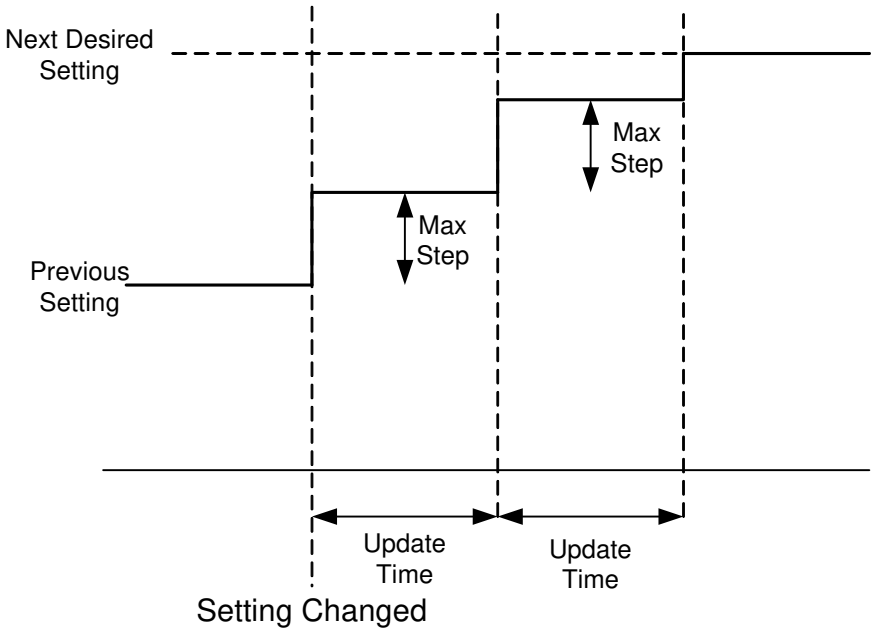

Figure 5.3 Ramp Rate Control

5.5.1 Temperature Bypass of Ramp Rate Control

As an optional feature, the Ramp Rate Control functionality can be disabled if any of the measured temperature channels exceed their respective high limits. In this mode, once the high limit has been exceeded, the ramp rate controls are removed which allows the fan to move instantly to the programmed drive setting (using the FSC or in manual mode).

5.6 Watchdog Timer

The EMC2112 contains an internal Watchdog Timer for the fan driver. The Watchdog timer monitors the SMBus traffic for signs of activity and works in two different modes based upon device operation. These modes are Power Up Operation and Continuous Operation as described below.

For either mode of operation, if four (4) seconds elapse without activity detected by the host, then the watchdog will be triggered and the following will occur:

1. The WATCH status bit will be set which will cause the $\overline{\text{ALERT}}$ pin to be asserted.
2. The fan driver will be set to full scale drive. It will remain at full scale drive until it is disabled.

APPLICATION NOTE: When the Watchdog timer is activated the Fan Speed Control Algorithm is automatically disabled. Disabling the Watchdog will not automatically set the fan drive nor re-activate the Fan Speed Control Algorithm. This must be done manually.