Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

EMC2113

RPM-Based Fan Controller with Multiple Temperature Zones & Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2113 is an SMBus compliant fan controller. The fan driver can be operated using two methods, each with two modes. The methods include an RPM-based Fan Speed Control Algorithm and a direct PWM drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The EMC2113 includes a temperature monitor that measures up to three (3) external diodes and the internal diode. The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors.

The device includes high and low limits for all temperature channels as well as a hardware set critical temperature limit. This hardware set limit drives a dedicated system shutdown pin.

Finally, the device includes an open-drain, active low interrupt pin to flag temperature or fan control errors.

Applications

- Notebook Computers
- Projectors
- Graphics Cards
- Industrial and Networking Equipment

Features

- Programmable Fan Control circuit
  - 4-wire fan compatible
  - Both Low and High frequency PWM
- RPM-based fan control algorithm
  - 2% accurate from 500 RPM to 16k RPM
  - Automatic Tachometer feedback
- Temperature Look-Up Table
  - Controls fan speed or PWM drive setting
  - Eight steps that incorporate up to four temperature zones simultaneously (user selectable)
  - Supports forced DTS or standard temperature data
  - Allows external PWM input (150Hz to 40kHz)
- Up to Three External Temperature Channels
  - Supports transistor model for 90nm - 45nm Intel CPUs
  - Resistance Error Correction and Beta Compensation
  - 1°C accurate (60°C to 125°C)
  - 0.125°C resolution
  - Programmable High and Low limits
- Hardware Programmable Thermal Shutdown Temperature
  - Cannot be altered by software
  - 65°C to 127°C Range
  - Dedicated system shutdown interrupt pin
- Internal Temperature Monitor
  - ±1°C accuracy
  - 0.125°C resolution
- 3.3V Supply Voltage
- Open drain interrupt pin
- SMBus 2.0 Interface
  - SMBus Alert compatible
  - Selectable SMBus Address via pull-up resistor and ADDR_SEL pin
  - Block Read and Write
- Available in 16-pin 4mm x 4mm QFN RoHS Compliant package

ORDERING INFORMATION:

ORDERING NUMBER	PACKAGE	FEATURES
EMC2113-1-AP-TR	16-pin 4mm x4mm QFN (ROHS Compliant)	RPM-based Fan Speed Control Algorithm, High Frequency PWM driver, HW Thermal / Critical shutdown

This product meets the halogen maximum concentration values per IEC61249-2-21

Table of Contents

Table of Figures

List of Tables

Chapter 1 Block Diagram

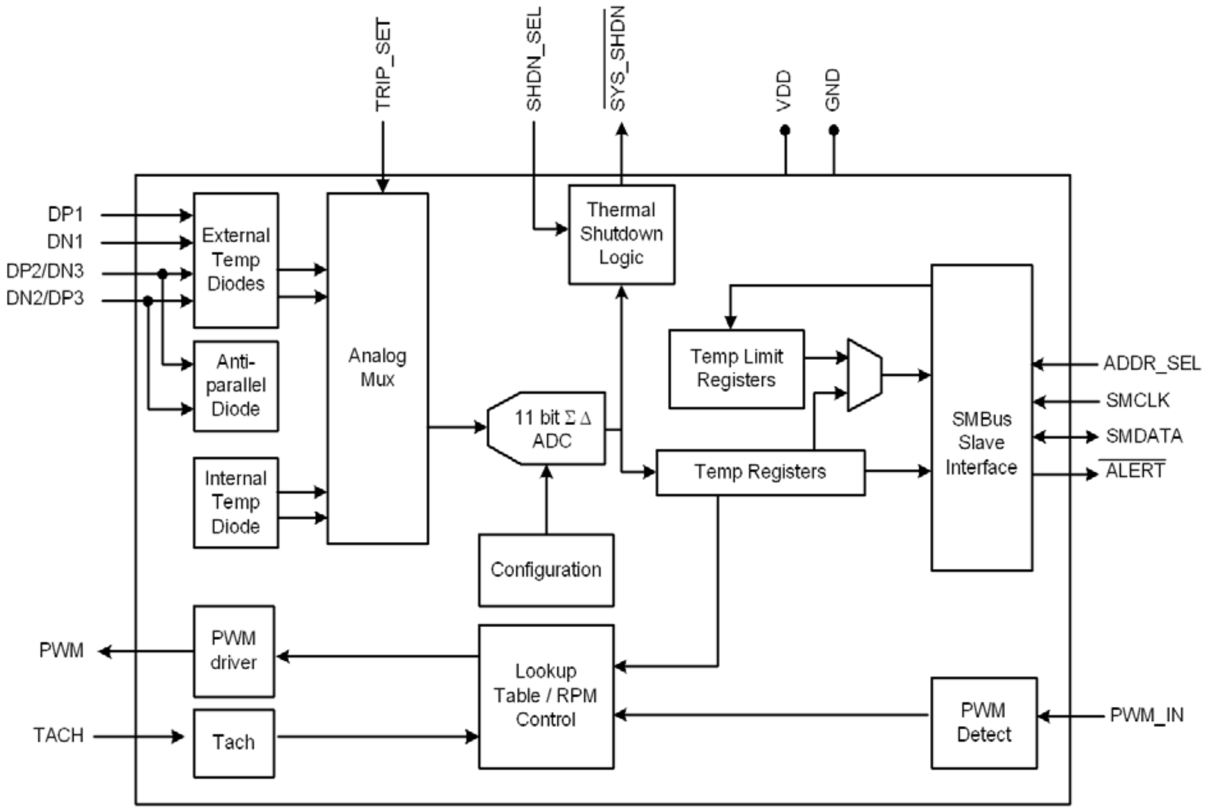

Figure 1.1 EMC2113 Block Diagram

Chapter 2 Delta from EMC2103

The EMC2113 is compatible with the EMC2103-2 with the following changes:

- Removed two GPIOs - Pins 4 and 5 of the EMC2103-2 were GPIO pins. These have been removed.
- Added PWM Input functionality - This functionality allows the user to drive a PWM input into the EMC2113. The duty cycle of the PWM represents a temperature value and can be used as an input to the Fan Control Look Up Table.
- Added ADDR_SEL functionality - This functionality allows the user to choose one of six SMBus address options.
- Updated Hysteresis within Look Up Table - The Fan Control Look Up Table in the EMC2113 allows the user to program a different hysteresis value to apply to each temperature input channel instead of a single hysteresis value that applies to all temperature input channels.
- Updated input muxing for the Look Up Table - The Fan Control Look Up Table has more options over which temperature channel is used for fan control.
- Updated HW set shutdown functionality to include option for Internal diode
- Added control to disable Ramp Rate control if one or more temperatures exceed the high limit
- Added SMBus Block Read and Write capability

Table 2.1 LUT Options

TEMPERATURE INPUT	EMC2113 OPTIONS
Temperature Column 1	External Diode 1 -or- Pushed Temperature 1
Temperature Column 2	External Diode 2
Temperature Column 3	External Diode 3 -or- Pushed Temperature 1
Temperature Column 4	Internal Diode -or- Pushed Temperature 2

Chapter 3 Pin Layout

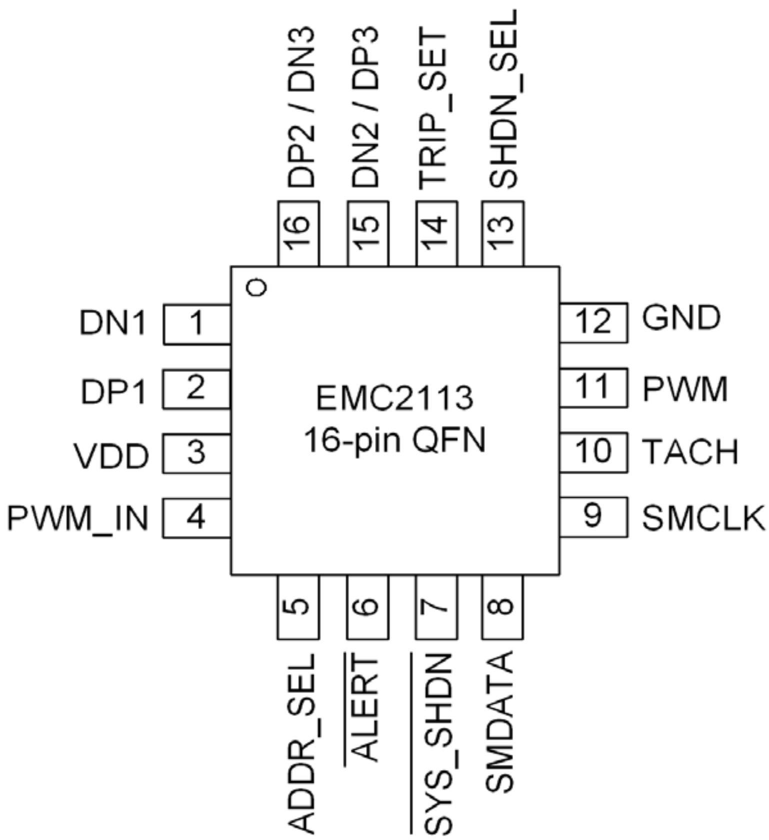

Figure 3.1 EMC2113-1 Pin Diagram (16-Pin QFN)

Table 3.1 Pin Description for EMC2113-1

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
1	DN1	Negative (cathode) analog input for External Diode 1	AIO
2	DP1	Positive (anode) analog input for External Diode 1	AIO
3	VDD	Power Supply	Power
4	PWM_IN	PWM input signal from host	DI (5V)
5	ADDR_SEL	Address Select Input	AIO
6	$\overline{\text{ALERT}}$	Active low SMBus slave interrupt - requires external pull-up resistor.	OD (5V)
7	$\overline{\text{SYS\_SHDN}}$	Active low Critical/Thermal Shutdown output - requires external pull-up resistor	OD (5V)

Table 3.1 Pin Description for EMC2113-1 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
8	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
9	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
10	TACH	Tachometer input for the Fan	DI (5V)
11	PWM	PWM - Open Drain PWM drive output for the Fan (default)	OD (5V)
		PWM - Push Pull PWM drive output for the fan	DO
12	GND	Ground	Power
13	SHDN_SEL	Selects the hardware shutdown channel and operating mode	AIO
14	TRIP_SET	Voltage input to set the Critical/Thermal Shutdown threshold	AIO
15	DN2 / DP3	DN2 - Negative (cathode) connection for External Diode 2	AIO
		DP3 - Positive (anode) connection for External Diode 3	AIO
16	DP2 / DN3	DP2 - Positive (anode connection for External Diode 2	AIO
		DN3 - Negative (cathode) connection for External Diode 3	AIO

The pin types are described in detail below. All pins labelled with (5V) are 5V tolerant.

Note: For all 5V tolerant pins that require a pull-up resistor, the pull-up voltage cannot exceed 3.6V when the device is unpowered.

Table 3.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIO	Digital Input / Output this pin is used as a digital I/O. It can both source and sink current.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 4 Electrical Characteristics

Table 4.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins (V_{PULLUP})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{PULLUP} - V_{DD}\|$) See Note 4.1	0 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to V_{DD} + 0.3	V
Package Power Dissipation	0.8W up to T_A = 85°C	W
Junction to Ambient (θ_{JA})	50	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note: All voltages are relative to ground.

Note: θ_{JA} numbers are based on a recommended four 12 mil vias connecting the thermal pad to PCB ground.

Note 4.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the EMC2113 is unpowered.

4.1 Electrical Specifications

Table 4.2 Electrical Specifications

VDD = 3V to 3.6V, T_A = -40°C to 125°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		1.1	1.5	mA	4 Conversions/second, Fan Driver active at maximum PWM frequency, Dynamic Averaging Enabled
			0.7	1.1	mA	1 Conversion/second, Fan Driver not active, Dynamic Averaging Disabled
First Conversion Ready	t_{CONV_T}		150	300	ms	Time after power up before all channels updated
SMBus Delay	t_{SMB_D}		10	15	ms	Time before SMBus communications should be sent by host
External Temperature Monitors						
Temperature Accuracy			±0.5	±1	°C	60°C < T_{DIODE} < 125°C 30°C < T_A < 100°C
			±1	±2	°C	-40°C < T_{DIODE} < 125°C
Temperature Resolution			0.125		°C	
Diode decoupling capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Resistance Error Corrected	R_{SERIES}		100		Ohm	Sum of series resistance in both DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy	T_A		±0.5	±1	°C	40°C < T_A < 100°C
			±1	±2	°C	
Temperature Resolution			0.125		°C	
RPM-Based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
RPM Control Accuracy	Δ_{TACH}		±1	±2	%	
PWM Fan Driver						
PWM Resolution	PWM		256		Steps	
PWM Duty Cycle	DUTY	0		100	%	

Table 4.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, T_A = -40°C to 125°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
PWM Input Detection						
PWM Frequency	f_{PWM_IN}	150		40k	Hz	
TRIP_SET Measurement						
TRIP_SET Decode Accuracy	V_{TRIP}		±0.5	±1	°C	1% resistor connected to ground
TRIP_SET Decode Accuracy	V_{TRIP}		±1	±2	°C	5% resistor connected to ground
Digital I/O pins						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	8 mA current drive
Output Low Voltage	V_{OL}			0.4	V	8 mA current sink
Leakage Current	I_{LEAK}			±5	uA	$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins Device powered or unpowered T_A < 85°C

4.2 SMBus Electrical Specifications

Table 4.3 SMBus Electrical Specifications

VDD= 3V to 3.6V, T_A = -40°C to 125°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Device powered or unpowered T_A < 85°C
Input Capacitance	C_{IN}		4	10	pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	

Table 4.3 SMBus Electrical Specifications (continued)

VDD= 3V to 3.6V, T_A = -40°C to 125°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	Total per bus line

Chapter 5 SMBus Slave Interface

The EMC2113 communicates with a host controller, such as an SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices.

5.1 System Management Bus Interface Protocol

The EMC2113 contains an SMBus slave interface. A detailed timing diagram is shown in Figure 5.1, "SMBus Timing Diagram". Stretching of the SMCLK signal is supported, however the EMC2113 will not stretch the clock signal.

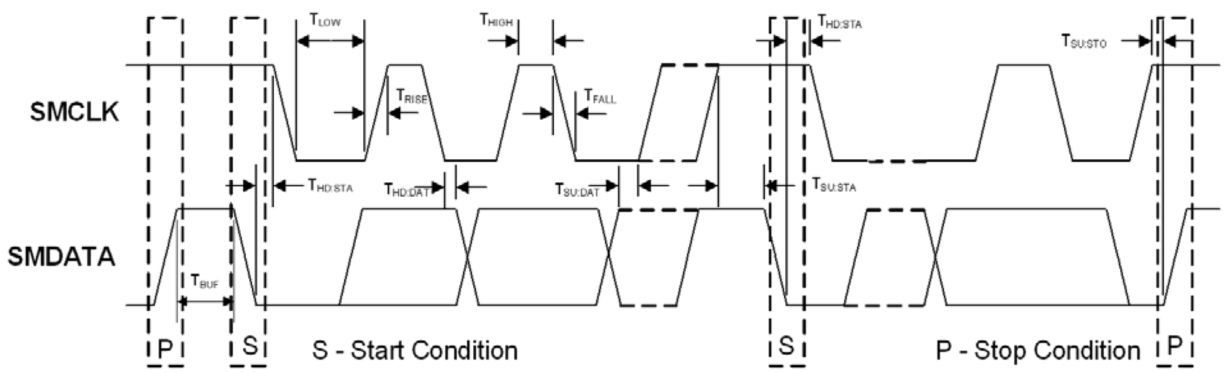

Figure 5.1 SMBus Timing Diagram

5.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

5.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit slave address followed by the RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the host device is writing data to the slave device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the host device is reading data from the slave device.

The EMC2113 SMBus slave address is determined via the pull-up resistor connected to the ADDR_SEL pin as shown Table 5.1, "ADDR_SEL Pin Decode".

Table 5.1 ADDR_SEL Pin Decode

PULL-UP RESISTOR VALUE	FAN CONTROL ADDRESS
4.7k Ohm ±5%	0101_100(r/w)
6.8k Ohm ±5%	0101_101(r/w)
10k Ohm ±5%	0101_110(r/w)
15k Ohm ±5%	1001_100(r/w)

Table 5.1 ADDR_SEL Pin Decode (continued)

PULL-UP RESISTOR VALUE	FAN CONTROL ADDRESS
22k Ohm ±5%	1001_101(r/w)
33k Ohm ±5%	1001_000(r/w)

5.1.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

5.1.4 SMBus ACK and NACK Bits

The SMBus slave will acknowledge all data bytes that it receives. This is done by the slave device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The Host will NACK (not acknowledge) the last data byte to be received from the slave by holding the SMBus data line high after the 8th data bit has been sent.

5.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC2113 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its slave interface and prepare to receive further communications.

5.1.6 SMBus Time-out

The EMC2113 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The SMBus timeout defaults to enabled and can be disabled by setting the DIS_TO bit (see Section 7.12, "Configuration 2 Register").

5.1.7 SMBus and I^2C Compliance

The major difference between SMBus and I^2C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The slave protocol will reset if the clock is held low longer than 30ms.
3. The slave protocol will reset if both the clock and the data line are high for longer than 150us (idle condition).
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

5.2 SMBus Protocols

The EMC2113 slave interface is SMBus 2.0 compatible and support Send Byte, Read Byte, Receive Byte, Write Byte, Block Read Byte, Block Write Byte, and the Alert Response Address as valid protocols. These protocols are used as shown below.

All of the below protocols use the convention in Table 5.2, "Protocol Format". For the Slave Address fields, the value of YYYY_YYY represents the programmed SMBus address.

Table 5.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

5.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 5.3.

Table 5.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYY	0	0	0 -> 1	0	XXh	0	0 -> 1

5.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 5.4.

Table 5.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

5.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 5.5.

Table 5.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	1	0 -> 1

5.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 5.6.

Table 5.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

5.2.5 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 5.7. It is an extension of the Write Byte Protocol.

Table 5.7 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

5.2.6 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 5.8. It is an extension of the Read Byte Protocol.

Table 5.8 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

5.2.7 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100b. All devices with active interrupts will respond with their slave address as shown in Table 5.9.

Table 5.9 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	YYYY_YYY	1	0 -> 1

The EMC2113 slave interface will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

Chapter 6 Product Description

The EMC2113 is an SMBus compliant fan controller with up to three (3) external and one (1) internal temperature channels. The fan driver can be operated using two methods, each with two modes. The methods include an RPM-based Fan Speed Control Algorithm and a direct PWM drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors (including support of the BJT or transistor model for a CPU diode).

The EMC2113 allows the user to program temperatures generated from external sources to control the fan speed. This functionality also supports DTS data from the CPU. By pushing DTS or standard temperature values into dedicated registers, the external temperature readings can be used in conjunction with the external diode(s) and internal diode to control the fan speed.

The EMC2113 also allows the user to input a PWM input signal on the PWM_IN pin that is used as an input to the Fan Speed Control Look Up Table.

The EMC2113 includes a hardware programmable temperature limit and dedicated system shutdown output for thermal protection of critical circuitry.

Figure 6.1 shows a system diagram of the EMC2113.

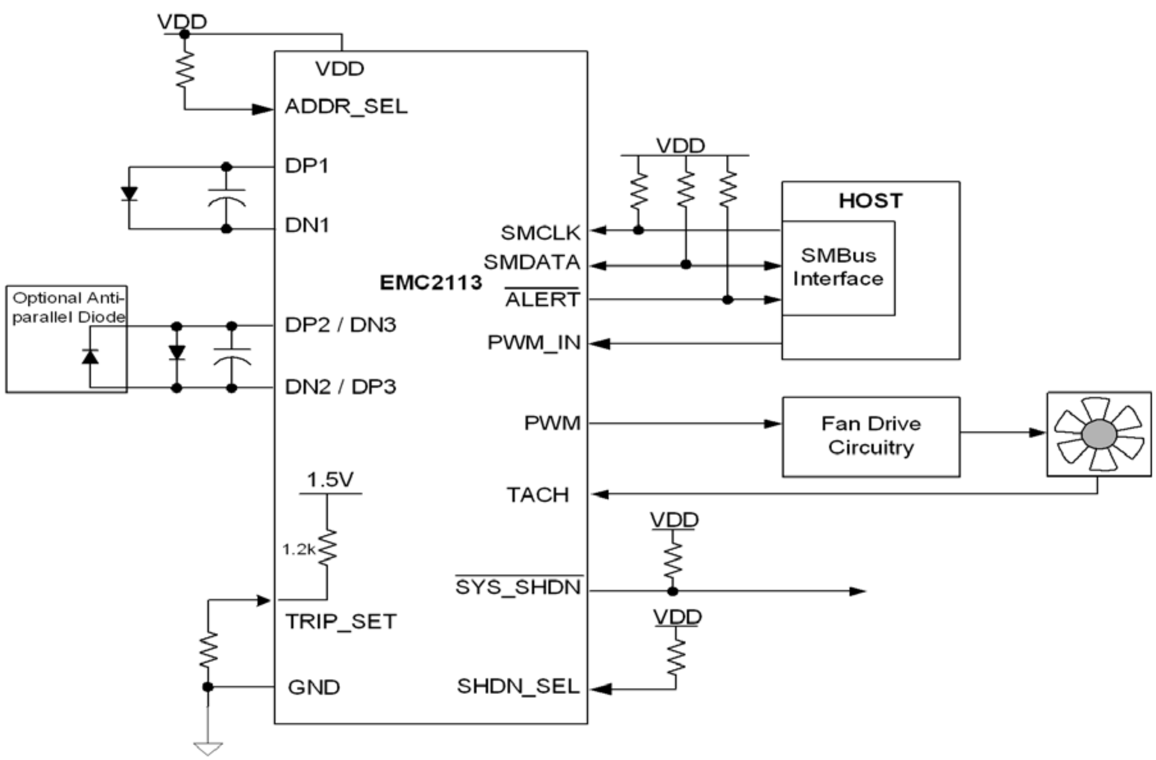

Figure 6.1 System Diagram for EMC2113

6.1 Critical/Thermal Shutdown

The EMC2113 provides a hardware Critical/Thermal Shutdown function for systems. Figure 6.2 is a block diagram of this Critical/Thermal Shutdown function. The Critical/Thermal Shutdown function accepts configuration information from the pullup resistor of the SHDN_SEL pin.

The analog portion of the Critical/Thermal Shutdown function monitors the hardware determined shutdown channel. This measured temperature is then compared with TRIP_SET point. This TRIP_SET point is set by the system designer with a single external resistor.

The $\overline{\text{SYS\_SHDN}}$ is asserted when the indicated temperature meets or exceeds the temperature threshold (T_{TRIP}) established by the TRIP_SET input pin for a number of consecutive measurements defined by the fault queue.

Each of the software programmed temperature limits can be optionally configured to act as inputs to the Critical/Thermal Shutdown independent of the hardware shutdown operation. When configured to operate this way, the $\overline{\text{SYS\_SHDN}}$ pin will be asserted when the temperature meets or exceeds the programmed Tcrit Limit for the enabled channel (see Section 7.10).

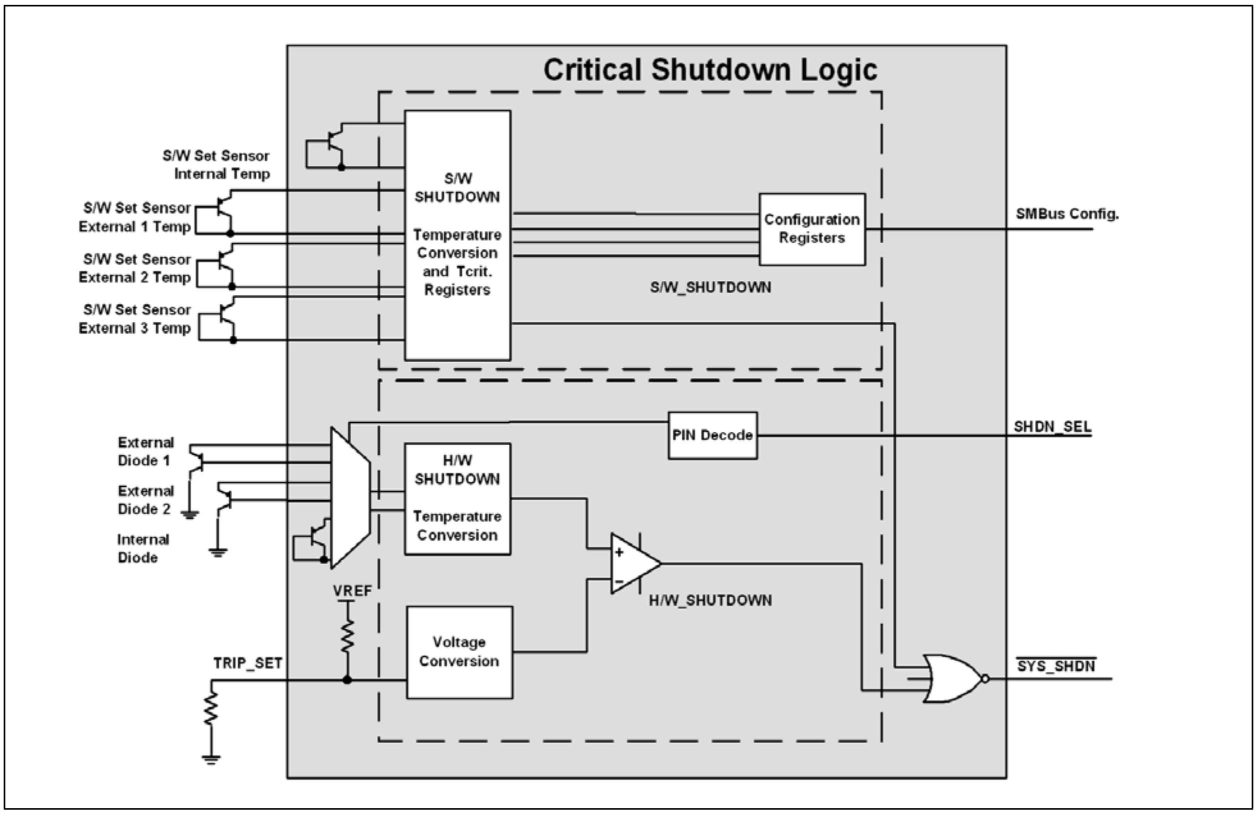

Figure 6.2 Block Diagram of Critical/Thermal Shutdown

6.1.1 $\overline{\text{SYS\_SHDN}}$ Pin

The $\overline{\text{SYS\_SHDN}}$ pin is an active low dedicated system interrupt. This pin is asserted low when:

1. The programmed temperature channel (see Section 6.1.2) exceeds the hardware set limit (see Section 6.1.3).
2. Any of the measured temperature channels meet or exceed their programmed TCRIT limits and have been linked to the $\overline{\text{SYS\_SHDN}}$ pin (see Section 7.10).
3. Any of the measured temperature channels meet or exceed their programmed High limits and have been linked to the SYS_SHDN pin (see Section 7.11).

When the SYS_SHDN pin is asserted, it will remain asserted until the measured temperatures drop below the respective limits minus the hysteresis. At this point, the pin will be released automatically.

6.1.2 SHDN_SEL Pin

The EMC2113 has a 'strappable' input (SHDN_SEL) allowing for configuration of the hardware Critical/Thermal Shutdown input channel. The pull-up resistor used on this pin identifies which configuration setting is used as shown in Table 6.1, "SHDN_SEL Pin Decode".

.

Table 6.1 SHDN_SEL Pin Decode

PULL UP RESISTOR	MODE / DIODE CHANNEL	EXTERNAL DIODE 1 CONFIG	EXTERNAL DIODE 2 CONFIG
≤ 4.7k Ohm	AMD CPU on External Diode 1	Beta Compensation disabled REC disabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
6.8k Ohm	2N3904 on External Diode 1	Beta Compensation disabled REC enabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
10k Ohm	Intel CPU or 2N3904 on External Diode 1	Beta Compensation enabled (auto) REC enabled Beta and REC controls are locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
15k Ohm	Internal Diode	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked
22k Ohm	Intel CPU or 2N3904 on External Diode 2	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are locked
≥ 33k Ohm	Intel CPU or 2N3904 on External Diode 1	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked	Beta Compensation enabled (auto) REC enabled Beta and REC controls are not locked

APPLICATION NOTE: The SHDN_SEL pin decode settings with Beta Compensation enabled (auto) will support a diode connected 2N3904 diode normally.

6.1.3 TRIP_SET Pin

The EMC2113's TRIP_SET pin is an analog input to the Critical/Thermal Shutdown block which sets the Thermal Shutdown temperature. The system designer creates a voltage level at the input through a simple resistor connected to GND as shown in Figure 6.2, "Block Diagram of Critical/Thermal Shutdown". The value of this resistor is used to create an input voltage on the TRIP_SET pin which is translated into a temperature ranging from 65°C to 127°C.

APPLICATION NOTE: Current only flows when the TRIP_SET pin is being monitored. At all other times, the internal reference voltage is removed and the TRIP_SET pin will be pulled down to ground.

APPLICATION NOTE: The TRIP_SET pin circuitry is designed to use a 1% resistor externally. Using a 1% resistor will result in the Thermal / Critical Shutdown temperature being decoded correctly. If a 5% resistor is used, then the Thermal / Critical Shutdown temperature may be decoded with as much as ±1°C error.

Table 6.2 TRIP_SET Resistor Setting

T_{TRIP} (°C)	RSET (1%)	T_{TRIP} (°C)	RSET (1%)
65	0.0	97	1240
66	28.7	98	1330
67	48.7	99	1400
68	69.8	100	1500
69	90.9	101	1580
70	113	102	1690
71	137	103	1820
72	158	104	1960
73	182	105	2050
74	210	106	2210
75	237	107	2370
76	261	108	2550
77	294	109	2740
78	324.	110	2940
79	348	111	3160
80	383	112	3480
81	412	113	3740
82	453	114	4120
83	487	115	4530
84	523	116	4990
85	562	117	5490
86	604	118	6040
87	649	119	6810
88	698	120	7870
89	750	121	9090
90	787	122	10700
91	845	123	12700
92	909	124	15800
93	953	125	20500