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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# EMC2302

# Dual RPM-Based PWM Fan Controller

## PRODUCT FEATURES

**Datasheet**

### General Description

The EMC2302 is an SMBus compliant fan controller with up to two independently controlled PWM fan drivers. Each fan driver is controlled by a programmable frequency PWM driver and Fan Speed Control algorithm that operates in either a closed loop fashion or as a directly PWM-controlled device.

The closed loop Fan Speed Control algorithm (FSC) has the capability to detect aging fans and alert the system. It will likewise detect stalled or locked fans and trigger an interrupt.

Additionally, the EMC2302 offers a clock output so that multiple devices may be chained and slaved to the same clock source for optimal performance in large distributed systems.

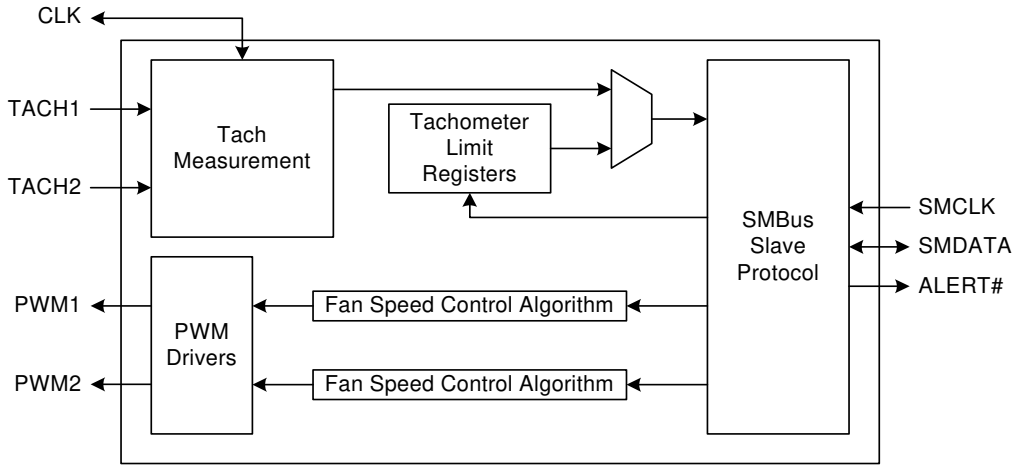
### Applications

- Servers
- Projectors
- Industrial and Networking Equipment
- Notebook Computers

### Features

- Two Programmable Fan Control circuits (EMC2302)
  - 4-wire fan compatible
  - High speed PWM (26 kHz)
  - Low speed PWM (9.5Hz - 2240 Hz)
  - Optional detection of aging fans
  - Fan Spin Up Control and Ramp Rate Control
  - Alert on Fan Stall
- Watchdog Timer
- RPM-based fan control algorithm
  - 0.5% accuracy from 500 RPM to 16k RPM (external crystal oscillator)
  - 1% accuracy from 500 RPM to 16k RPM (internal clock)
- SMBus 2.0 Compliant
  - SMBus Alert compatible
- CLK Pin can provide a clock source output
- Available in a 10-pin MSOP Lead-free RoHS Compliant package

### Block Diagram



**Order Number(s):**

| ORDERING NUMBER | PACKAGE | FEATURES |
|---|---|---|
| EMC2302-1-AIZL-TR | 10-pin MSOP (Lead-free RoHS compliant) | Two RPM-based fan speed control algorithms. SMBus address 0101_110(r/w) |
| EMC2302-2-AIZL-TR | 10-pin MSOP (Lead-free RoHS compliant) | Two RPM-based fan speed control algorithms. SMBus address 0101_111(r/w) |

**This product meets the halogen maximum concentration values per IEC61249-2-21**

**For RoHS compliance and environmental information, please visit www.smsc.com/rohs**

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

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# Chapter 1 Pin Description

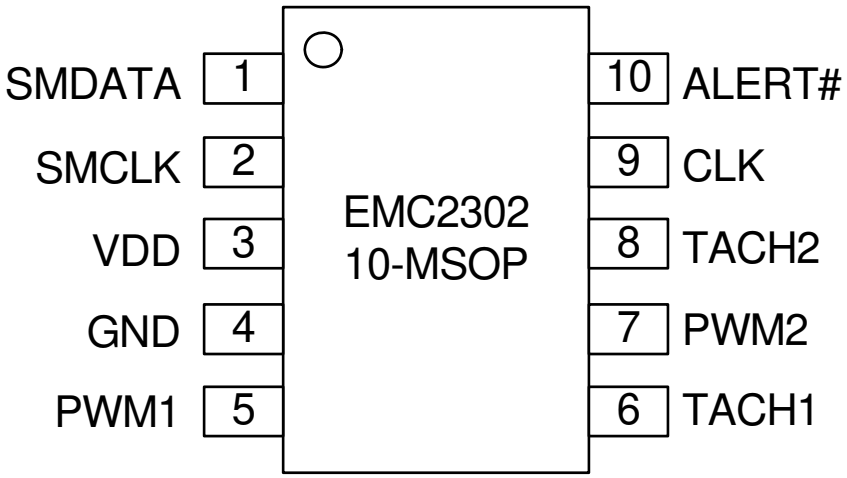


**Figure 1.1 EMC2302 Pin Diagram (10-Pin MSOP)**

**Table 1.1 Pin Description for EMC2302**

| PIN NUMBER | PIN NAME | PIN FUNCTION | PIN TYPE |
|---|---|---|---|
| 1 | SMDATA | SMBus data input/output - requires external pull-up resistor | DIOD (5V) |
| 2 | SMCLK | SMBus clock input - requires external pull-up resistor | DI (5V) |
| 3 | VDD | Power Supply | Power |
| 4 | GND | Ground | Power |
| 5 | PWM1 | Push-Pull PWM output driver for Fan 1 | DO |
| | | Open Drain PWM output driver for Fan 1 | OD (5V) |
| 6 | TACH1 | Open drain tachometer input for Fan 1- requires pull-up resistor | DI (5V) |
| 7 | PWM2 | Push-Pull PWM output driver for Fan 2 | DO |
| | | Open Drain PWM output driver for Fan 2 | OD (5V) |
| 8 | TACH2 | Open drain tachometer input for Fan 2 - requires pull-up resistor | DI (5V) |

**Table 1.1 Pin Description for EMC2302 (continued)**

| PIN NUMBER | PIN NAME | PIN FUNCTION | PIN TYPE |
|---|---|---|---|
| 9 | CLK | Clock input for tachometer measurement | DI (5V) |
| | | Push Pull Clock output to other fan controllers to synchronize Fan Speed Control | DO |
| 10 | ALERT# | Active low interrupt - requires external pull-up resistor. | OD (5V) |

The pin types are described in detail below. All pins labeled with (5V) are 5V tolerant.

**APPLICATION NOTE:** For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the 5V tolerant pad must never be more than 3.6V.

**Table 1.2 Pin Types**

| PIN TYPE | DESCRIPTION |
|---|---|
| Power | This pin is used to supply power or ground to the device. |
| DI | Digital Input - this pin is used as a digital input. This pin is 5V tolerant. |
| DO | Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current. |
| DIOD | Digital Input / Open Drain Output this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant. |
| OD | Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant. |

# Chapter 2 Electrical Specifications

**Table 2.1 Absolute Maximum Ratings**

| | | |
|---|---|---|
| Voltage on 5V tolerant pins ($V_{5VT\_pin}$) | -0.3 to 5.5 | V |
| Voltage on 5V tolerant pins ($\|V_{5VT\_pin} - V_{DD}\|$) (see Note 2.1) | 0 to 3.6 | V |
| Voltage on VDD pin | -0.3 to 4 | V |
| Voltage on any other pin to GND | -0.3 to VDD + 0.3 | V |
| Package Thermal Restance - Junction to Ambient ($\theta_{JA}$) | 132 | °C/W |
| Operating Ambient Temperature Range | -40 to 125 | °C |
| Storage Temperature Range | -55 to 150 | °C |
| ESD Rating, All Pins, HBM | 2000 | V |

**Note:** Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

**Note 2.1** For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the EMC2302 is unpowered.

## 2.1 Electrical Specifications

**Table 2.2 Electrical Specifications**

| $V_{DD}$ = 3V to 3.6V, $T_A$ = -40°C to 125°C, all Typical values at $T_A$ = 27°C unless otherwise noted. | | | | | | |
|---|---|---|---|---|---|---|
| **CHARACTERISTIC** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNIT** | **CONDITIONS** |
| DC Power | | | | | | |
| Supply Voltage | $V_{DD}$ | 3 | 3.3 | 3.6 | V | |
| Supply Current | $I_{DD}$ | | 400 | 550 | uA | |
| PWM Fan Driver | | | | | | |
| PWM Resolution | PWM | | 256 | | Steps | |
| PWM Duty Cycle | DUTY | 0 | | 100 | % | |
| RPM-based Fan Controller | | | | | | |
| Tachometer Range | TACH | 480 | | 16000 | RPM | |
| Tachometer Setting Accuracy | $\Delta_{TACH}$ | | ±0.5 | ±1 | % | External oscillator 32.768kHz |
| | $\Delta_{TACH}$ | | ±1 | ±2 | % | Internal Oscillator |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |

**Table 2.2 Electrical Specifications (continued)**

| $V_{DD}$ = 3V to 3.6V, $T_A$ = -40°C to 125°C, all Typical values at $T_A$ = 27°C unless otherwise noted. | | | | | | |
|---|---|---|---|---|---|---|
| **CHARACTERISTIC** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNIT** | **CONDITIONS** |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Output High Voltage | $V_{OH}$ | VDD - 0.4 | | | V | 8 mA current drive |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | 8 mA current sink |
| Leakage current | $I_{LEAK}$ | | | ±5 | uA | ALERT# pin<br>Powered and unpowered<br>0°C < TA < 85°C<br>pull-up voltage ≤ 3.6V |

**Note 2.2** All voltages are relative to ground.

## 2.2 SMBus Electrical Specifications

**Table 2.3 SMBus Electrical Specifications**

| VDD= 3V to 3.6V, $T_A$ = -40°C to 125°C Typical values are at $T_A$ = 27°C unless otherwise noted. | | | | | | |
|---|---|---|---|---|---|---|
| **CHARACTERISTIC** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNITS** | **CONDITIONS** |
| SMBus Interface | | | | | | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Output High Voltage | $V_{OH}$ | VDD - 0.4 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | 4 mA current sink |
| Input High/Low Current | $I_{IH}$ / $I_{IL}$ | | | ±5 | uA | Powered and unpowered<br>0°C < TA < 85°C |
| Input Capacitance | $C_{IN}$ | | 5 | | pF | |
| SMBus Timing | | | | | | |
| Clock Frequency | $f_{SMB}$ | 10 | | 400 | kHz | |
| Spike Suppression | $t_{SP}$ | | | 50 | ns | |
| Bus free time Start to Stop | $t_{BUF}$ | 1.3 | | | us | |
| Setup Time: Start | $t_{SU:STA}$ | 0.6 | | | us | |
| Setup Time: Stop | $t_{SU:STP}$ | 0.6 | | | us | |
| Data Hold Time | $t_{HD:DAT}$ | 0 | | | us | |
| Data Setup Time | $t_{SU:DAT}$ | 0.6 | | | us | |

**Table 2.3 SMBus Electrical Specifications (continued)**

| VDD= 3V to 3.6V, $T_A$ = -40°C to 125°C Typical values are at $T_A$ = 27°C unless otherwise noted. | | | | | | |
|---|---|---|---|---|---|---|
| **CHARACTERISTIC** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNITS** | **CONDITIONS** |
| Clock Low Period | $t_{LOW}$ | 1.3 | | | us | |
| Clock High Period | $t_{HIGH}$ | 0.6 | | | us | |
| Clock/Data Fall time | $t_{FALL}$ | | | 300 | ns | Min = 20+0.1$C_{LOAD}$ ns |
| Clock/Data Rise time | $t_{RISE}$ | | | 300 | ns | Min = 20+0.1$C_{LOAD}$ ns |
| Capacitive Load | $C_{LOAD}$ | | | 400 | pF | per bus line |

# Chapter 3 Communications

## 3.1 System Management Bus Interface Protocol

The EMC2302 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the EMC2302 will not stretch the clock signal.

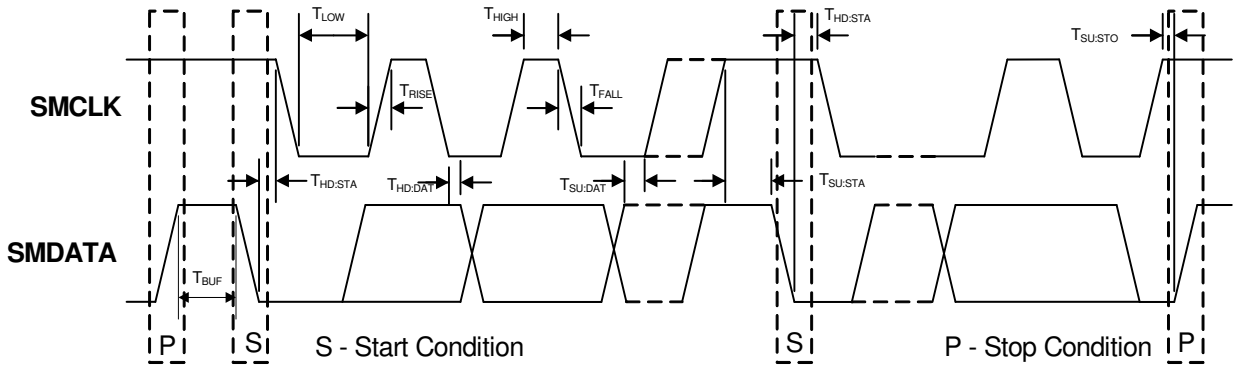


**Figure 3.1 SMBus Timing Diagram**

### 3.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

### 3.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The EMC2302-1 SMBus address is set at 0101_110(r/w)b.

The EMC2302-2 SMBus address is set at 0101_111(r/w)b.

### 3.1.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

### 3.1.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the ALERT# pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The Host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

### 3.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC2302 detects an SMBus Stop bit has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

### 3.1.6 SMBus Time-out

The EMC2302 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The SMBus timeout feature is disabled by default and can be enabled via clearing the DIS_TO bit in the Configuration register (20h).

### 3.1.7 SMBus and $I^2C$ Compliance

The major difference between SMBus and $I^2C$ devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz ($I^2C$ has no minimum frequency).
2. The slave protocol will reset if the clock is held low for longer than 30ms ($I^2C$ has no timeout).
3. The slave protocol will reset if both the clock and data lines are held high for longer than 150us.
4. $I^2C$ devices do not support the Alert Response Address functionality (which is optional for SMBus).
5. The Block Read and Block Write protocols are only compliant with $I^2C$ data formatting. They do not support SMBus formatting for Block Read and Block Write protocols.

## 3.2 SMBus Protocols

The EMC2302 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and Write Byte as valid protocols as shown below. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 3.1. When reading the protocol blocks, the value of YYYY_YYYb should be replaced with the respective SMBus addresses.

**Table 3.1 Protocol Format**

| DATA SENT TO DEVICE | DATA SENT TO THE HOST |
|---|---|
| # of bits sent | # of bits sent |

### 3.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 3.2.

**Table 3.2 Write Byte Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | REGISTER DATA | ACK | STOP |
|---|---|---|---|---|---|---|---|---|
| 1 -> 0 | YYYY_YYYb | 0 | 0 | XXh | 0 | XXh | 0 | 0 -> 1 |

### 3.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.3.

**Table 3.3 Read Byte Protocol**

| START | SLAVE ADDRESS | WR | ACK | Register Address | ACK | START | Slave Address | RD | ACK | Register Data | NACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 -> 0 | YYYY_YYYb | 0 | 0 | XXh | 0 | 0 -> 1 | YYYY_YYYb | 1 | 0 | XXh | 1 | 0 -> 1 |

### 3.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.4.

**Table 3.4 Send Byte Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | STOP |
|---|---|---|---|---|---|---|
| 1 -> 0 | YYYY_YYYb | 0 | 0 | XXh | 0 | 0 -> 1 |

### 3.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.5.

**Table 3.5 Receive Byte Protocol**

| START | SLAVE ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|---|---|---|---|---|---|---|
| 1 -> 0 | YYYY_YYYb | 1 | 0 | XXh | 1 | 0 -> 1 |

### 3.2.5 Block Write Protocol

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 3.6. It is an extension of the Write Byte Protocol.

**Table 3.6 Block Write Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | REGISTER DATA | ACK |
|---|---|---|---|---|---|---|---|
| 1 ->0 | YYYY_YYYb | 0 | 0 | XXh | 0 | XXh | 0 |
| **REGISTER DATA** | **ACK** | **REGISTER DATA** | **ACK** | **. . .** | **REGISTER DATA** | **ACK** | **STOP** |
| XXh | 0 | XXh | 0 | . . . | XXh | 0 | 0 -> 1 |

### 3.2.6 Block Read Protocol

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 3.7. It is an extension of the Read Byte Protocol.

**Table 3.7 Block Read Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | START | SLAVE ADDRESS | RD | ACK | REGISTER DATA |
|---|---|---|---|---|---|---|---|---|---|---|
| 1->0 | YYYY_YYYb | 0 | 0 | XXh | 0 | 1 ->0 | YYYY_YYYb | 1 | 0 | XXh |
| **ACK** | **REGISTER DATA** | **ACK** | **REGISTER DATA** | **ACK** | **REGISTER DATA** | **ACK** | **. . .** | **REGISTER DATA** | **NACK** | **STOP** |
| 0 | XXh | 0 | XXh | 0 | XXh | 0 | . . . | XXh | 1 | 0 -> 1 |

### 3.2.7 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the ALERT# pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 3.8.

**Table 3.8 Alert Response Address Protocol**

| START | ALERT RESPONSE ADDRESS | RD | ACK | DEVICE ADDRESS | NACK | STOP |
|---|---|---|---|---|---|---|
| 1 -> 0 | 0001_100b | 1 | 0 | YYYY_YYYb | 1 | 0 -> 1 |

The EMC2302 will respond to the ARA in the following way if the ALERT# pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the ALERT# pin.

# Chapter 4 Product Description

The EMC2302 is an SMBus compliant fan controller with two programmable frequency PWM fan drivers. The fan drivers can be operated using two modes: the RPM-based Fan Speed Control Algorithm or the direct fan drive setting.

Figure 4.1 shows a system diagram of the EMC2302.

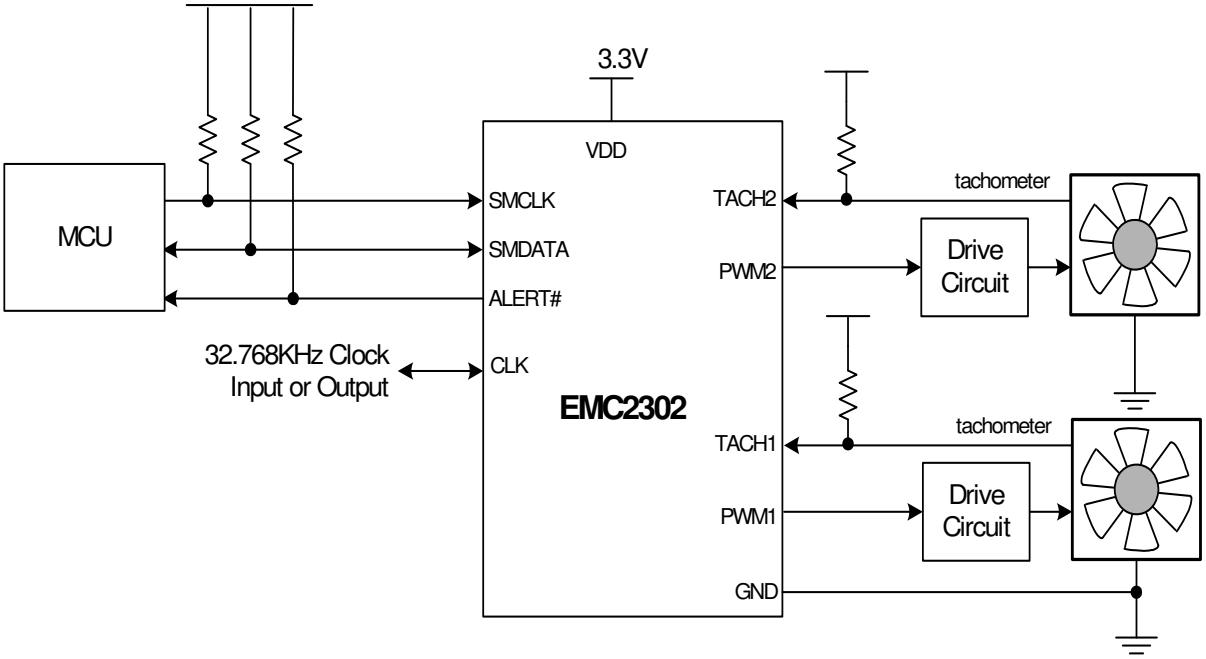


**Figure 4.1 System Diagram of EMC2302**

## 4.1 Fan Control Modes of Operation

The EMC2302 has two modes of operation for each fan driver. Each mode of operation uses the Ramp Rate control and Spin Up Routine.

1. Direct Setting Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 5.7) will instantly update the PWM fan drive. Ramp Rate control is optional and enabled via the EN_RRC bits.
   - Whenever the Direct Setting Mode is enabled, the current drive will be changed to what was last written into the Fan Driver Setting Register.
2. Fan Speed Control Mode (FSC) - in this mode of operation, the user determines a target tachometer count and the PWM drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.
   - This mode is enabled setting the EN_ALGO bit in the Fan Configuration Register.

**Table 4.1 Fan Controls Active for Operating Mode**

| DIRECT SETTING MODE | FSC MODE |
|---|---|
| Fan Driver Setting (read / write) | Fan Driver Setting (read only) |
| EDGES[1:0] | EDGES[1:0]<br>(Fan Configuration) |
| - | RANGE[1:0]<br>(Fan Configuration) |
| UPDATE[2:0]<br>(Fan Configuration) | UPDATE[2:0]<br>(Fan Configuration) |
| LEVEL<br>(Spin Up Configuration) | LEVEL<br>(Spin Up Configuration) |
| SPINUP_TIME[1:0]<br>(Spin Up Configuration) | SPINUP_TIME[1:0]<br>(Spin Up Configuration) |
| Fan Step | Fan Step |
| - | Fan Minimum Drive |
| Valid TACH Count | Valid TACH Count |
| - | TACH Target (read / write) |
| TACH Reading | TACH Reading |
| - | DRIVE_FAIL_CNT[1:0] and Drive Band Fail Registers |

## 4.2 PWM Fan Driver

The EMC2302 supports 2 PWM output drivers. Each output driver can be configured to operate as an open-drain (default) or push-pull driver and each driver can be configured with normal or inverse polarity. Additionally, the PWM frequencies are independently programmable with ranges from 9.5Hz to 26kHz in four programmable frequency bands.

## 4.3 RPM-based Fan Speed Control Algorithm (FSC)

The EMC2302 includes 2 RPM-based Fan Speed Control Algorithms. Each algorithm operates independently and controls a separate fan driver. Each algorithm is controlled manually (by setting the target fan speed).

This fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source.

The desired tachometer count is set by the user inputting the desired number of 32.768kHz cycles that occur per fan revolution. This is done by manually setting the TACH Target Register. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPMs, then the user would input the hexidecimal equivalent of 1296 (51h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs.

The EMC2302's RPM-based Fan Speed Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the ALERT# pin. The EMC2302 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal.

The fan controller will function either with an externally supplied 32.768kHz clock source or with it's own internal 32kHz oscillator depending on the required accuracy. The EMC2302 offers a clock output that enables additional devices to be slaved to the same clock source.

### 4.3.1 Programming the RPM-based Fan Speed Control Algorithm

The RPM-based Fan Speed Control Algorithm is disabled upon device power up. The following registers control the algorithm. The EMC2302 fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

Note that steps 1 - 6 are optional and need only be performed if the default settings do not provide the desired fan response.

1. Set the Spin Up Configuration Register to the Spin Up Level and Spin Time desired.
2. Set the Fan Step Register to the desired step size.
3. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
4. Set the Update Time and Edges options in the Fan Configuration Register.
5. Set the Valid TACH Count Register to the highest tach count that indicates the fan is spinning. Refer to AN17.4 RPM to TACH Counts Conversion for examples and tables for supported RPM ranges (500, 1k, 2k, 4k).
6. Set the TACH Target Register to the desired tachometer count.
7. Enable the RPM-based Fan Speed Control Algorithm by setting the EN_ALGO bit.

## 4.4 Tachometer Measurement

The tachometer measurement circuitry is used in conjunction with the RPM-based Fan Speed Control Algorithm to update the fan driver output. Additionally, it can be used in Direct Setting mode as a diagnostic for host based fan control.

This method monitors the TACHx signal in real time. It constantly updates the tachometer measurement by reporting the number of clocks between a user programmed number of edges on the TACHx signal (see Table 5.12).

The tachometer measurement provides fast response times for the RPM-based Fan Speed Control Algorithm and the data is presented as a count value that represents the fan RPM period.

**APPLICATION NOTE:** The tachometer measurement method works independently of the drive settings. If the device is put into Direct Setting and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

### 4.4.1 Stalled Fan

A Stalled fan is detected if the tach counter exceeds the user-programmable Valid TACH Count setting. If a stall is detected, the device will flag the fan as stalled and trigger an interrupt.

If the RPM-based Fan Speed Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Direct Setting Mode or the Spin Up Routine is enabled, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 5.22) to allow the fan to reach a valid speed without generating unnecessary interrupts.
- In Direct Setting Mode, whenever the TACH Reading Register value exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When using the RPM-based Fan Speed Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

### 4.4.2 Aging Fan or Invalid Drive Detection

This is useful to detect aging fan conditions (where the fan's natural maximum speed degrades over time) or a speed setting that is faster than the fan is capable of. The EMC2302 contains circuitry that detects that the programmed fan speed can be reached by the fan. If the target fan speed cannot be reached within a user defined band of tach counts at maximum drive, the DRIVE_FAIL status bits are set and the ALERT# pin is asserted.

## 4.5 CLK Pin

The CLK pin has multiple functionality as determined by the  settings of the Configuration register.

### 4.5.1 External Clock

The EMC2302 allows the user to choose between supplying an external 32.768kHz clock or use of the internal 32kHz oscillator to measure the tachometer signal. This clock source is used by the RPM-based Fan Speed Control Algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

When this function is used, the external clock is driven into the device via the CLK pin.

### 4.5.2 Internal Clock

Alternately, the EMC2302 may be configured to use its internal clock as a clock output to drive other fan driver devices. When configured to operate in this mode, the device uses its internal clock for tachometer reading and drives the CLK pin using a push-pull driver.

## 4.6 Spin Up Routine

The EMC2302 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation.

The Spin Up Routine is initiated in Direct Setting mode when the setting value changes from 00h to anything else.

When the Fan Speed Control Algorithm is enabled, the Spin Up Routine is initiated under the following conditions:

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 5.15).
2. The RPM-based Fan Speed Control Algorithm's measured TACH Reading Register value is greater than the Valid TACH Count setting.

When the Spin Up Routine is operating, the fan driver is set to full scale (optional) for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set at a user defined level (30% through 65% drive).

After the Spin Up Routine has finished, the EMC2302 measures the TACHx signal. If the measured TACH Reading Register value is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 4.2 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

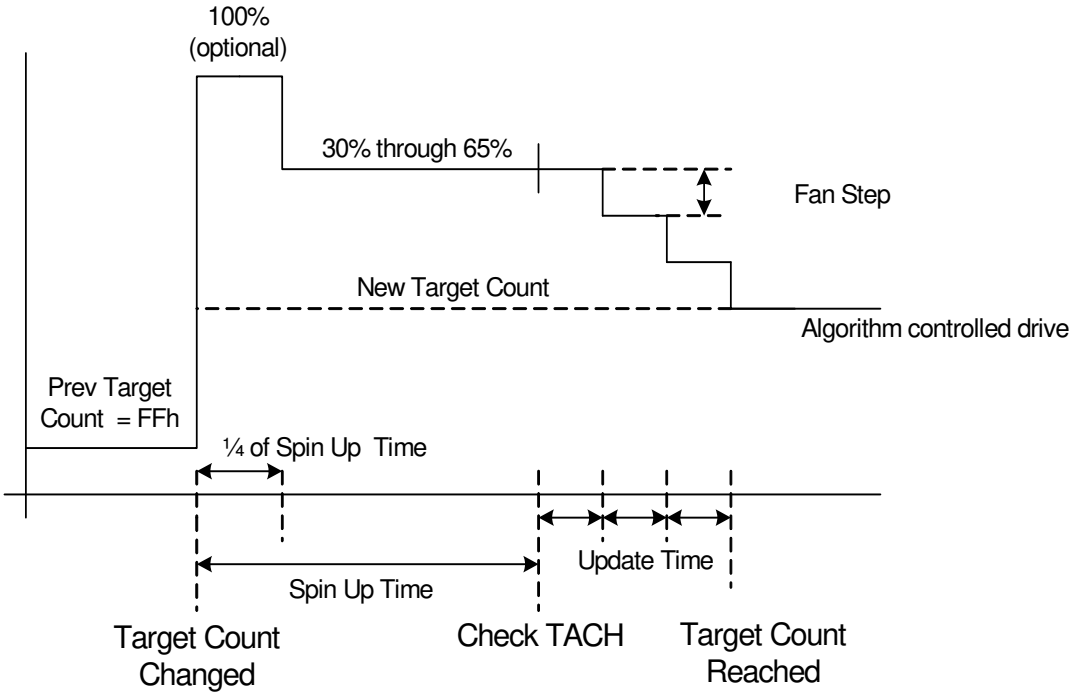


**Figure 4.2 Spin Up Routine**

## 4.7 Ramp Rate Control

The Fan Driver can be configured with automatic ramp rate control. Ramp rate control is accomplished by adjusting the drive output settings based on the Maximum Fan Step Register settings and the Update Time settings.

If the RPM-based Fan Speed Control Algorithm is used, then this ramp rate control is automatically used. The user programs a maximum step size for the fan drive setting and an update time. The update time varies from 100ms to 1.6s while the fan drive maximum step can vary from 1 count to 31 counts.

When a new fan drive setting is entered, the delta from the next fan drive setting and the previous fan drive setting is determined. If this delta is greater than the Max Step settings, then the fan drive setting is incrementally adjusted every 100ms to 1.6s as determined by the Update Time until the target fan drive setting is reached. See Figure 4.3.

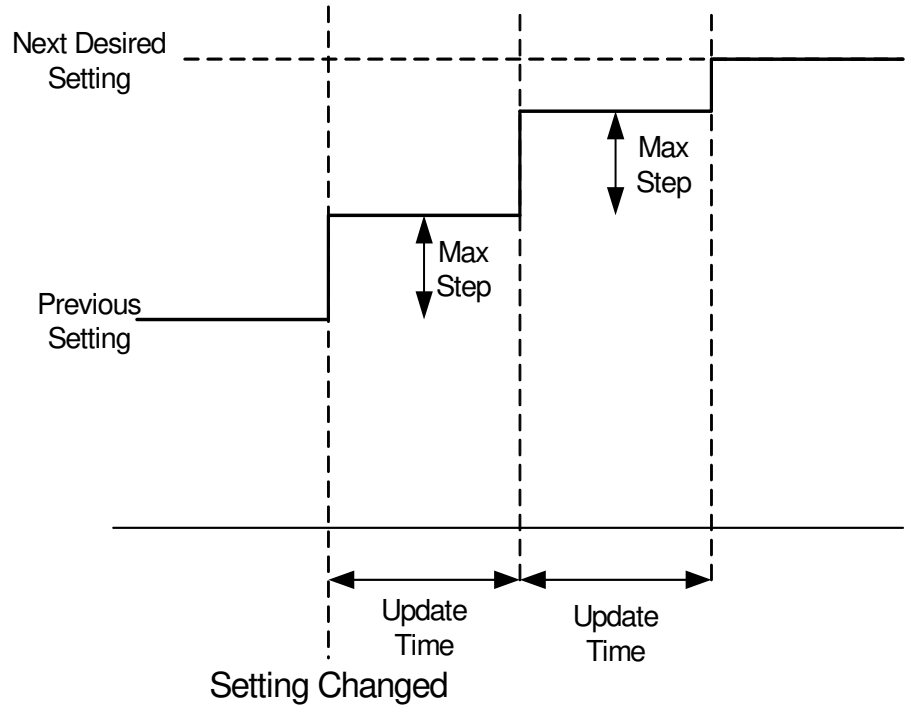


**Figure 4.3 Ramp Rate Control**

## 4.8 Watchdog Timer

The EMC2302 contains an internal Watchdog Timer for all fan drivers. The Watchdog timer monitors the SMBus traffic for signs of activity and works in two different modes based upon device operation. These modes are Power Up Operation and Continuous Operation as described below.

For either mode of operation, if four (4) seconds elapse without activity detected by the host, then the watchdog will be triggered and the following will occur:

1. The WATCH status bit will be set.
2. The fan driver will be set to full scale drive. It will remain at full scale drive until it is disabled.
3. The ALERT# pin is asserted.

**APPLICATION NOTE:** When the Watchdog timer is activated, the Fan Speed Control Algorithm is automatically disabled. Disabling the Watchdog will not automatically set the fan drive nor re-activate the Fan Speed Control Algorithm. This must be done manually.

### 4.8.1 Power Up Operation

The Watchdog Timer only starts immediately after power-up. Once it has been triggered or deactivated, it will not restart although it can be configured to operate in Continuous operation. While the Watchdog timer is active, the device will not check for a Stalled Fan condition.

In the Power Up Operation, the Watchdog Timer is disabled by any of the following actions:

1. Writing the Fan Setting Register will disable the Watchdog Timer.
2. Enabling the RPM-based Fan Speed Control Algorithm by setting the EN_ALGO bit will disable the Watchdog Timer. The fan driver will be set based on the RPM-based Fan Speed Control Algorithm.

Writing any other configuration registers will not disable the Watchdog Timer upon power up.

### 4.8.2 Continuous Operation

When configured to operate in Continuous Operation, the Watchdog timer will start immediately. The timer will be reset by any access (read or write) to the SMBus register set. The four second Watchdog timer will restart upon completion of SMBus activity.

# Chapter 5 Register Set

## 5.1 Register Map

The following registers are accessible through the SMBus Interface. All register bits marked as '-' will always read '0'. A write to these bits will have no effect.

**Table 5.1 EMC2302 Register Set**

| ADDR | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | LOCK | PAGE |
|---|---|---|---|---|---|---|
| Configuration and control | | | | | | |
| 20h | R/W | Configuration | Configures the clocking and watchdog functionality | 40h | SWL | Page 25 |
| 24h | R-C | Fan Status | Stores the status bits for the RPM-based Fan Speed Control Algorithm | 00h | No | Page 26 |
| 25h | R-C | Fan Stall Status | Stores status bits associated with a stalled fan | 00h | No | Page 26 |
| 26h | R-C | Fan Spin Status | Stores status bits associated with a spin-up failure | 00h | No | Page 26 |
| 27h | R-C | Drive Fail Status | Stores status bits associated with drive failure | 00h | No | Page 26 |
| 29h | R/W | Fan Interrupt Enable Register | Controls the masking of interrupts on all fan related channels | 00h | No | Page 27 |
| 2Ah | R/W | PWM Polarity Config | Configures Polarity of all PWM drivers | 00h | No | Page 28 |
| 2Bh | R/W | PWM Output Config | Configures Output type of PWM drivers | 00h | No | Page 28 |
| 2Dh | R/W | PWM Base Frequency | Selects the base frequency for PWM output 2 | 00h | No | Page 28 |
| Fan 1 Control Registers | | | | | | |
| 30h | R/W | Fan 1 Setting | Always displays the most recent fan driver input setting for Fan 1. If the RPM-based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver. | 00h | No | Page 29 |
| 31h | R/W | PWM 1 Divide | Stores the divide ratio to set the frequency for Fan 1 | 01h | No | Page 30 |
| 32h | R/W | Fan 1 Configuration 1 | Sets configuration values for the RPM-based Fan Speed Control Algorithm for the Fan 1 driver | 2Bh | No | Page 30 |
| 33h | R/W | Fan 1 Configuration 2 | Sets additional configuration values for the Fan 1 driver | 28h | SWL | Page 32 |

**Table 5.1 EMC2302 Register Set (continued)**

| ADDR | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | LOCK | PAGE |
|---|---|---|---|---|---|---|
| 35h | R/W | Gain 1 | Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for the Fan 1 driver | 2Ah | SWL | Page 33 |
| 36h | R/W | Fan 1 Spin Up Configuration | Sets the configuration values for Spin Up Routine of the Fan 1 driver | 19h | SWL | Page 34 |
| 37h | R/W | Fan 1 Max Step | Sets the maximum change per update for the Fan 1 driver | 10h | SWL | Page 35 |
| 38h | R/W | Fan 1 Minimum Drive | Sets the minimum drive value for the Fan 1 driver | 66h (40%) | SWL | Page 36 |
| 39h | R/W | Fan 1 Valid TACH Count | Holds the tachometer reading that indicates Fan 1 is spinning properly | F5h | SWL | Page 36 |
| 3Ah | R/W | Fan 1 Drive Fail Band Low Byte | Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive | 00h | SWL | Page 37 |
| 3Bh | R/W | Fan 1 Drive Fail Band High Byte | | 00h | SWL | |
| 3Ch | R/W | TACH 1 Target Low Byte | Holds the target tachometer reading low byte for Fan 1 | F8h | No | Page 37 |
| 3Dh | R/W | TACH 1 Target High Byte | Holds the target tachometer reading high byte for Fan 1 | FFh | No | Page 37 |
| 3Eh | R | TACH 1 Reading High Byte | Holds the tachometer reading high byte for Fan 1 | FFh | No | Page 38 |
| 3Fh | R | TACH 1 Reading Low Byte | Holds the tachometer reading low byte for Fan 1 | F8h | No | Page 38 |
| Fan 2 Control Registers | | | | | | |
| 40h | R/W | Fan 2 Setting | Always displays the most recent fan driver input setting for Fan 2. If the RPM-based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver. | 00h | No | Page 29 |
| 41h | R/W | PWM 2 Divide | Stores the divide ratio to set the frequency for Fan 2 | 01h | No | Page 30 |
| 42h | R/W | Fan 2 Configuration1 | Sets configuration values for the RPM-based Fan Speed Control Algorithm for Fan 2 | 2Bh | No | Page 30 |
| 43h | R/W | Fan 2 Configuration 2 | Sets additional configuration values for the Fan 2 driver | 28h | SWL | Page 32 |
| 45h | R/W | Gain 2 | Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for Fan 2 | 2Ah | SWL | Page 33 |
| 46h | R/W | Fan 2 Spin Up Configuration | Sets the configuration values for Spin Up Routine of the Fan 2 driver | 19h | SWL | Page 34 |
| 47h | R/W | Fan 2 Max Step | Sets the maximum change per update for Fan 2 | 10h | SWL | Page 35 |

**Table 5.1 EMC2302 Register Set (continued)**

| ADDR | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | LOCK | PAGE |
|---|---|---|---|---|---|---|
| 48h | R/W | Fan 2 Minimum Drive | Sets the minimum drive value for the Fan 2 driver | 66h (40%) | SWL | Page 36 |
| 49h | R/W | Fan 2 Valid TACH Count | Holds the tachometer reading that indicates Fan 2 is spinning properly | F5h | SWL | Page 36 |
| 4Ah | R/W | Fan 2 Drive Fail Band Low Byte | Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive | 00h | SWL | Page 37 |
| 4Bh | R/W | Fan 2 Drive Fail Band High Byte | | 00h | SWL | |
| 4Ch | R/W | TACH 2 Target Low Byte | Holds the target tachometer setting low byte for Fan 2 | F8h | No | Page 37 |
| 4Dh | R/W | TACH 2 Target High Byte | Holds the target tachometer setting high byte for Fan 2 | FFh | No | Page 37 |
| 4Eh | R | TACH 2 Reading High Byte | Holds the tachometer reading high byte for Fan 2 | FFh | No | Page 38 |
| 4Fh | R | TACH 2 Reading Low Byte | Holds the tachometer reading low byte for Fan 2 | F8h | No | Page 38 |
| Lock Register | | | | | | |
| EF | R/W | Software Lock | Locks all SWL registers | 00h | SWL | Page 39 |
| Revision Registers | | | | | | |
| FDh | R | Product ID | Stores the unique Product ID | 36h | No | Page 39 |
| FEh | R | Manufacturer ID | Stores the Manufacturer ID | 5Dh | No | Page 40 |
| FFh | R | Revision | Revision | 80h | No | Page 40 |

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

### 5.1.1 Lock Entries

The Lock Column describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set.

## 5.2 Configuration Register

**Table 5.2 Configuration Register**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20h | R/W | Configuration | MASK | DIS_TO | WD_EN | - | - | - | DR_EXT_CLK | USE_EXT_CLK | 40h |