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EMC6D103

Fan Control Device with High Frequency PWM Support and Hardware Monitoring Features

PRODUCT FEATURES

Datasheet

- 3.3 Volt Operation (5 Volt Tolerant Input Buffers)
- SMBus 2.0 Compliant Interface (Fixed, not Discoverable) with Three Slave Address Options
- Fan Control
  - PWM (Pulse width Modulation) Outputs (3)
  - Fan Tachometer Inputs (4)
  - Programmable automatic fan control based on temperature
  - Backwards compatible with fans requiring lower frequency PWM drive
  - High frequency fan support for 4 wire fans
  - One fan can be controlled from as many as 3 temperature zones
  - Fan ramp rate control for acoustic noise reduction
- Power Savings Modes
  - Two monitoring modes: continuous or cycling (for power savings)
  - Two low power modes when monitoring if off: Sleep and Shutdown
- Temperature Monitor
  - Monitoring of Two Remote Thermal Diodes (+/- 3 deg C accuracy)
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Temperature Indication
  - Configurable offset for internal or external temperature channels.
- Voltage Monitor
  - Monitor Power supplies (+2.5V, +5V, +12V, Vccp, and VCC)
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Voltage Indication
- 5 VID (Voltage Identification) Inputs
- XOR Tree Test Mode
- 24-Pin, SSOP Lead-Free RoHS Compliant Packages

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Chapter 1 General Description

The EMC6D103 is an environmental monitoring device with automatic fan control capability. This ACPI compliant device provides hardware monitoring for up to five voltages and three thermal zones, measures the speed of up to four fans, and controls the speed of multiple DC fans using Pulse Width Modulator (PWM) outputs. High frequency and low frequency PWMs are supported.

The EMC6D103 hardware monitor provides analog inputs for monitoring external voltages of +2.5V, +5V, +12V and Vccp. This device has the capability to monitor its own internal VCC power supply, which may be connected to either main power (VCC) or the suspend power well (VTR). In addition to monitoring the processor voltage, VID inputs are available to identify the voltage specification. External components are not required for voltage scaling or similar treatment.

The EMC6D103 hardware monitor includes support for monitoring three thermal zones: two external and one internal. The external temperatures are measured via thermal diode inputs capable of monitoring remote devices. In addition, they are equipped with an ambient temperature sensor for measuring the internal temperature.

Pulse Width Modulators (PWM) control the speed of the fans by varying the output duty cycle of the PWM. Each PWM can be associated with any or all of the thermal zones monitored. As the temperature of the associated zone varies, the PWM duty cycle is adjusted accordingly. The Ramp Rate Control feature controls the rate of change of the PWM output, thereby reducing system noise created by changing the fan speed. The speed of each fan is monitored by a Fan Tachometer input. The measured values are compared to values stored in Limit Registers to detect if a fan has stalled or seized.

Fan speed may be under host software control or automatic. In host control mode, the host software continuously monitors temperature and fan speed registers, makes decisions as to desired fan speed and sets the PWM's to drive the required fan speed. This device offers an interrupt output signal (INT#), which may be used to interrupt the host on out-of-limit temperature or voltage condition enabling an ACPI response as opposed to the host software continuously monitoring status. In auto "zone" mode, the logic continuously monitors the temperature and fan speeds and adjusts speeds without intervention from the host CPU. Fan speed is adjusted according to an algorithm using the temperature measured in the selected zone, the high and low limits set by the user, and the current fan speed.

The EMC6D103 supports two Monitoring modes: Continuous Mode and Cycle Mode. In the continuous monitoring mode, the sampling and conversion process is performed continuously for each voltage and temperature reading after monitoring is enabled. The time for each voltage and temperature reading varies depending on the measurement option. In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.2 seconds (1.4 sec max - default averaging enabled). The sampling and conversion of each voltage and temperature reading is performed once every monitoring cycle. (This is a power saving mode.)

The EMC6D103 can be placed in one of two low-power modes: Sleep mode or Shutdown mode. These modes do not reset any of the registers of the device. In Sleep mode bias currents are on and the internal oscillator is on, but the the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode. In Shutdown mode the bias currents are off, the internal oscillator is off, and the the A/D converter and monitoring cycle are turned off. Serial communication is only possible with a select register.

Chapter 2 Pinout

This Environmental Monitoring and Control device (EMC) is offered in a 24 pin SSOP mechanical package.

2.1 EMC6D103 Pinout

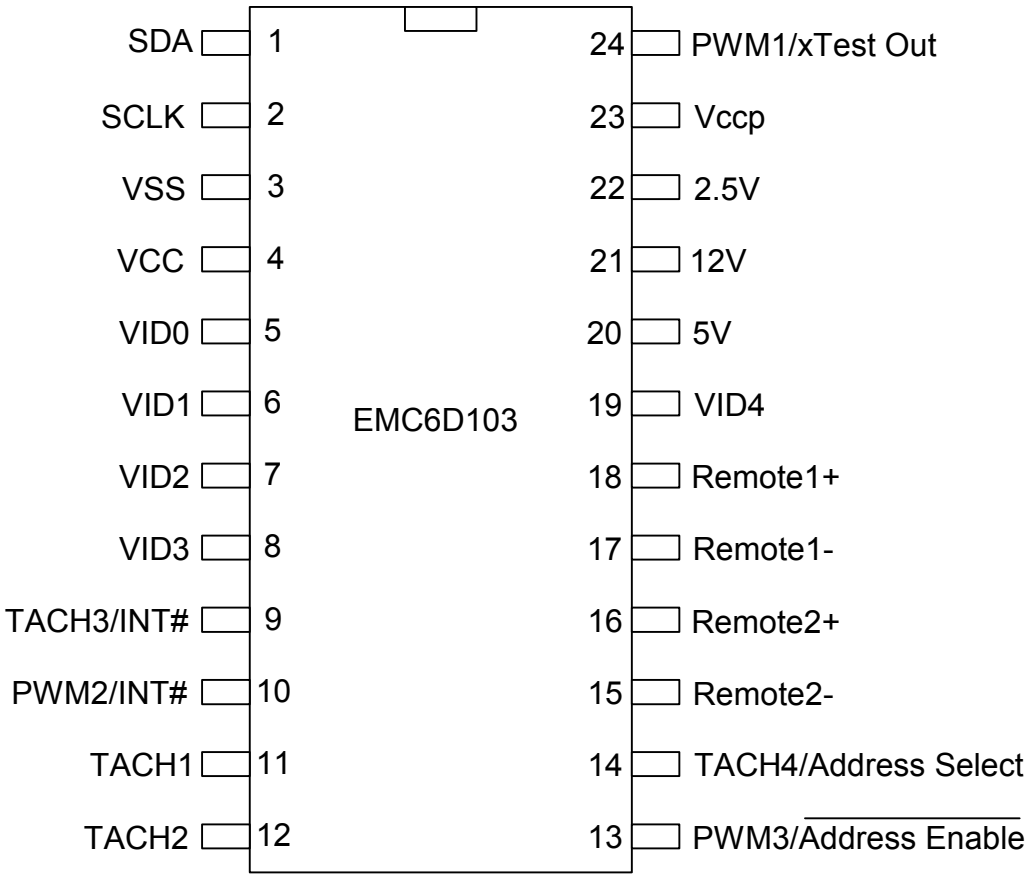

Figure 2.1 EMC6D103 24 Pin SSOP Pinout

Chapter 3 Pin Description

3.1 Pin Functions

Table 3.1 Pin Description

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER REQUIREMENT PER FUNCTION (Note 3.1)	POWER WELL	NOTES
HARDWARE MONITORING BLOCK (24)						
1	SDA	System Management Bus bi-directional Data. Open Drain output.	I_MOD3	I_MOD3	VCC	
2	SCLK	System Management Bus Clock.	I_M	I_M	VCC	
5	VID0	Voltage ID 0 Input	I_M	I_M	VCC	
6	VID1	Voltage ID 1 Input	I_M	I_M	VCC	
7	VID2	Voltage ID 2 Input	I_M	I_M	VCC	
8	VID3	Voltage ID 3 Input	I_M	I_M	VCC	
19	VID4	Voltage ID 4 Input	I_M	I_M	VCC	
17	Remote1-	This is the negative Analog input (current sink) from the remote thermal diode. This serves as the negative input into the A/D. Digital Input.	I_{AN}	I_{AN}	VCC	
18	Remote1+	This is the positive input (current source) from the remote thermal diode. This serves as the positive input into the A/D.	I_{AN}	I_{AN}	VCC	
15	Remote2-	This is the negative Analog input (current sink) from the remote thermal diode. This serves as the negative input into the A/D. Digital Input.	I_{AN}	I_{AN}	VCC	
16	Remote2+	This is the positive input (current source) from the remote thermal diode. This serves as the positive input into the A/D.	I_{AN}	I_{AN}	VCC	
20	+5V_IN	Analog input for +5V	I_{AN}	I_{AN}	VCC	Note 3.2
22	+2.5V_IN	Analog input for +2.5V	I_{AN}	I_{AN}	VCC	Note 3.2
23	Vccp	Analog input for +Vccp (processor voltage: 0 to 3.0V).	I_{AN}	I_{AN}	VCC	Note 3.2
21	12V_IN	Analog input for +12V	I_{AN}	I_{AN}	VCC	Note 3.2

Table 3.1 Pin Description (continued)

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER REQUIREMENT PER FUNCTION (Note 3.1)	POWER WELL	NOTES
HARDWARE MONITORING BLOCK (24)						
11	TACH1	Input for monitoring a fan tachometer input.	I_M	I_M	VCC	
12	TACH2	Input for monitoring a fan tachometer input.	I_M	I_M	VCC	
9	TACH3 /INT#	Input for monitoring a fan tachometer input. /Interrupt output to indicate a thermal and/or voltage event.	I_MOD3	I_M /OD3	VCC	
14	TACH4 /Address Select	Input for monitoring a fan tachometer input. If in Address Select Mode, determines the SMBus address of the device.	I_M	I_M	VCC	
24	PWM1 /xTest Out	PWM Output 1 controlling speed of fan. When in XOR tree test mode, functions as XOR Tree output.	O8	OD8/O8	VCC	
10	PWM2 /INT#	PWM Output 2 controlling speed of fan. /Interrupt output to indicate a thermal and/or voltage event.	OD8	OD8/OD8	VCC	
13	PWM3 /Address Enable#	PWM Output 3 controlling speed of fan. If pulled to ground at power on, enables Address Select Mode (Address Select pin controls SMBus address of the device).	IOD8	OD8/I	VCC	
4	VCC	Positive Power Supply. Nominal 3.3V. VCC is monitored by the Hardware Monitoring Block. (Can be powered by +3.3V Standby power if monitoring in low power states is required.)				
3	VSS	Analog Ground.				

Note: The “#” as the suffix of a signal name indicates an “Active Low” signal.

Note 3.1 Buffer types per function on multiplexed pins are separated by a slash “/”. Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 3.2 This analog input is backdrive protected.

3.2 Buffer Type Description

Note: The buffer type values are specified at VCC=3.3V

Table 3.2 Buffer Type Descriptions

BUFFER TYPE	DESCRIPTION
I_M	Digital Input
I_{AN}	Analog Input, Hardware Monitoring Block.
I_MOD3	Input/Output (Open Drain), 3mA sink.
O8	Output, 8mA sink, 4mA source.
OD8	Output (Open Drain), 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.

3.3 3.3V Operation, 5V Tolerance

The EMC6D103 is intended to operate with a nominal 3.3V power supply. The analog voltage pins are connected to voltage sources at their respective nominal levels. All digital signal pins are 3V switching, but are tolerant to 5V.

Chapter 4 Operational Description

4.1 Maximum Guaranteed Ratings

Operating Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range . . . . . -55° to +150°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

Maximum V_{cc} 5.0V

Positive Voltage on any pin (except for analog inputs), with respect to Ground 5.5V

Negative Voltage on any pin (except for analog inputs), with respect to Ground . . . . . -0.3V

Positive Voltage on voltage analog inputs:

- Vccp_in 4.5V
- 2.5V_in 5.0V
- +5V_in 8.0V
- 12V_in 17V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

4.2 Ratings for Operation

TA = 0°C - 70°C, VCC=+3.3V±10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Temperature-to-Digital Converter Characteristics						
Internal Temperature Accuracy		-3 -2	±0.25	+3 +2	°C °C °C	0°C <= T_A <= 70°C 40°C <= T_A <= 70°C Resolution
External Diode Sensor Accuracy		-5 -3	±0.25	+5 +3	°C °C °C	-40°C <= T_S <= 125°C 40°C <= T_S <= 100°C Resolution

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Analog-to-Digital Converter Characteristics						
Total Unadjusted Error	TUE			±2	%	Note 4.1
Differential Non-Linearity	DNL		±1		LSB	
Power Supply Sensitivity	PSS		±1		%/V	
Total Monitoring Cycle Time (Cycle Mode, Default Averaging)	$t_{C(Cycle)}$		1.22	1.4	sec	Note 4.2
Conversion Time (Continuous Mode, Default Averaging)	$t_{C(Cts)}$	203	223	248	msec	Note 4.3
Input Resistance			140	200	kΩ	
ADC Resolution						10 bits Note 4.6
Input Buffer (VID0-VID4,TACH1-TACH4)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
IOD Type Buffer (SCL, SDA, PWM1, PWM2, PWM3/ADDRESS ENABLE, INT#						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
Hysteresis	V_{HYS}		500		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = +4.0 mA (Note 4.5)
Leakage Current (ALL - Digital)						(Note 4.4)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Digital Input Capacitance	C_{IN}			10	pF	
V_{CC} Supply Current						All outputs open, all inputs transitioning from/to 0V to/from 3.3V.
Active Mode	I_{CC}			3	mA	
Sleep Mode	I_{CC}			2	mA	
Shutdown Mode	I_{CC}			100	µA	

Notes:

- Voltages are measured from the local ground potential, unless otherwise specified.
- Typical values are at TA=25°C and represent most likely parametric norm.

- Timing specifications are tested at the TTL logic levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 4.1 TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

Note 4.2 Total Monitoring Cycle Time for cycle mode includes a one second delay plus all temperature conversions and all analog input voltage conversions.

Note 4.3 See Table 6.2, "Conversion Cycle Timing," on page 23 for conversion cycle timing for all averaging options. Only the nominal default case is shown in this section.

Note 4.4 All leakage currents are measured with all pins in high impedance.

Note 4.5 The low output level for PWM pins is actually +8.0mA.

Note 4.6 The h/w monitor analog block implements a 10-bit ADC. The output of this ADC goes to an averager block, which can be configured to accumulate the averaged value of the analog inputs. The amount of averaging is programmable. The output of the averaging block produces a 12-bit temperature or voltage reading value. The 8 MSbits go to the reading register and the 4 LSbits to the A/D LSb register.

Chapter 5 SMBus Interface

The host processor communicates with the Fan Monitoring device through a series of read/write registers via the SMBus interface. SMBus is a serial communication protocol between a computer host and its peripheral devices.

5.1 Slave Address

The default Slave Address is 0101110b. If this address is desired, the designer should not ground the Address Enable# pin and should not apply a strapping resistor to the Address Select pin.

If multiple devices are implemented in a system or another SMBus device requires address 0101110b, TACH4 and PWM3 must be disabled. In this case, addressing is implemented as follows:

The board designer will apply a 10KΩ pull-down resistor to ground on the Address Enable# pin. Upon power up, the EMC6D103 device will be placed into Address Enable mode and assign itself an SMBus address according to the Address Select input. The device will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the EMC6D103 address. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection.

Table 5.1 SMBus Slave Address Options

ADDRESS ENABLE#	ADDRESS SELECT	BOARD IMPLEMENTATION	SMBUS ADDRESS [7:1]
1	X	Address Enable# pulled to VCC through resistor **Note:** Resistor value will be dependent on PWM circuit implemented.	0101 110b (default)
0	0	Address Enable# pulled to ground through 10kΩ resistor Address Select Pulled to ground through a 10kΩ resistor	0101 100b
0	1	Address Enable# pulled to ground through 10kΩ resistor Address Select pulled to VCC through a 10kΩ resistor	0101 101b

In this way, there can be up to three EMC6D103 devices on the SMBus at any time. Multiple EMC6D103 devices can be used to monitor additional processors and temperature zones.

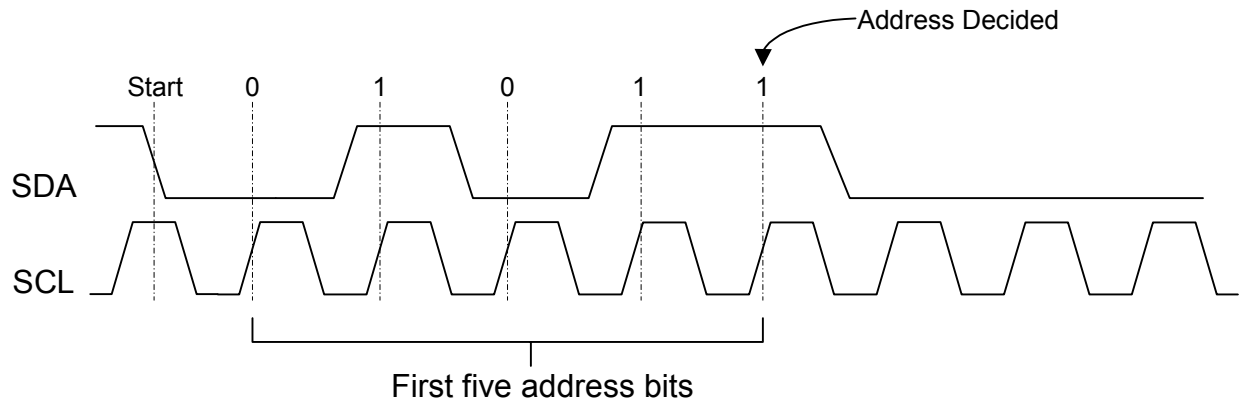

Figure 5.1 Address Selection on EMC6D103

5.2 Slave Bus Interface

The EMC6D103 device SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports Write Byte and Read Byte protocols.

The Write Byte and Read Byte protocols are valid SMBus protocols for the device. This part responds to other protocols as described in the Invalid Protocol Section. Reference the System Management Bus Specification, Rev 2.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in section 11 Register Set on page 31.

5.3 Bus Protocols

Typical Write Byte and Read Byte protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the Hardware Monitor Block driving data on the SDA line; otherwise, host data is on the SDA line.

The slave address is the unique SMBus Interface Address for the Hardware Monitor Block that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

Byte Protocols

A write byte transfer will always consist of the SMBus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. The normal read protocol consists of a write to the Hardware Monitor Block with the SMBus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the SMBus Interface Address byte, followed by the data byte read from the Hardware Monitor Block. This can be accomplished by using the Read Byte protocol or by using the Send Byte protocol followed by the Receive Byte protocol.
2. If the Internal Address Register is known to be at the desired Address, simply read the Hardware Monitor Block with the SMBus Interface Address byte, followed by the data byte read from the Hardware Monitor Block. This corresponds to the Receive Byte protocol.

Write Byte

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in Table 5.2 is performed correctly. Only one byte is transferred at time for a Write Byte protocol.

Table 5.2 SMBus Write Byte Protocol

FIELD	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	REG. DATA	ACK	STOP
Bits	1	7	1	1	8	1	8	1	1

Read Byte

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in Table 5.3 is performed correctly. Only one byte is transferred at time for a Read Byte protocol.

Table 5.3 SMBus Read Byte Protocol

FIELD:	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	START	SLAVE ADDR	RD	ACK	REG. DATA	NACK	STOP
Bits:	1	7	1	1	8	1	1	7	1	1	8	1	1

5.4 Invalid Protocol Response Behavior

Registers that are accessed with an invalid protocol will not be updated. A register will only be updated following a valid protocol. The only valid protocols are the Write Byte, Read Byte, Send Byte, and Receive Byte protocols, which are described above.

The EMC6D103 device responds to three SMBus slave addresses:

1. The SMBus slave address that supports the valid protocols defined in the previous sections is determined by the level on the Address Select and Address Enable pins as shown in Section 5.1, "Slave Address," on page 17.
2. SMBus Alert Response (0001 100). The SMBus will only respond to the SMBus Alert Response Address if the SMBus Alert Response interrupt was generated to request a response from the Host. The SMBus Alert Response is defined in Section 5.10, "SMBus Alert Response Address," on page 20.

Attempting to communicate with the Hardware Monitor Block over SMBus with an invalid slave address, or invalid protocol will result in no response, and the SMBus Slave Interface will return to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. See Section 5.4.1, "Undefined Registers" for response to undefined registers.

5.4.1 Undefined Registers

Reads to undefined registers return 00h. Writes to undefined registers have no effect and return no error.

5.5 General Call Address Response

The EMC6D103 will not respond to a general call address of 0000_000.

5.6 Slave Device Time-Out

The EMC6D103 supports the slave device timeout as per the SMBus Specification, v2.0.

According to SMBus specification, v2.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35ms ($T_{TIMEOUT, MAX}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition

5.7 Stretching the SCLK Signal

The EMC6D103 supports stretching of the SCLK by other devices on the SMBus. The Hardware Monitor Block does not stretch the SCLK.

5.8 SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing diagram shown in the section titled Section 9.2, "SMBus Interface," on page 87.

5.9 Bus Reset Sequence

The SMBus Slave Interface will reset and return to the idle state upon a START field followed immediately by a STOP field.

5.10 SMBus Alert Response Address

The EMC6D103 device responds to the SMBus Alert Response Address, 0001 100, if the INTEN bit (register 7Ch bit 2) is set and one or more status events bits are high. The interrupt signal (INT#), which can be enabled on either the PWM2 or TACH3 pins, can be used as the SMBALERT#. See the section describing the Interrupt Status Registers on page 25 and the section describing the Interrupt Pin on page 27 for more details on interrupts.

The device can signal the host that it wants to talk by pulling the SMBALERT# low, if a status bit is set in one of the interrupt status registers and properly enabled onto the INT# pin. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through a modified Receive Byte operation with the Alert Response Address (ARA).

The EMC6D103 device, which pulled SMBALERT# low, will acknowledge the Alert Response Address and respond with its device address. The 7-bit device address provided by the EMC6D103 device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

Table 5.4 Modified SMBus Receive Byte Protocol Response to ARA

FIELD:	START	ALERT RESPONSE ADDRESS	RD	ACK	EMC6D103 SLAVE ADDRESS	NACK	STOP
Bits:	1	7	1	1	8	1	1

After acknowledging the slave address, the EMC6D103 device will disengage the SMBALERT# pull-down by clearing the INT enable bit. If the condition that caused the interrupt remains, the Fan Control device will reassert the SMBALERT# on the next monitoring cycle, provided the INT enable bit has been set back to ‘1’ by software.

Note: The INT# signal is an alternate function on the PWM2 and TACH3 pins. The EMC6D103 device will respond to the SMBus Alert Response address even if the INT# signal is not selected as the alternate function on one of these pins as long as the following conditions exist: the INTEN bit (register 7Ch bit 2) is set, an individual status bit is set in one of the interrupt status registers, and the corresponding group enable bit is set. Each interrupt event must be enabled into the interrupt status registers, and the status bits must be enabled onto the INT# signal via the group enable bits for each type of event (i.e., temperature, voltage and fan). See the section titled Interrupt Status Registers on page 25.

Chapter 6 Hardware Monitoring

The following sub-sections describe the EMC6D103 Hardware Monitoring features.

6.1 Input Monitoring

The EMC6D103 device's monitoring function is started by writing a '1' to the START bit in the **Ready/Lock/Start** Register (0x40). Measured values from the analog inputs and temperature sensors are stored in Reading Registers. The values in the reading registers can be accessed via the SMBus interface. These values are compared to the programmed limits in the Limit Register. The out-of-limit and diode fault conditions are stored in the Interrupt Status Registers.

6.2 Resetting the EMC6D103

6.2.1 Power-On Reset

All the registers in the Hardware Monitor Block, except the reading registers, reset to a default value when power is applied to the block. The default state of the register is shown in the table in the Register Summary subsection. The default state of Reading Registers are not shown because these registers have indeterminate power on values.

Note: Usually the first action after power up is to write limits into the Limit Registers.

6.2.2 Soft Reset (Initialization)

Setting bit 7 of the CONF register performs a soft reset. This bit is self-clearing. Soft Reset performs reset on all the registers except the Reading Registers.

6.3 Monitoring Modes

The Hardware Monitor Block supports two Monitoring modes: Continuous Mode and Cycle Mode. These modes are selected using bit 1 of the Special Function Register (7Ch). The following subsections contain a description of these monitoring modes.

The hardware monitor conversion clock is 45KHz ± 10%. Temperature conversions take 96 clocks, each (2.133ms nom.); voltage conversions take 68 clocks, each (1.511ms nom). The time to complete a conversion cycle depends upon the number of inputs in the conversion sequence to be measured (see Table 6.3, "ADC Conversion Sequence," on page 24) and the amount of averaging per input, which is selected using the AVG[2:0] bits in the Special Function register (see Register 7Ch: Special Function Register on page 76).

For each mode, there are four options for the number of measurements that are averaged for each temperature and voltage reading. These options are selected using bits[7:5] of the Special Function register (7Ch). These bits are defined as follows:

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated (Table 6.1). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

Table 6.1 AVG[2:0] Bit Decoder

SFTR[7:5]			MEASUREMENTS PER READING			
AVG2	AVG1	AVG0	REMOTE DIODE 1	REMOTE DIODE 2	INTERNAL DIODE	ALL VOLTAGE READINGS (+2.5V, +5V, +12V, VCCP, AND VCC)
0	0	0	128	128	8	8
0	0	1	16	16	1	1
0	1	X	16	16	16	16
1	X	X	32	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

To calculate conversion cycle timing for a given averaging mode:

- Compute total number of temperature conversions (TEMP_CONV)
- Compute total number of voltage conversions (VOLT_CONV)
- Calculate Time to complete all conversions is:

Total Conversion Time = (TEMP_CONV)*96/(45kHz +/-10%)+ (VOLT_CONV)*68/(45kHz +/-10%)

Example: To calculate the nominal conversion time FOR AVG[2:0] = 001b.

Total Conversion Time = (TEMP_CONV)*96/(45kHz)+ (VOLT_CONV)*68/(45kHz)

Total Conversion Time = (16+16+1)*96/(45kHz)+ (5*1)*68/(45kHz)

Total Conversion Time = (33)*2.133ms+ (5)*1.511ms = ~78ms

Table 6.2 illustrates the min., nom., and max. conversion cycle timing for each of the four averaging modes.

Table 6.2 Conversion Cycle Timing

AVG[2:0]	TOTAL TEMPERATURE CONVERSIONS	TOTAL VOLTAGE CONVERSIONS	CONVERSION CYCLE TIME (MSEC)		
			MIN.	NOM.	MAX.
000	(2x128)+(1x8)=264	5x8=40	567	624	693
001	(2x16)+(1x1)=33	5x1=5	71	78	87
01X (default)	3x16=48	5x16=80	203	223	248
1XX	3x32=96	5x32=160	406	447	496

Note 6.1 The hardware monitor conversion clock is 45KHz ± 10%.

Note 6.2 Temperature conversions take 96 clocks, each (2.133ms nom.); Voltage conversions take 68 clocks, each (1.511ms nom).

6.3.1 Continuous Monitoring Mode

In the continuous monitoring mode, the sampling and conversion process is performed continuously for each voltage and temperature reading after the Start bit is set high. The time for each voltage and temperature reading is shown above for each measurement option.

The continuous monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown below (see Table 6.3). Sampling of all values occurs in a nominal 223 ms (default - see Table 6.2, “Conversion Cycle Timing,” on page 23).

Table 6.3 ADC Conversion Sequence

SAMPLING ORDER	REGISTER
1	Remote Diode Temp Reading 1
2	Ambient Temperature reading
3	VCC reading
4	+12V reading
5	+5V reading
6	+2.5V reading
7	Vccp (processor) reading
8	Remote Diode Temp Reading 2

When the continuous monitoring function is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 223 ms (default - see Table 6.2, “Conversion Cycle Timing,” on page 23). Each measured value is compared to values stored in the Limit registers. When the measured value violates the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See Auto Fan Control Operating Mode on page 34.

The results of the sampling and conversions can be found in the Reading Registers and are available at any time.

6.3.2 Cycle Monitoring Mode

In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.2 seconds (1.4 sec max - default averaging enabled). The sampling and conversion of each voltage and temperature reading is performed once every monitoring cycle. This is a power saving mode.

The cycle monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown above.

When the cycle monitoring function is started, it cycles through each measurement in sequence, and it produces a converted voltage and temperature reading for each input. The state machine waits approximately one second before repeating this process. Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled Auto Fan Control Operating Mode on page 34.

The results of each sampling and conversion can be found in the Reading Registers and are available at any time, however, they are only updated once per conversion cycle.

6.4 Interrupt Status Registers

The Hardware Monitor Block contains two interrupt status registers: Register 41h: Interrupt Status Register 1 on page 61 and on page 62. These registers are used to reflect the state of all temperature, voltage and fan violation of limit error conditions and diode fault conditions that the Hardware Monitor Block monitors.

When an error occurs during the conversion cycle, its corresponding bit is set in its respective interrupt status register. The bit remains set until the register is read by software, at which time the bit will be cleared to ‘0’ if the associated error event no longer violates the limit conditions or if the diode fault condition no longer exists. Reading the register will not cause a bit to be cleared if the source of the status bit remains active.

These registers are read only – a write to these registers have no effect. These registers default to 0x00 on VCC POR and Initialization.

See the description of the Interrupt Status registers in Chapter 8, "Register Set," on page 49.

Each interrupt status bit has a corresponding bit located in an interrupt enable register, which may be used to enable/disable the individual event from setting the status bit. See the following figure for the status and enable bits used to control the interrupt bits and INT# pin.