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EMIF02-MIC02F3

2-line IPAD™, EMI filter including ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filtering
- Lead-free package
- Very low PCB space consumption: 0.9 mm^2
- Very thin package: 0.60 mm
- High efficiency ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards

- IEC61000-4-2 level 4 on external pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC61000-4-2 level 1 on internal pins:
  - 2 kV (air discharge)
  - 2 kV (contact discharge)

Applications

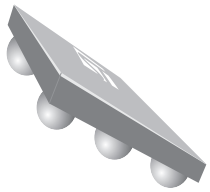
Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

Description

The EMIF02-MIC02F3 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents damage to the protected device when subjected to ESD surges up 15 kV.



Flip Chip
(6 bumps)

Figure 1. Pin layout (bump side)

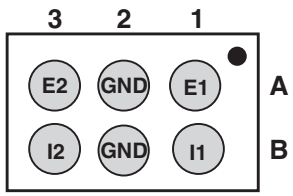
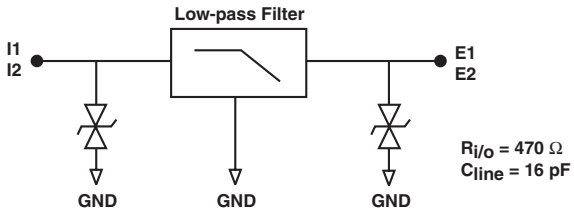


Figure 2. Basic cell configuration



TM: IPAD is a trademark of STMicroelectronics.

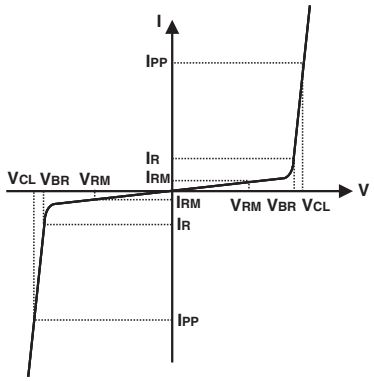
1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V_{PP}	**External pins (A1, A3):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge **Internal pins (B1, B3):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	 15 8 2 2	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	14	16		V
I_{RM}	V_{RM} = 12 V per line			200	nA
$R_{I/O}$	Tolerance ± 10 %		470		Ω
C_{line}	V_{line} = 0V, V_{OSC} = 30 mV, F = 1 MHz, (measured under zero light conditions)		16	20	pF

Figure 3. S21 (dB) attenuation measurement (Line 1)

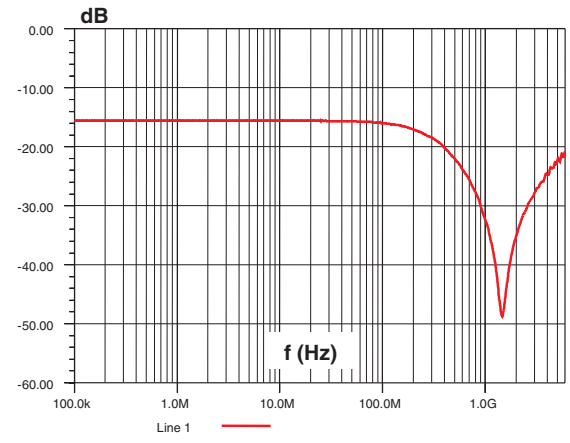


Figure 4. S21 (dB) attenuation measurement (Line 2)

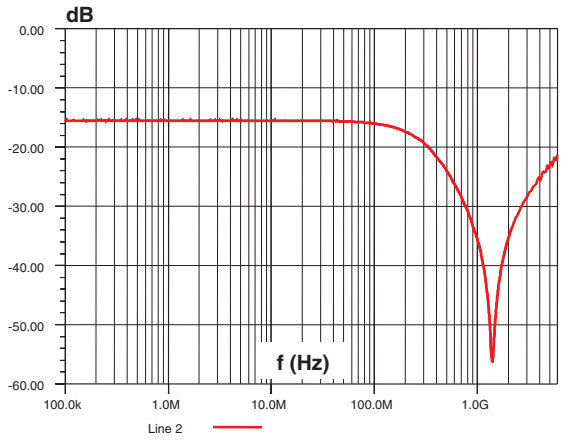


Figure 5. Analog crosstalk measurement

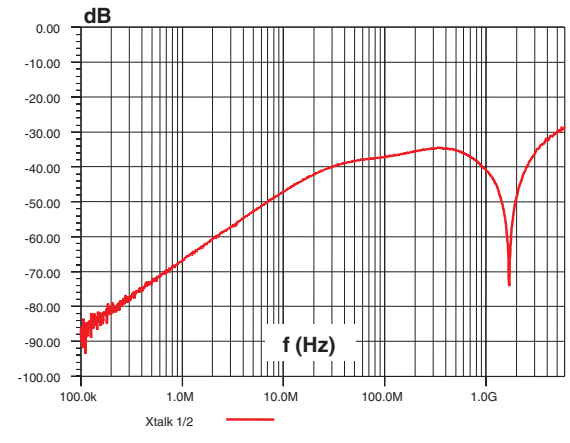


Figure 6. Digital crosstalk measurement

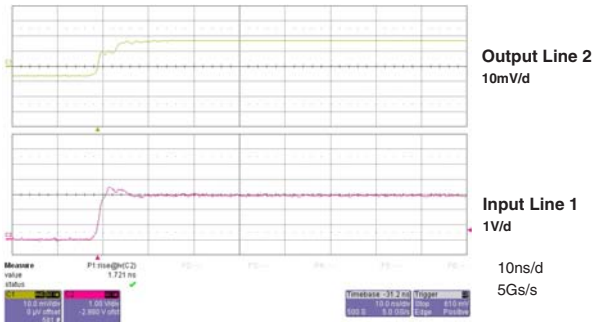


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input and on one output

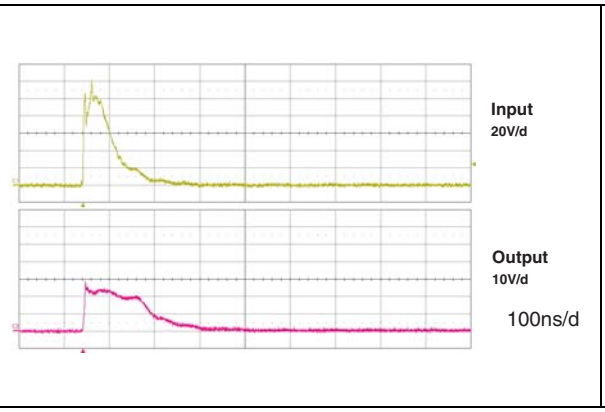


Figure 8. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input and on one output

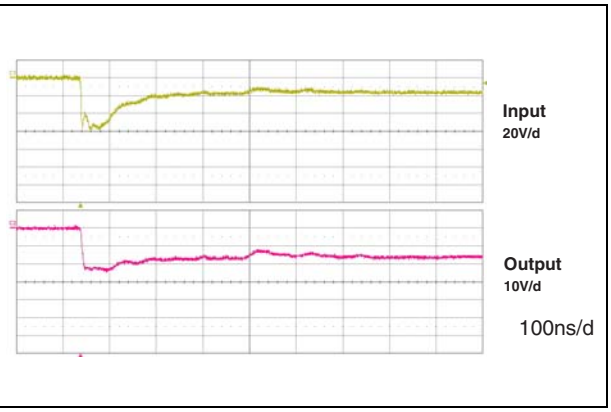
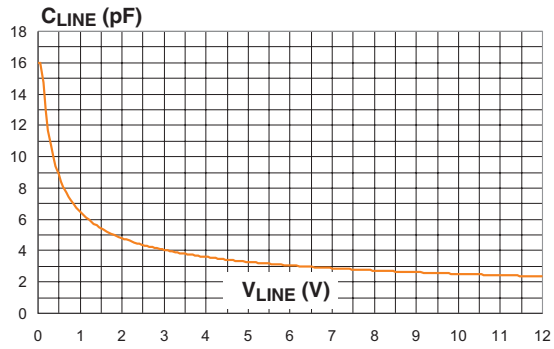


Figure 9. Line capacitance versus applied voltage



2 Application information

Figure 10. Aplac model

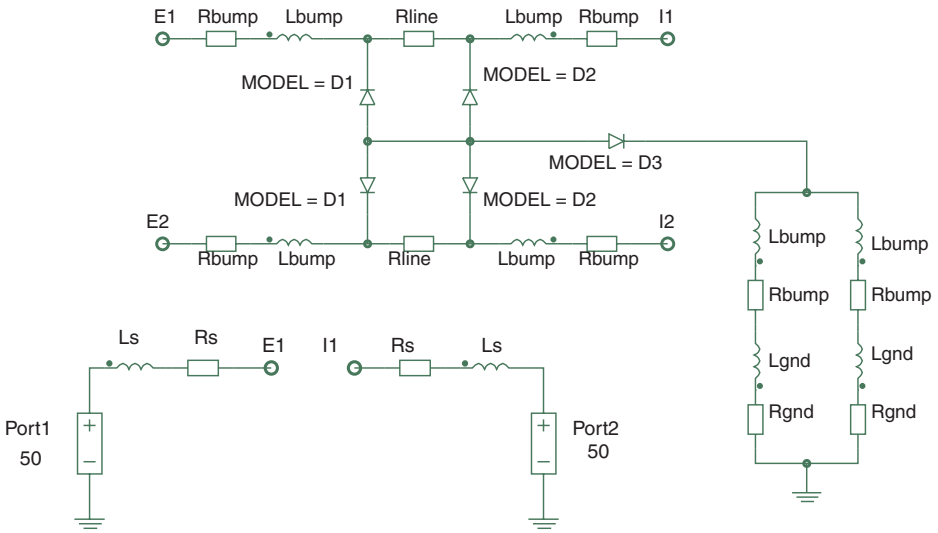
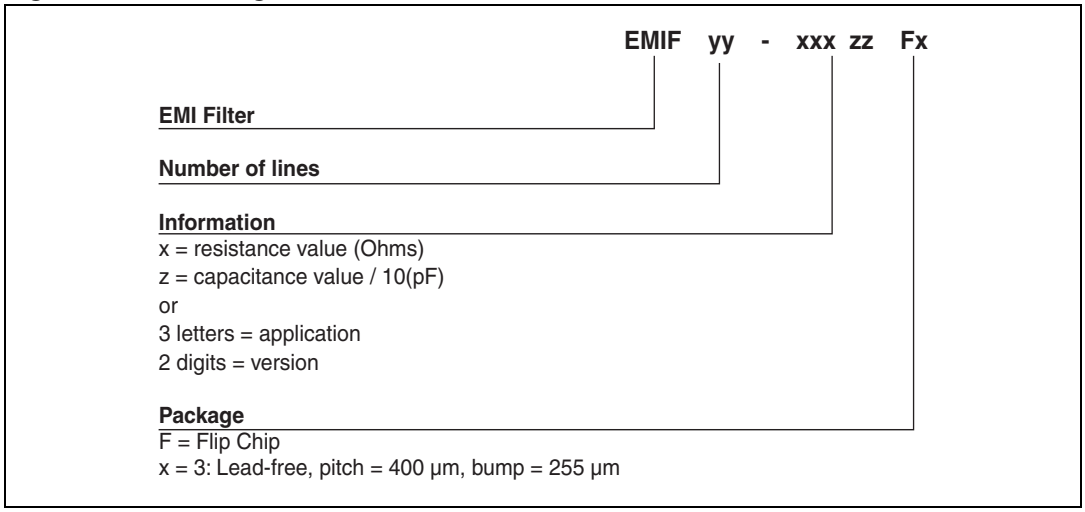


Figure 11. Aplac parameters

Variables	Diode D1	Diode D2	Diode D3
aplacvar Rline 490	BV=7	BV=7	BV=7
aplacvar C_d1 11p	CJO=c_d1	CJO=c_d2	CJO=c_d3
aplacvar C_d2 5p	IBV=1u	IBV=1u	IBV=1u
aplacvar C_d3 240p	IKF=1000	IKF=1000	IKF=1000
aplacvar L 2pH	IS=10f	IS=10f	IS=10f
aplacvar Ls 950pH	ISR=100p	ISR=100p	ISR=100p
aplacvar Rs 150m	N=1	N=1	N=1
aplacvar Lbump 50pH	M=0.3333	M=0.3333	M=0.3333
aplacvar Rbump 20m	RS=0.85	RS=0.85	RS=0.47
aplacvar Lgnd 80pH	VJ=0.6	VJ=0.6	VJ=0.6
aplacvar Rgnd 100m	TT=50n	TT=50n	TT=50n

3 Ordering information scheme

Figure 12. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 13. Package dimensions

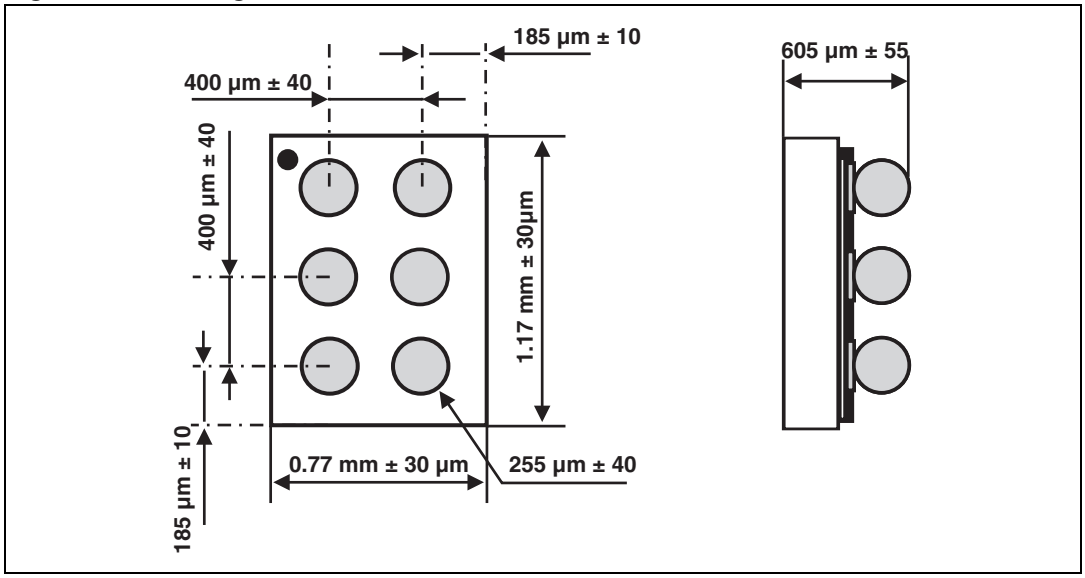


Figure 14. Footprint

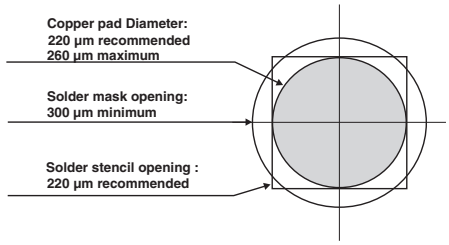


Figure 15. Marking

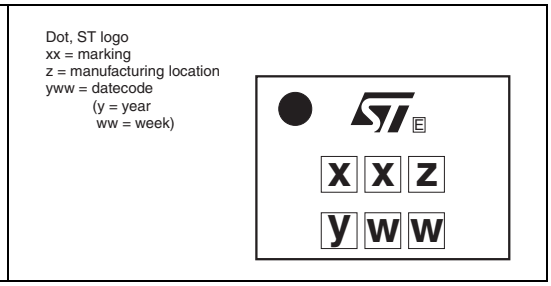
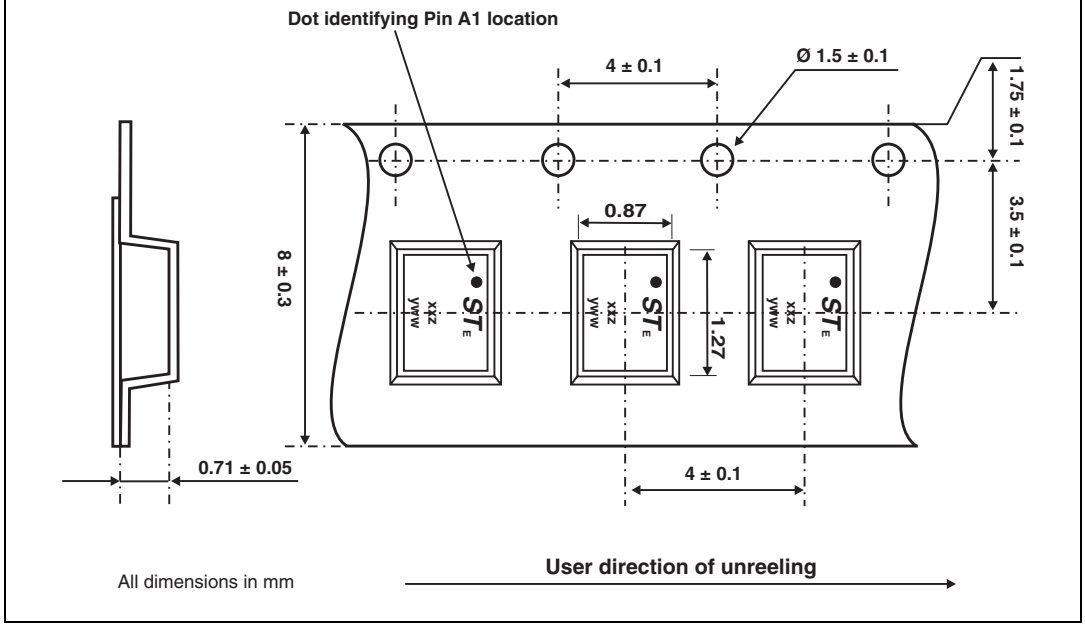


Figure 16. Flip Chip tape and reel specifications



Note: More information is available in the application notes:

AN2348: "STMicroelectronics 400 micro-metre Flip Chip: Package description and recommendation for use"

AN1751: EMI Filters: Recommendations and measurements

5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Base qty	Delivery mode
EMIF02-MIC02F3	HB	Flip Chip	5000	Tape and reel (7")

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
17-Jan-2006	1	Initial release.
28-Apr-2008	2	Updated ECOPACK statement. Updated *Figure 12*, *Figure 13* and *Figure 16.* Reformatted to current standards.

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