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EMIF02-USB01F2

2-line IPAD[™], EMI filter including ESD protection

Features

- 2-line low-pass filter + ESD protection
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space occupation: < 2.5 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards

- IEC 61000-4-2 level 4
 - ±15 kV (air discharge)
 - ±8 kV (contact discharge)

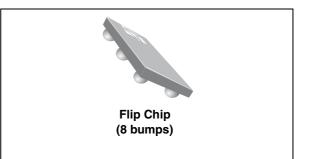
Application

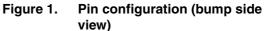
■ ESD protection and EMI filtering for USB port

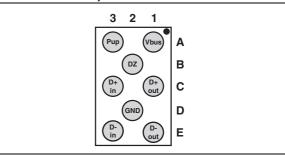
Description

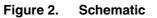
The EMIF02-USB01F2 is a highly integrated array designed to suppress EMI / RFI noise for USB port filtering. The EMIF02-USB01F2 Flip-Chip packaging means the package size is equal to the die size.

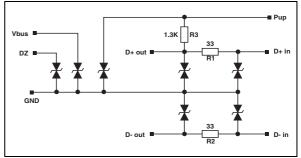
Additionally, this filter includes ESD protection circuitry which prevents damage to the protected device when subjected to ESD surges up to 15 kV.











TM: IPAD is a trademark of STMicroelectronics.

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1 Characteristics

Table 1.	Absolute	ratings	$(T_{amb} = 2)$	25 °C)
	Absolute	runngo		-0 0,

Symbol	Parameter	Value	Unit
Тј	Junction temperature	125	°C
T _{op}	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to 150	°C

Figure 3. Electrical characteristics - definitions

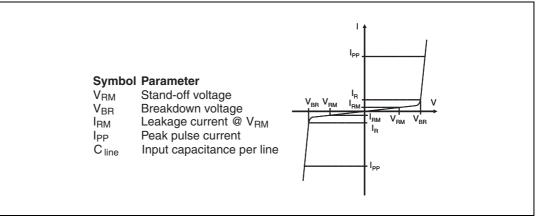


Table 2.	Electrical characteristics - values (T _{amb} = 25 °C)
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Symbol	Test conditions	Min.	Тур.	Max.	Unit
V _{BR}	I _R = 1 mA	6	-	-	V
I _{RM}	V _{RM} = 3 V	-	-	0.5	μA
C _{line}	@ 0 V	-	40	45	pF
R ₁ , R ₂	Tolerance ± 5 %	-	33	-	Ω
R ₃	Tolerance ± 5 %	-	1.30	-	kΩ

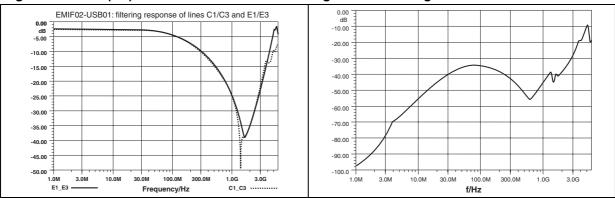
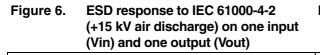
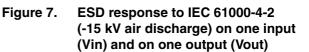
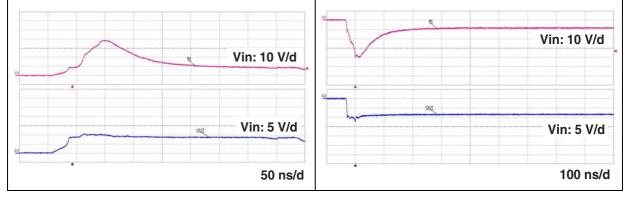
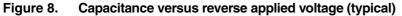


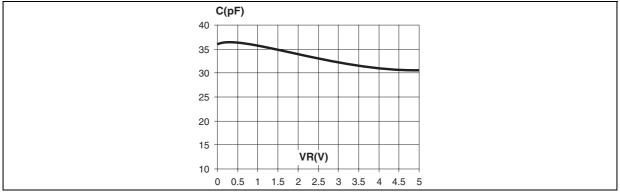
Figure 4. S21 (dB) attenuation measurement Figure 5. Analog crosstalk measurements











2 Application information

A1, A3, B2, C1, C3, E1, E3 R 1k3 3.8nH 02 Cbump Rsubump C1O () A3 C 1/00 Obulk 0.15nH Lbump 1k3 D02_usb 100m bulk Rbump R_33F 0.23nH 0.15nH D02_usb 🛓 **太** D02_Nw Lhole ₽ cap_33R Csub cap_33R Csub Rhole rsub_33R Rsub_D Lgnd_D Q 0.7nH ------OE3 0.3nH E1Ocap_33R cap_33R Csub Csub rsub_33R 33B rsub_

Figure 9. Aplac model (resistors, diodes and bumps and ground connections)

Figure 10. Aplac model parameters

R_33R 33.9 cap_33R 1.2pF	Model D02_Nw BV=100 IBV=1m	Model D02_usb BV=16 IBV=1m	
R_1k3 1.3k	CJO=6.8p M=0.3333	CJO=Cz M=0.3333	
Cz29pF Rsub_D 100	RS=2 VJ=0.6 TT=100n	RS=2 VJ=0.6 TT=100n	
Csub0.3pF Rsub_33R 15 Rsub_1k3 50			
lhole10pH Rhole400m Caphole0.4pF Lgnd_D 150pH			
Lbump50pH Rbump50m Cbump1.5pF Rsubump150			



3 Ordering information scheme

Figure 11. Ordering information scheme

EMI filter			
Number of lines			
Information			
x = resistance value (Ohms)			
z = capacitance value / 10(pF)			
or			
3 letters = application			
2 digits = version			
Package			
F = Flip Chip			
X = 2: lead-free, pitch = 500 μm,	, bump = 315 μm	1	

4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>. ECOPACK[®] is an ST trademark.

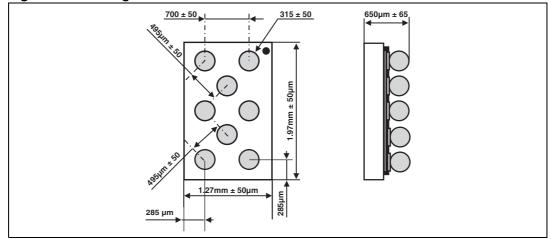


Figure 12. Package dimensions

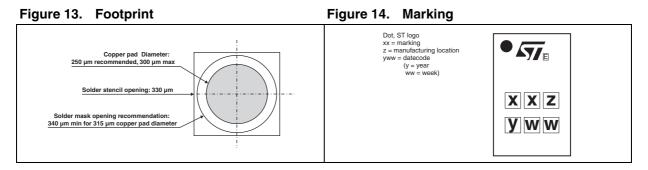
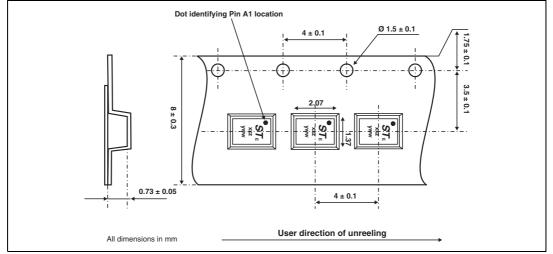


Figure 15. Flip Chip tape and reel specification



5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB01F2	FF	Flip Chip	3.35 mg	5000	Tape and reel 7"

Note: More information is available in the application notes: AN1235:"Flip Chip: Package description and recommendations for use" AN1751: "EMI filters: Recommendations and measurements"



6 Revision history

Table 4.Document revision history

Date	Revision	Changes
26-Oct-2004	1	Initial release.
16-Apr-2007	2	Updated ECOPACK statement. Updated <i>Figure 11</i> , <i>Figure 12</i> and <i>Figure 15</i> . Reformatted to current standards.
29-Apr-2008	3	Typographical errors corrected.
18-Sep-2009	4	Updated ESD graphic in <i>Figure 6</i> and <i>Figure 7</i> .



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