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## EMIF02-USB02F2

### 2-line IPAD™, EMI filter with ESD protection

#### **Features**

- 2-line low-pass filter + ESD protection
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space occupation < 3.2 mm<sup>2</sup>
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

#### Complies with the following standards:

- IEC 61000-4-2
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883E Method 3015-6 Class 3

### **Application**

EMI filtering and ESD p ctertion for USB port.

#### Description

The EMITO2-JSB02F2 is a highly integrated array designed to suppress EM. / RFI noise for a USB port. The EMIF02-US302F2 Flip Chip packaging means the package size is equal to the die size.

Additionally this filter includes ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

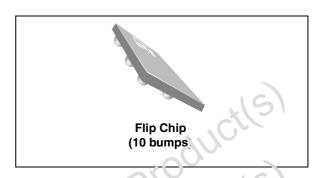


Figure 1. Pin layout (bump side)

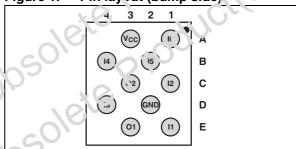
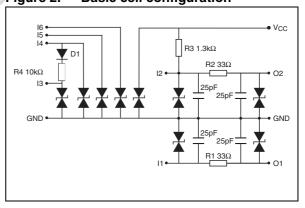


Figure 2. Basic cell configuration



Characteristics EMIF02-USB02F2

### 1 Characteristics

Table 1. Absolute ratings ( $T_{amb} = 25 \, ^{\circ}C$ )

Symbol	Parameter and test conditions	Value	Unit
V <sub>PP</sub>	ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	15 8	kV
T <sub>j</sub>	Junction temperature	125	°C
T <sub>op</sub>	Operating temperature range	- 40 to + 85	°C
T <sub>stg</sub>	Storage temperature range	- 55 to + 150	°C

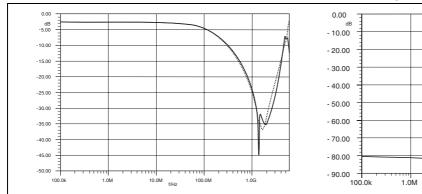
Table 2. Electrical characteristics ( $T_{amb} = 25$  °C)

Table 2.	Electrical characteristics (T <sub>amb</sub> = 25 °C)				<b>9</b> 1
Symbol	Parameter	I.		(J)	
$V_{BR}$	Breakdown voltage	IPP -		5	
I <sub>RM</sub>	Leakage current @ V <sub>RM</sub>	O			5
V <sub>RM</sub>	Stand-off voltage	IR .			
V <sub>CL</sub>	Clamping voltage	R VRM IRM.		<b>→</b>	V
R <sub>d</sub>	Dynamic impedance		RM VRM IR	VBR VCL	
I <sub>PP</sub>	Peak pulse current				
R <sub>I/O</sub>	Series resistance between input and output		lpp		
C <sub>line</sub>	Input capacitance car line	I			
Symbol	Test conditions	Min.	Тур.	Max.	Unit
V <sub>BR</sub>	I <sub>P</sub> – m A	6			V
I <sub>RK</sub>	V <sub>RM</sub> = 3V		0.1	0.5	μA
Cline	@ 0V			50	pF
R <sub>1</sub> ,R <sub>2</sub>	Tolerance ± 5%		33		Ω
R <sub>3</sub>	Tolerance ± 5%		1.3		kΩ
R <sub>4</sub>	Tolerance ± 5%		10		kΩ
$V_{F}$	@ 1 mA (D1 diode)		1		V
R <sub>4</sub>					

EMIF02-USB02F2 Characteristics

Figure 3. Attenuation measurement

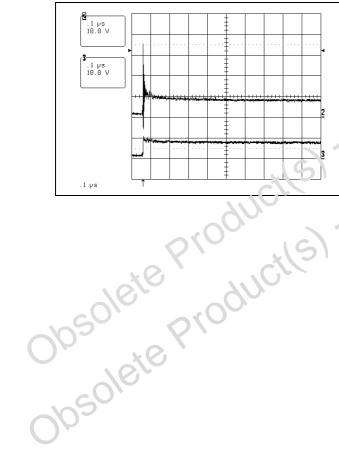
Figure 4. Analog crosstalk measurement (I1- O2)

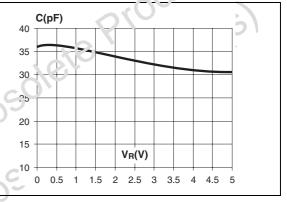


-10.00
-20.00
-30.00
-40.00
-50.00
-70.00
-80.00
-90.00
100.0k
1.0M
10.0M
1/Hz
100.0M
1.0G

Figure 5. ESD response to IEC 61000-4-2 (+15kV contact discharge)

Figure 6. Line capacitance versus reverse applied voltage





#### **Application information** 2

Figure 7. Aplac model of D+ & D- cells

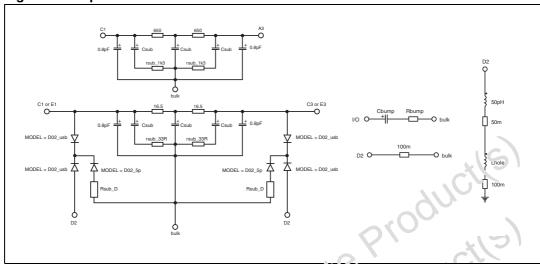
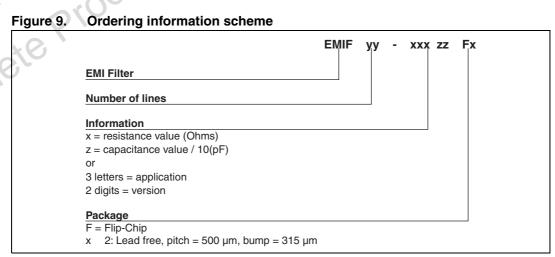


Figure 8. Aplac model parameters

```
Cz 17pF opt
                    D02_usb dio to model
                                              D02_5p diodes model
Ls 0.4nH
                    + P\'- \'
                                              + BV = 100
Rs 0.1
                    + BV = 1ni
                                              + IBV = 1m
Rsub_D 10
                    + CJC = Cz
                                              + CJO = 5p
Csub 0.3pF
                    + M = 0.3333
                                              + M = 0.3333
Rsub_33R 16
                    + RS = 2
                                              + RS = 2
Rsub_1k3 13
                    + VJ = 0.6
                                              + VJ = 0.6
Ihole 1.70p'H opt
                    + TT = 100n
                                              + TT = 100n
Cbi mp 1.2pr opt
Rt 11112 350
```

# **Sidering information scheme**

Ordering information scheme



EMIF02-USB02F2 Package information

### 4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at <a href="https://www.st.com">www.st.com</a>.

Figure 10. Flip Chip package dimensions

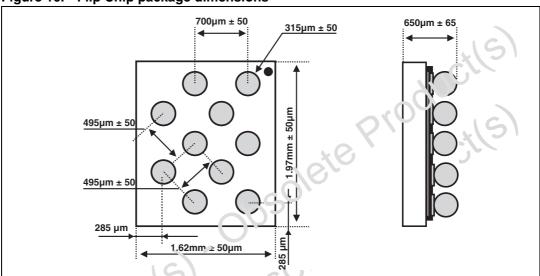
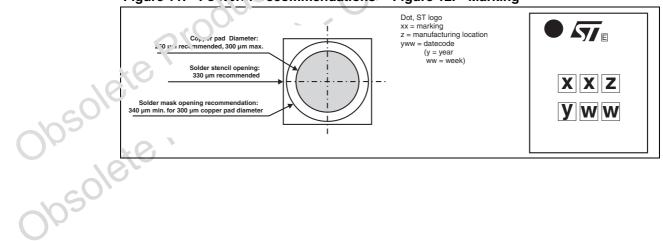


Figure 11. Footorint recommendations Figure 12. Marking



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Dot identifying Pin A1 location  $8 \pm 0.3$ 0.73 ± 0.05  $4 \pm 0.1$ User direction of unreeling All dimensions in mm

Figure 13. Flip Chip tape and reel specification

Note:

More information is available in the application notes:

#### **Ordering Information** 5

Table 3. Ordering information

More information is	available in t	the application	notes:	~4O	
AN1235: "Flip Chip: Package description and recommendations for use"					
AN1751: "EMI Filte	rs: Recomme	endations and	measureา.รก	ts"	'C'
AN1751: "EMI Filters: Recommendations and measurements"  Ordering Information					
Table 3. Ordering information					
Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB02-2	FG	Flip Chip	4.25 mg	5000	Tape and reel 7"

## Revision history

**Document revision history** 

Date	Revision	Changes		
14-Dec-2004	1	First issue		
28-Apr-2008	2	Updated ECOPACK statement. Updated Figure 9, Figure 10, Figure 12, and Figure 13. Reformatted to current standards.		

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