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Features

- High design flexibility
- Lead free package
- Very low PCB space consumption: 3.5 mm x 1.2 mm
- Very thin package: 0.5 mm
- High efficiency in ESD suppression
- IEC 61000-4-2 level 4
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and μ QFN packaging

Complies with following standards:

- IEC 61000-4-2 level 4 external pins

Applications

- Mobile telephones,
- Navigation systems
- Digital still cameras
- Portable devices.

Description

The EMIF06-MSD02N16 is a highly integrated device designed to suppress EMI/RFI noise for interface line filtering. It is packaged in micro QFN.

This filter includes ESD protection circuitry, which prevents damage to the protected device when subjected to ESD surges.

TM: IPAD is a trademark of STMicroelectronics

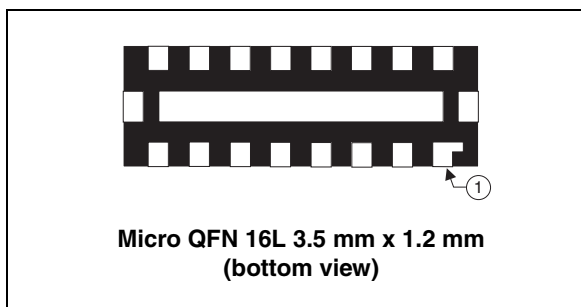


Figure 1. Pin configuration

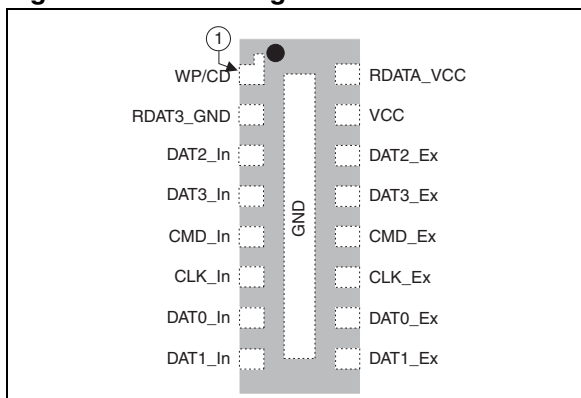
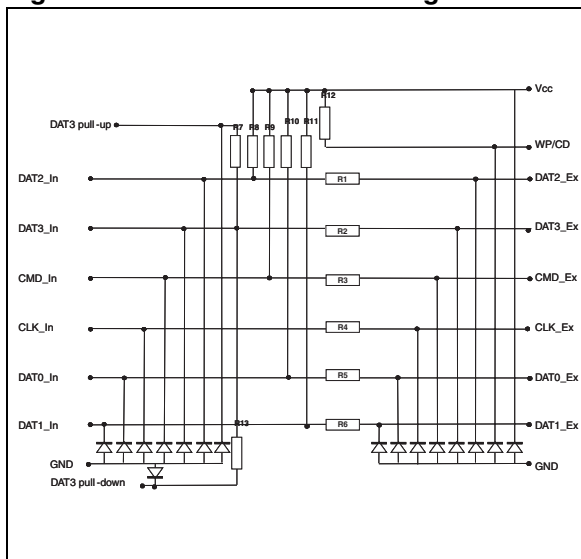


Figure 2. Schematic circuit diagram



1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V _{PP}	ESD IEC 61000-4-2	2	kV
	Contact discharge on DATx_In, CMD_In and CLK_In pins		
	On all other pins		
V _{PP}	Contact discharge	8	kV
	Air discharge	12	
T _j	Maximum junction temperature	125	°C
T _{op}	Operating temperature range	- 30 to + 85	°C
T _{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter				
V _{BR}	Breakdown voltage				
I _{RM}	Leakage current @ V _{RM}				
V _{RM}	Stand-off voltage				
V _{CL}	Clamping voltage				
R _d	Dynamic resistance				
I _{PP}	Peak pulse current				
R _{I/O}	Series resistance between Input & Output				
C _{LINE}	Input capacitance per line				
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V _{BR}	I _R = 1 mA	5		8	V
I _{RM}	V _{RM} = 3 V			200	nA
R ₁ , R ₂ , R ₃ , R ₄ , R ₅ , R ₆	Series resistors - tolerance ±20%	36	45	54	Ω
R ₇ , R ₈ , R ₉ , R ₁₀ , R ₁₁ , R ₁₂	Pull-up resistors	80	90	100	kΩ
R ₁₃	Pull-down resistor - tolerance ±20%	375	470	565	kΩ
C _{line}	V _{LINE} = 0 V, V _{OSC} = 30 mV, F = 1 MHz (under zero light conditions)			20	pF

Figure 3. S21 attenuation measurement

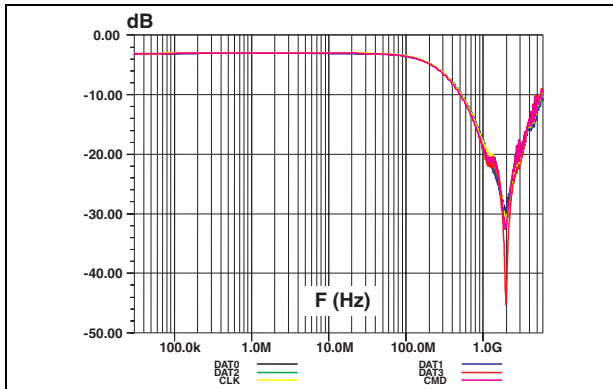


Figure 4. Analog cross talk measurements

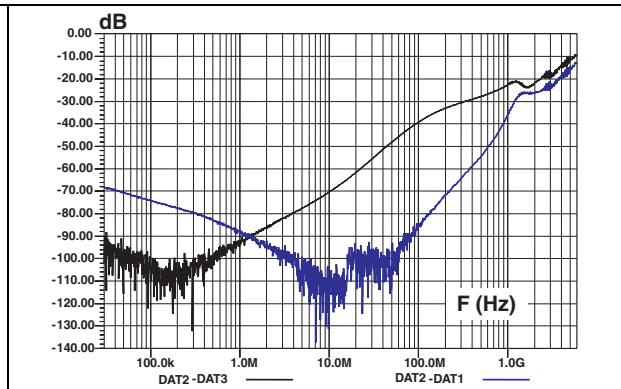


Figure 5. ESD response to IEC 61000-4-2 (+12 kV air discharge) on one input (V_{in}) and on one output (V_{out})

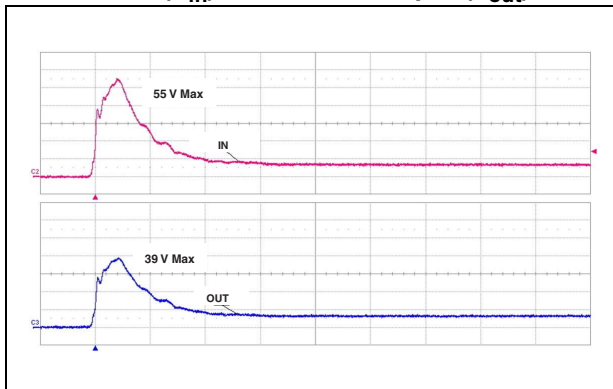


Figure 6. ESD response to IEC 61000-4-2 (-12 kV air discharge) on one input (V_{in}) and on one output (V_{out})

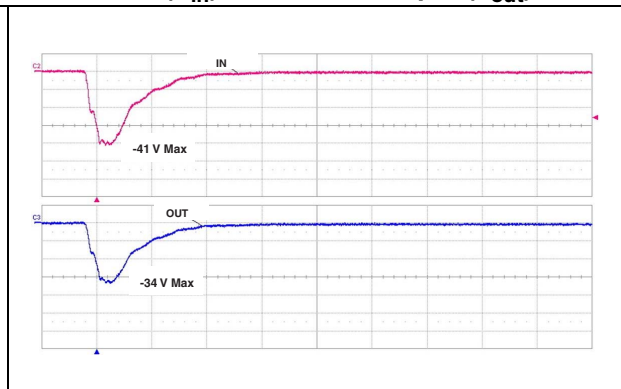
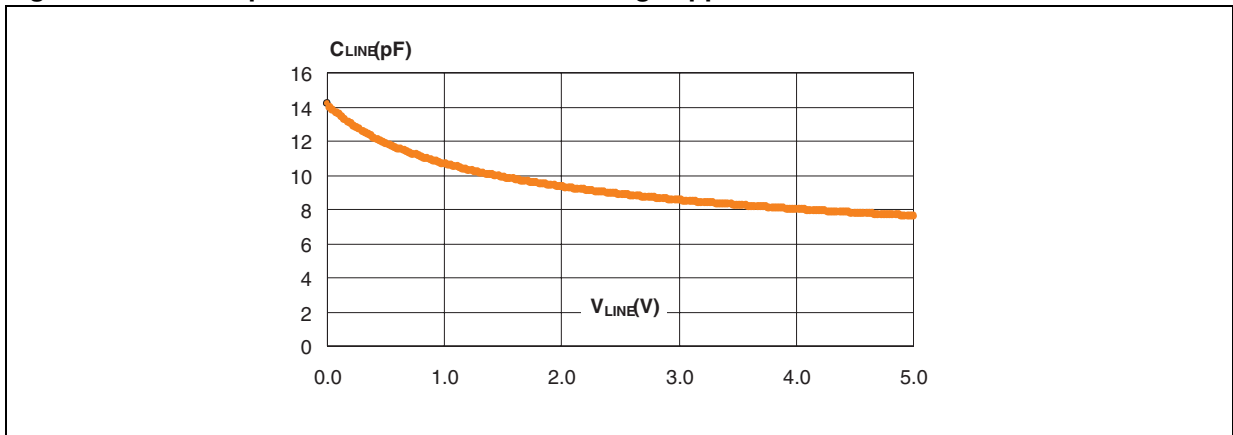


Figure 7. Line capacitance versus reverse voltage applied on DATx and CMD line



2 Application information

The EMIF06-mSD02N16 is a dedicated interface device for micro SD card/T-Flash card in mobile phones. The device provides:

- ESD protection
- EMI filtering
- Pull-up resistors
- Card detection circuit

2.1 ESD protection

Each pin is connected to a TVS diode able to withstand 12 kV on all pins except on DATx_In, CMD_In and CLK_In.

2.2 EMI filtering

DATx, CMD and CLK lines are immunized against EMI radiations thanks to pi-filters. To avoid any degradation of the signal integrity at high frequency, the total line capacitance stays lower than 20 pF making the device compatible with a clock frequency up to 52 MHz.

2.3 Pull-up resistors

As recommended by the SD Specifications (Part 1 Physical Layer Version 2.00), all the data lines DATx and the CMD line must be pulled-up with resistors of 10 to 100 k Ω to avoid bus floating not only in SD 4-bit mode but also in SD 1-bit and SPI mode.

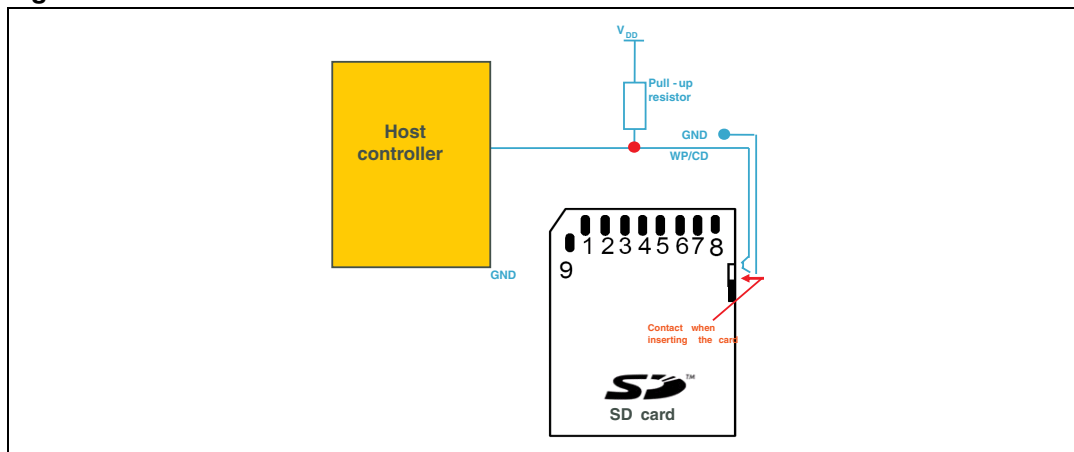
For the EMIF06-MSD02N16 device the pull-up resistor value has been fixed at 90 k Ω . This value makes the EMIF06-MSD02N16 compatible with most of the level shifters that may be used in the circuit including auto direction-sensing translators known to exhibit a weak current output.

2.4 Card detection circuit

The EMIF06-mSD02N16 provides the flexibility to use either mechanical card detection with a dedicated pin connected to the memory card slot or the electrical card detection using the internal pull resistor of DAT3 of the micro SD card/T-Flash card.

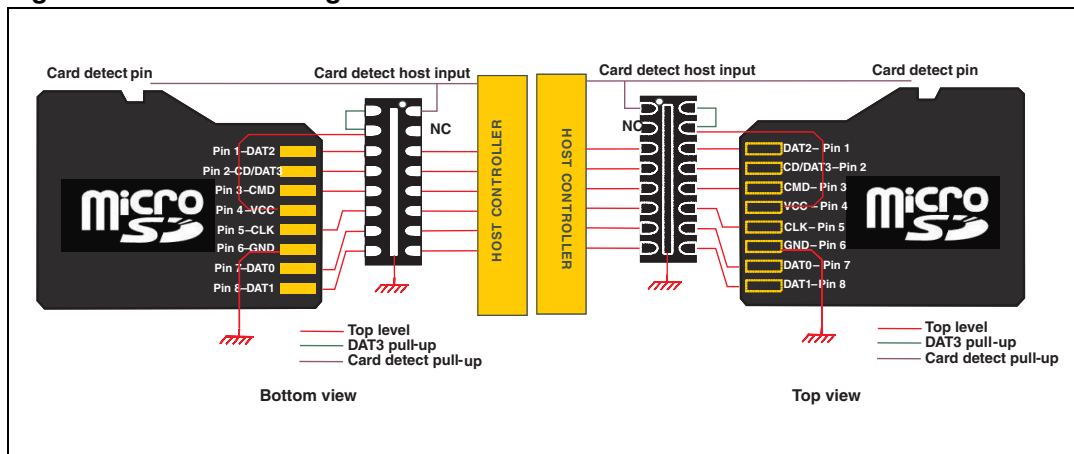
In case of mechanical card detection, the user must add a pull-up on the circuit connected to the CD (Card Detect) of the micro-SD/T-Flash slot as shown in [Figure 8](#).

Figure 8. Mechanical card detection



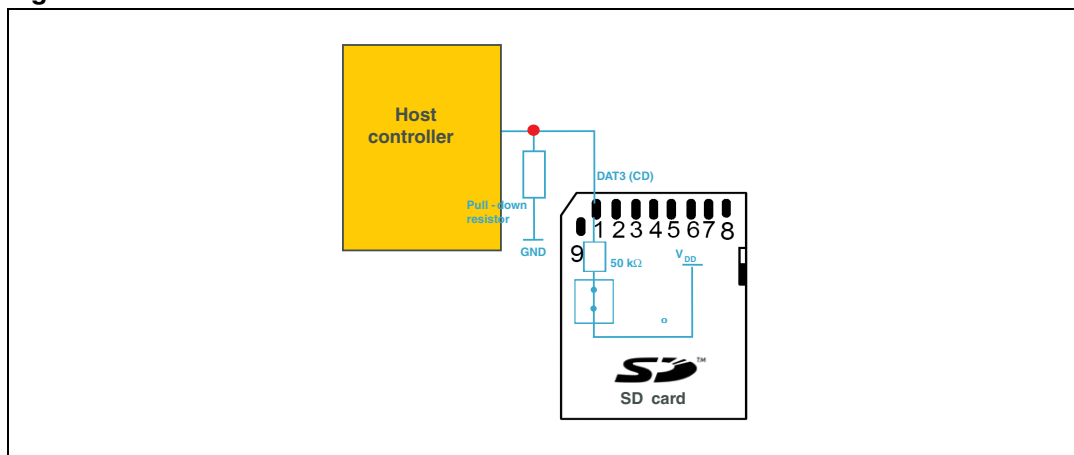
A pull-up of 90 kΩ is embedded into the EMIF06-MSD02N16. The routing corresponding to the mechanical card detection configuration is shown in [Figure 9](#).

Figure 9. Circuit routing for mechanical card detection



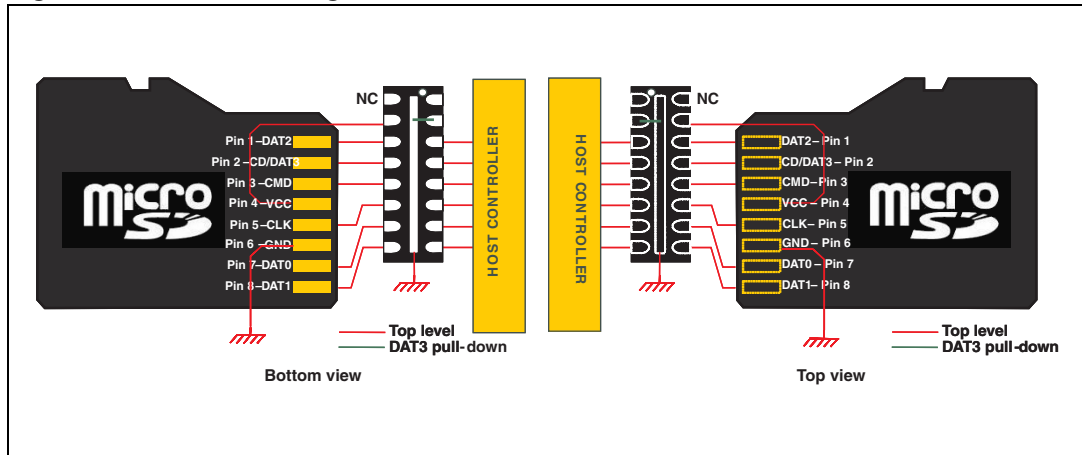
In case of electrical card detection, the user must add a pull-down on the circuit connected to the CD/DAT3 pin of the micro-SD/T-Flash pin as shown in [Figure 10](#).

Figure 10. Electrical card detection



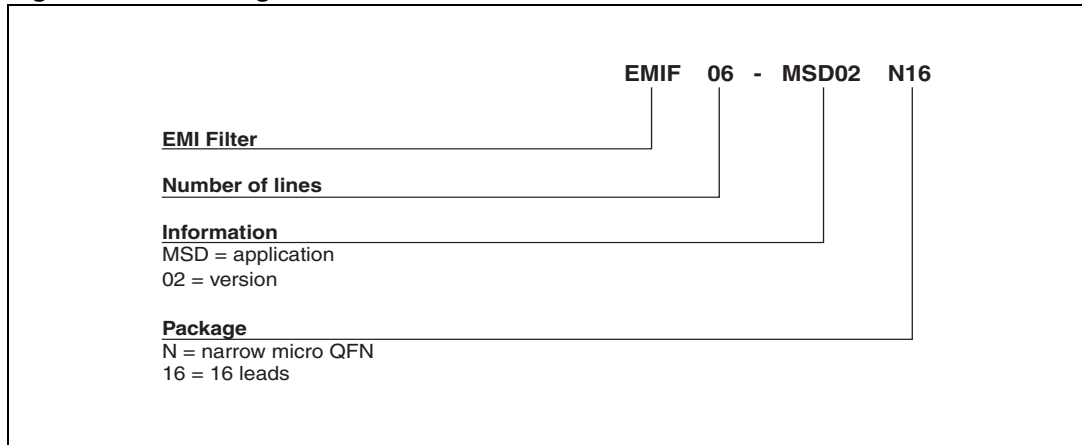
A pull-down of 470k is embedded into the EMIF06-mSD02N16. The routing corresponding to the electrical card detection configuration is shown in the [Figure 11](#).

Figure 11. Circuit routing for electrical card detection



3 Ordering information scheme

Figure 12. Ordering information scheme



4 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Table 3. Micro QFN 3.5x1.2 16L dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00		0.05	0.000		0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.25	0.30	0.35	0.010	0.012	0.014
D	3.45	3.50	3.55	0.136	0.138	0.140
D2	2.70	2.80	2.90	0.106	0.110	0.114
E	1.15	1.20	1.25	0.045	0.047	0.049
E2	0.25	0.30	0.40	0.010	0.012	0.016
e		0.40			0.016	
k		0.20			0.008	
L	0.20	0.25	0.30	0.008	0.010	0.012
L1		0.15			0.006	
M		0.20			0.008	

Figure 13. Micro QFN 3.5x1.2 16L footprint (dimensions in mm)

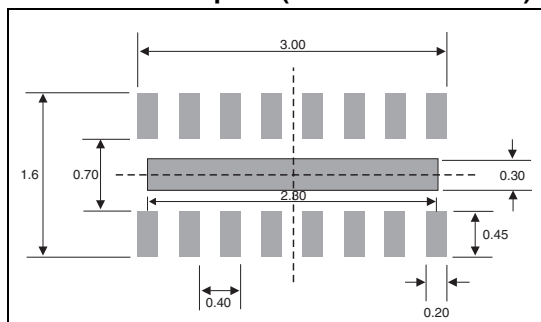


Figure 14. Marking

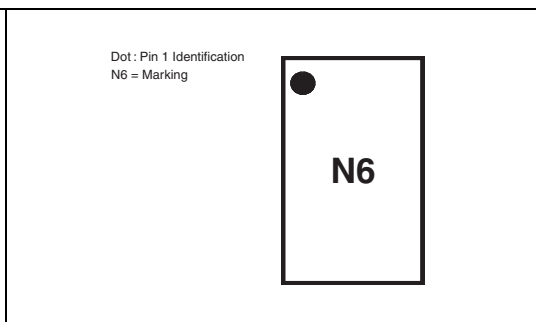
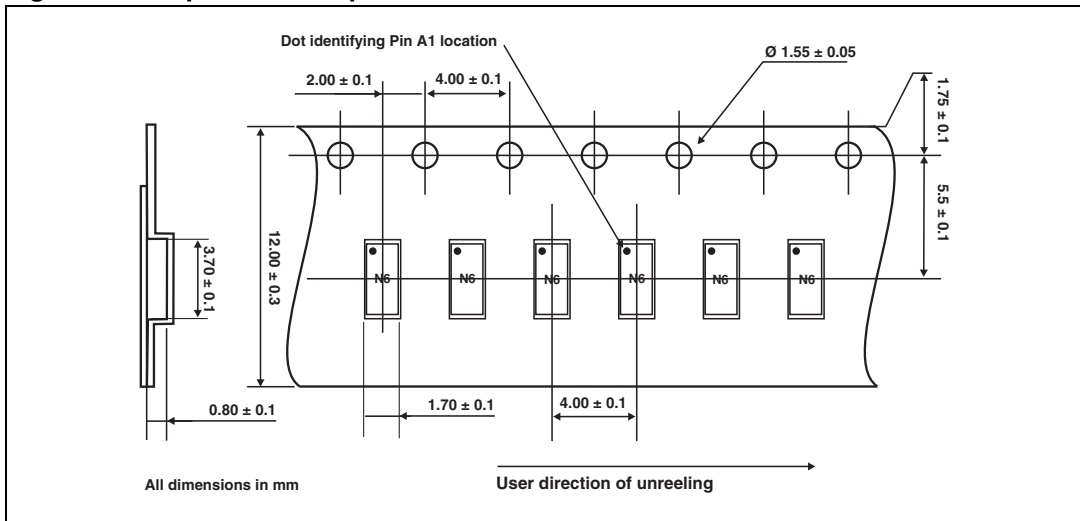


Figure 15. Tape and reel specification



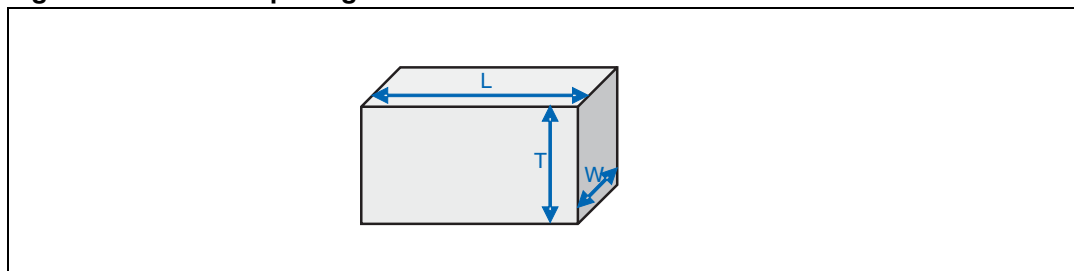
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

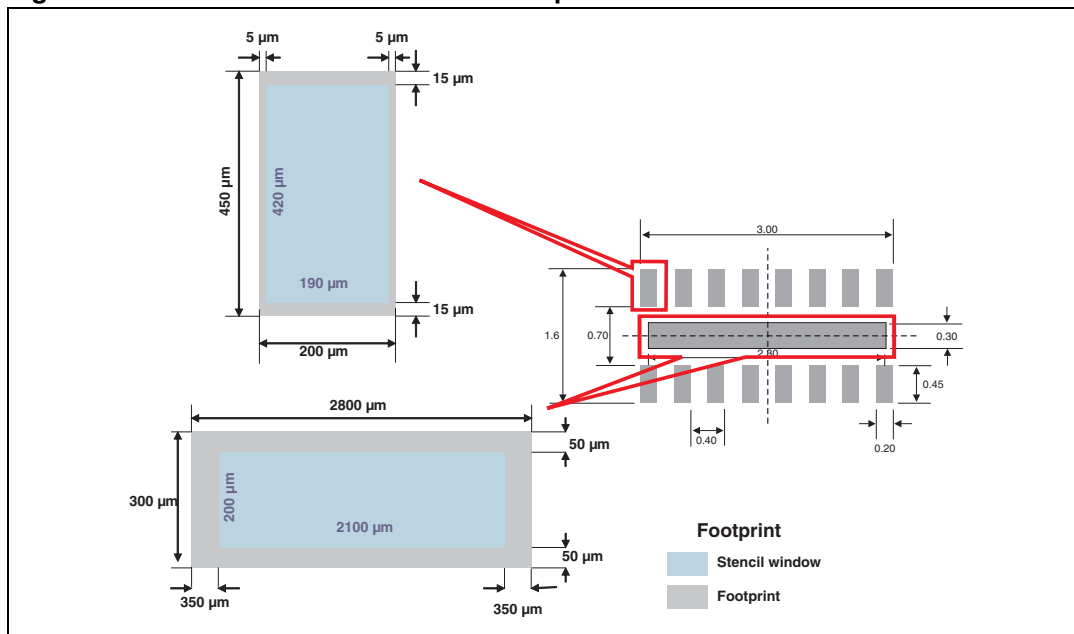
Figure 16. Stencil opening dimensions



- b) General design rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - Aspect Ratio = $\frac{W}{T} \geq 1.5$
 - Aspect Area = $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Reference design
 - a) Stencil opening thickness: 100 μm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 17. Recommended stencil window position



5.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 μm .

5.3 Placement

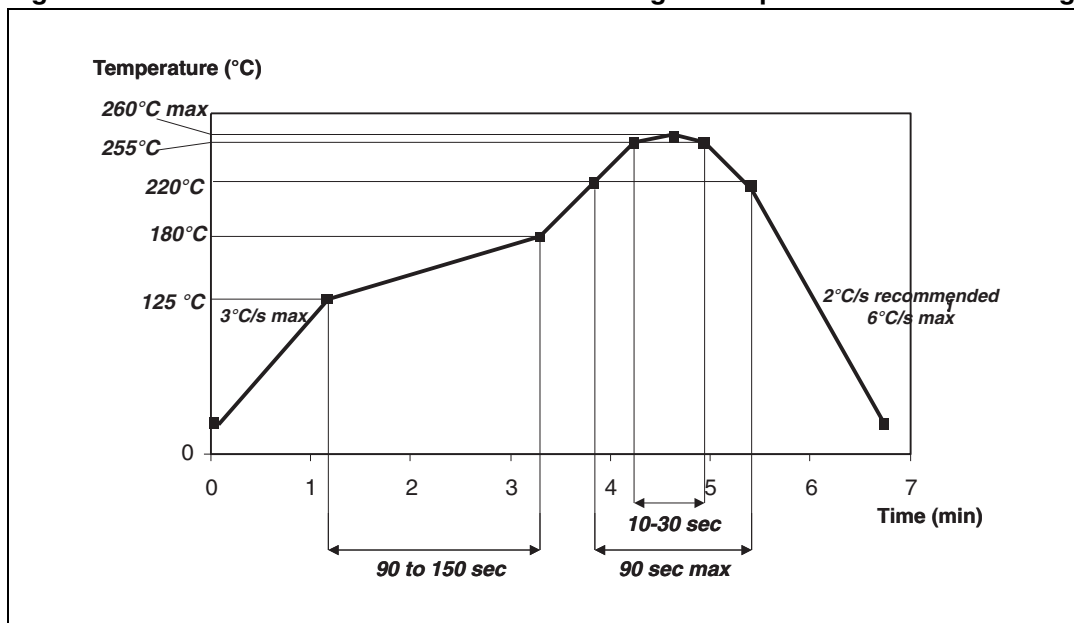
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-MSDN16	N6 ⁽¹⁾	Micro QFN	6.17 mg	3000	Tape and reel (7")

1. The marking can be rotated by 90° to differentiate assembly location

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
21-Nov-2008	1	Initial release.

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