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EMIF10-LCD01F2

10 line EMI filter and ESD protection

Main product characteristics:

Where EMI filtering in ESD sensitive equipment is required:

- LCD for Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

Description

The EMIF10-LCD01F2 is a 10 line highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

Benefits

- EMI symmetrica: ('/O) low-pass filter
- High efficiency in EMI filtering
- Very lov CB space consuming: < 6 mm²
- Leag free package
- very thin package: 0.69 mm
- High efficiency in ESD suppression on input pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging.

Complies with following standards:

IEC 61000-4-2

level 4 input pins 15 kV (air discharge)

8 kV (contact discharge)

MIL STD 883G - Method 3015-7 Class 3



Order code

Part Number	Marking		
≦/JIF10-LCD01F2	FL		

Figure 1. Pin Configuration (bump side)

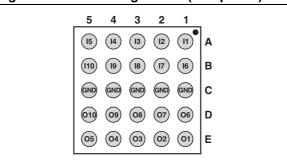
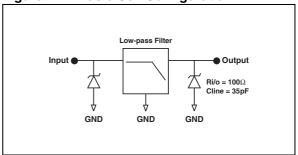


Figure 2. Basic Cell Configuration



TM: IPAD is a trademark of STMicroelectronics.

Characteristics EMIF10-LCD01F2

1 Characteristics

Table 1. Absolute Maximum Ratings $(T_{amb} = 25^{\circ} C)$

Symbol	Parameter	Value	Unit
T _j	Junction temperature	125	° C
T _{op}	Operating temperature range	-40 to + 85	° C
T _{stg}	Storage temperature range	-55 to +150	° C

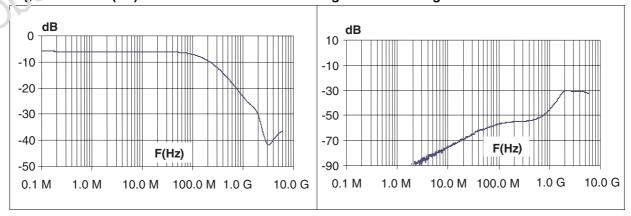
Table 2. Electrical Characteristics $(T_{amb} = 25^{\circ} C)$

Symbol	Parameter	1
V _{BR}	Breakdown voltage	le (5)
I _{RM}	Leakage current @ V _{RM}	
V _{RM}	Stand-off voltage	
V _{CL}	Clamping voltage	VCL VBR VF W
R _d	Dynamic resistance	
I _{PP}	Peak pulse current	76,
R _{I/O}	Series resistance between Input and Output	
C _{line}	Input capacitance per line	

Symbol	Test conditions	Min.	Тур.	Max.	Unit
V_{BR}	I _R = 1 mA	6	8	10	٧
I _{RM}	V _{RM} = 3 V			500	nA
R _{I/O}	100	90	100	110	Ω
C _{line}	@ 0 V 's s		28	35	pF
Rt / Ft	Induceo rise and fall time 10-90% at 26 MHz frequency signal $V = 1.9 \text{ V}$ (Rt / Ft input 1 ns, 50Ω impedance generator)		8 ⁽¹⁾		ns

^{1.} guaranเจะd by design

Figure 3. S21(dB) attenuation measurement Figure 4. Analog cross talk measurement



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EMIF10-LCD01F2 Characteristics

Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input and on one output

Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input and on one output

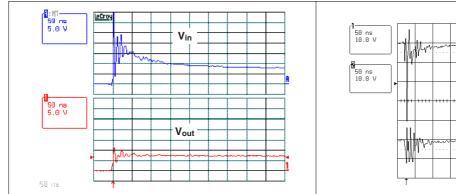
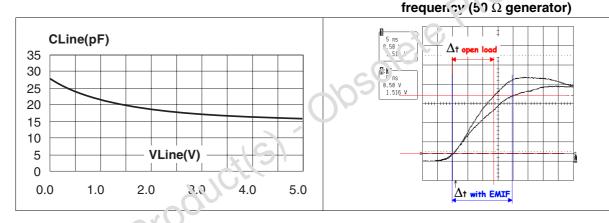


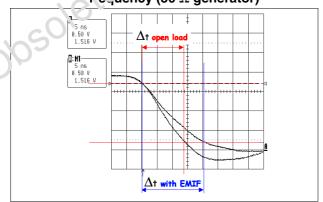
Figure 7. Line capacitance versus applied voltage

Figure 8. Rise time 10-90% incasurements with 1.9 V signal at 26 MHz

Vout



Fall time 10-90% measurements with 1.5 V signal at 26 MHz requency (50 Ω generator)



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Characteristics EMIF10-LCD01F2

Figure 10. Aplac model

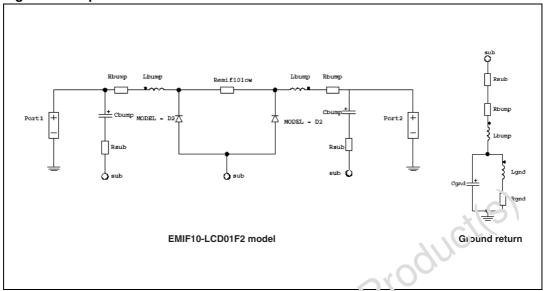
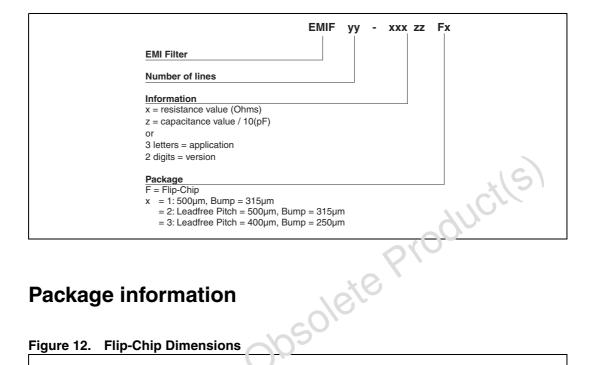


Figure 11. Aplac parametersl

	ZRZ structure aplacvar Remif10low 100 aplacvar Cemif10flow 17.5pr Bumps aplacvar Lbump 50pH aplacvar Rbunp 20n aplacvar Chump 1.5pF Bulk aplacvar Rsub 100m Cha connections aplacvar Rgnd 100m	BV = 7 CJO = Cemif10low IBV = 1u IKF = 1000 IS = 10f ISR = 100p N = 1 M = 0.3333 RS = 0.015 VJ = 0.6	
	aplacvar C ხump 1.5pF Bulk ap!გიvar Rsub 100m Chra connections	ISR = 100p N = 1 M = 0.3333 RS = 0.015	
Obsolete	aplacvar Cgnd 0.15pF	11 – 3011	

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Ordering information scheme 2



Package information 3

Figure 12. Flip-Chip Dimensions

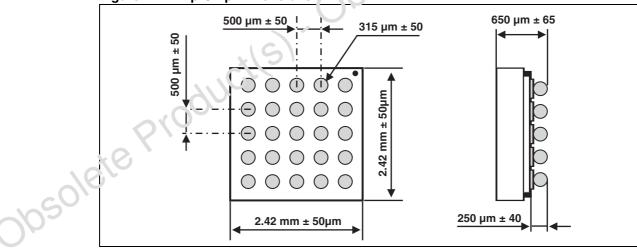


Figure 13. Marking Figure 14. Footprint recommendation Copper pad Diameter: 250µm recommended, 300 µm max **√7**/_□ XXZ Solder stencil opening: 330 µm y w w 340 µm min for 315 µm copper pad dia

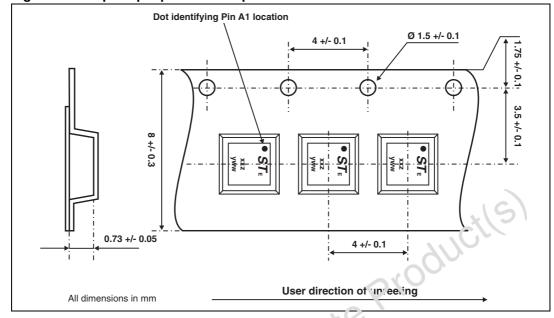


Figure 15. Flip-Chip tape and reel specification

In order to meet environmental requirements, ST offers those devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESDET. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: More packing information is available in the application notes:

AN1235: "Flip-Chip: Package description and recommendations for use"

AN1751: "EMI Filters' Fiecommendations and measurements"

4 Crdering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-LCD01F2	FL	Flip-Chip	9.3 mg	5000	Tape and reel (7")

EMIF10-LCD01F2 Revision history

5 Revision history

Date	Revision	Changes	
14-Feb-2005 1		Initial release.	
17-Mar-2005 2		Capacitance C_{line} specification changed from 47 pF (typ) to 28 pF (typ) and 35 pF (max).	
30-Jan-2007 3		Reformatted to current standards. Reduced die size and updated Figures 3 and 4.	

Obsolete Productis).

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