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ENC28J60

Stand-Alone Ethernet Controller with SPI Interface

Ethernet Controller Features

- IEEE 802.3™ Compatible Ethernet Controller
- Fully Compatible with 10/100/1000Base-T Networks
- Integrated MAC and 10Base-T PHY
- Supports One 10Base-T Port with Automatic Polarity Detection and Correction
- Supports Full and Half-Duplex modes
- Programmable Automatic Retransmit on Collision
- Programmable Padding and CRC Generation
- Programmable Automatic Rejection of Erroneous Packets
- SPI Interface with Clock Speeds up to 20 MHz

Buffer

- 8-Kbyte Transmit/Receive Packet Dual Port SRAM
- Configurable Transmit/Receive Buffer Size
- Hardware Managed Circular Receive FIFO
- Byte-Wide Random and Sequential Access with Auto-Increment
- Internal DMA for Fast Data Movement
- Hardware Assisted Checksum Calculation for Various Network Protocols

Medium Access Controller (MAC) Features

- Supports Unicast, Multicast and Broadcast Packets
- Programmable Receive Packet Filtering and Wake-up Host on Logical AND or OR of the Following:
  - Unicast destination address
  - Multicast address
  - Broadcast address
  - Magic Packet™
  - Group destination addresses as defined by 64-bit Hash Table
  - Programmable Pattern Matching of up to 64 bytes at user-defined offset

Physical Layer (PHY) Features

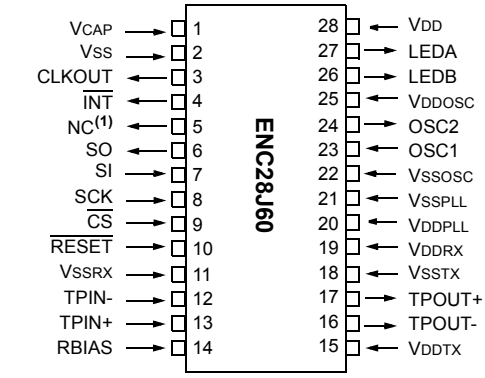
- Loopback mode
- Two Programmable LED Outputs for LINK, TX, RX, Collision and Full/Half-Duplex Status

Operational

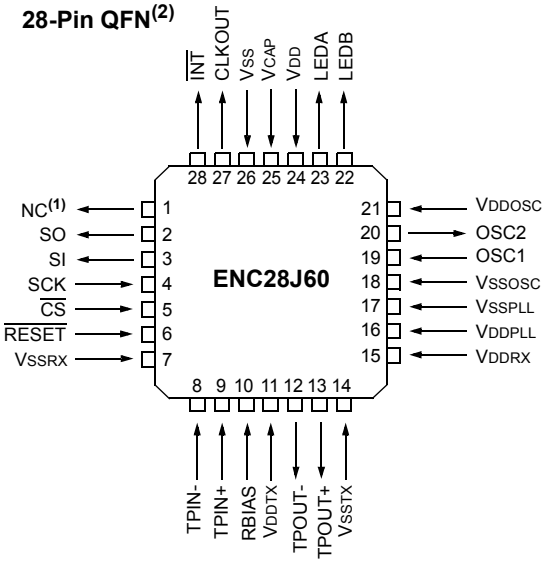
- Six Interrupt Sources and One Interrupt Output Pin
- 25 MHz Clock Input Requirement
- Clock Out Pin with Programmable Prescaler
- Operating Voltage of 3.1V to 3.6V (3.3V typical)
- 5V Tolerant Inputs
- Temperature Range: -40°C to +85°C Industrial, 0°C to +70°C Commercial (SSOP only)
- 28-Pin SPDIP, SSOP, SOIC, QFN Packages

Package Types

28-Pin SPDIP, SSOP, SOIC



28-Pin QFN(2)



Note 1: Reserved pin; always leave disconnected.
2: The back pad on QFN devices should be connected to Vss.

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1.0 OVERVIEW

The ENC28J60 is a stand-alone Ethernet controller with an industry standard Serial Peripheral Interface (SPI). It is designed to serve as an Ethernet network interface for any controller equipped with SPI.

The ENC28J60 meets all of the IEEE 802.3 specifications. It incorporates a number of packet filtering schemes to limit incoming packets. It also provides an internal DMA module for fast data throughput and hardware assisted checksum calculation, which is used in various network protocols. Communication with the host controller is implemented via an interrupt pin and the SPI, with clock rates of up to 20 MHz. Two dedicated pins are used for LED link and network activity indication.

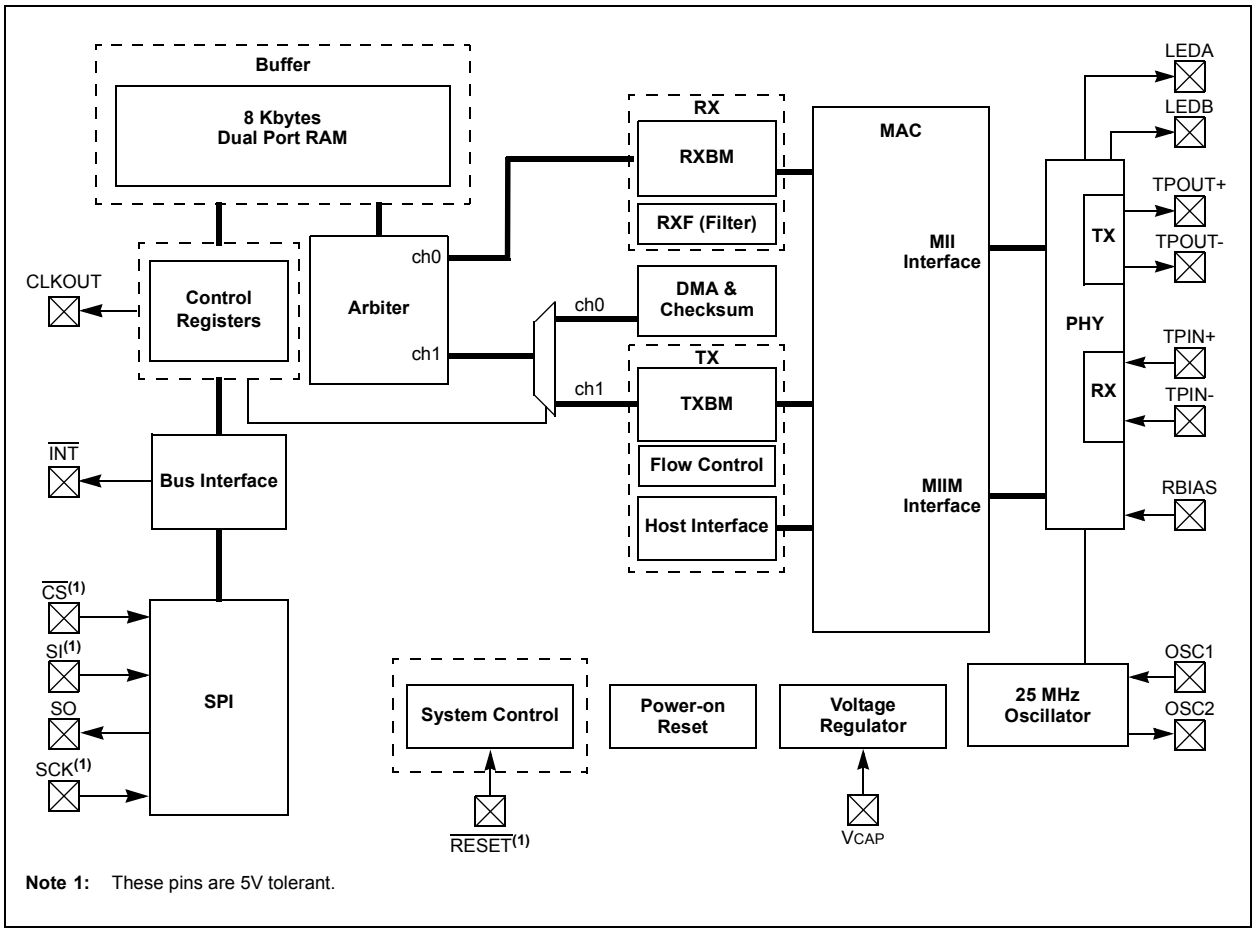
A simple block diagram of the ENC28J60 is shown in Figure 1-1. A typical application circuit using the device is shown in Figure 1-2. With the ENC28J60, two pulse transformers and a few passive components are all that are required to connect a microcontroller to an Ethernet network.

The ENC28J60 consists of seven major functional blocks:

1. An SPI interface that serves as a communication channel between the host controller and the ENC28J60.
2. Control registers which are used to control and monitor the ENC28J60.
3. A dual port RAM buffer for received and transmitted data packets.
4. An arbiter to control the access to the RAM buffer when requests are made from DMA, transmit and receive blocks.
5. The bus interface that interprets data and commands received via the SPI interface.
6. The MAC (Medium Access Control) module that implements IEEE 802.3 compliant MAC logic.
7. The PHY (Physical Layer) module that encodes and decodes the analog data that is present on the twisted-pair interface.

The device also contains other support blocks, such as the oscillator, on-chip voltage regulator, level translators to provide 5V tolerant I/Os and system control logic.

FIGURE 1-1: ENC28J60 BLOCK DIAGRAM



Note 1: These pins are 5V tolerant.

FIGURE 1-2: TYPICAL ENC28J60 BASED INTERFACE

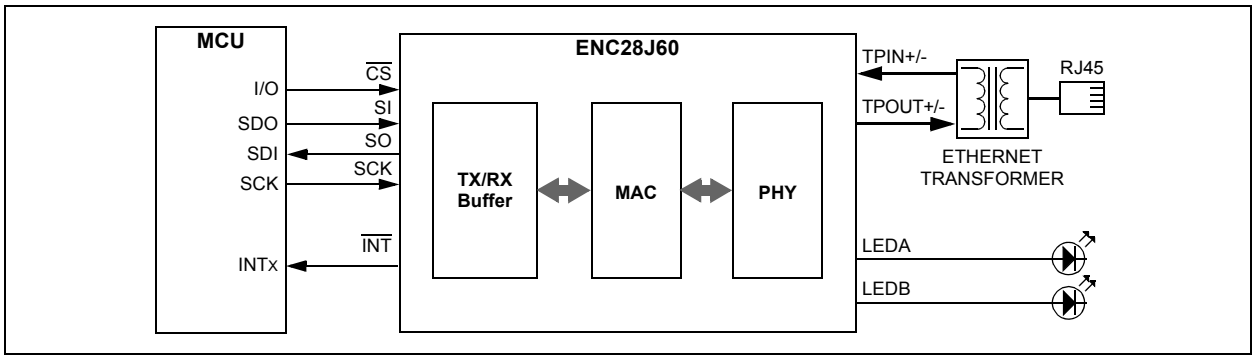


TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	SPDIP, SOIC, SSOP	QFN			
VCAP	1	25	P	—	2.5V output from internal regulator. A low Equivalent Series Resistance (ESR) capacitor, with a typical value of 10 µF and a minimum value of 1 µF to ground, must be placed on this pin.
VSS	2	26	P	—	Ground reference.
CLKOUT	3	27	O	—	Programmable clock output pin.(1)
$\overline{INT}$	4	28	O	—	$\overline{INT}$ interrupt output pin.(2)
NC	5	1	O	—	Reserved function; always leave unconnected.
SO	6	2	O	—	Data out pin for SPI interface.(2)
SI	7	3	I	ST	Data in pin for SPI interface.(3)
SCK	8	4	I	ST	Clock in pin for SPI interface.(3)
$\overline{CS}$	9	5	I	ST	Chip select input pin for SPI interface.(3,4)
$\overline{RESET}$	10	6	I	ST	Active-low device Reset input.(3,4)
VSSRX	11	7	P	—	Ground reference for PHY RX.
TPIN-	12	8	I	ANA	Differential signal input.
TPIN+	13	9	I	ANA	Differential signal input.
RBIAS	14	10	I	ANA	Bias current pin for PHY. Must be tied to ground via a resistor (refer to **Section 2.4 "Magnetics, Termination and Other External Components"** for details).
VDDTX	15	11	P	—	Positive supply for PHY TX.
TPOUT-	16	12	O	—	Differential signal output.
TPOUT+	17	13	O	—	Differential signal output.
VSSTX	18	14	P	—	Ground reference for PHY TX.
VDDRX	19	15	P	—	Positive 3.3V supply for PHY RX.
VDDPLL	20	16	P	—	Positive 3.3V supply for PHY PLL.
VSSPLL	21	17	P	—	Ground reference for PHY PLL.
VSSOSC	22	18	P	—	Ground reference for oscillator.
OSC1	23	19	I	ANA	Oscillator input.
OSC2	24	20	O	—	Oscillator output.
VDDOSC	25	21	P	—	Positive 3.3V supply for oscillator.
LEDB	26	22	O	—	LEDB driver pin.(5)
LEDA	27	23	O	—	LEDA driver pin.(5)
VDD	28	24	P	—	Positive 3.3V supply.

Legend: I = Input, O = Output, P = Power, ANA = Analog Signal Input, ST = Schmitt Trigger

Note 1: Pins have a maximum current capacity of 8 mA.

2: Pins have a maximum current capacity of 4 mA.

3: Pins are 5V tolerant.

4: Pins have an internal weak pull-up to VDD.

5: Pins have a maximum current capacity of 12 mA.

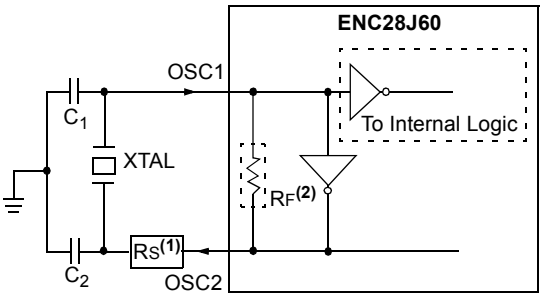
2.0 EXTERNAL CONNECTIONS

2.1 Oscillator

The ENC28J60 is designed to operate at 25 MHz with a crystal connected to the OSC1 and OSC2 pins. The ENC28J60 design requires the use of a parallel resonance crystal. Use of a series resonance crystal may give a frequency out of the crystal manufacturer specifications. A typical oscillator circuit is shown in Figure 2-1.

The ENC28J60 may also be driven by an external clock source connected to the OSC1 pin as shown in Figure 2-2.

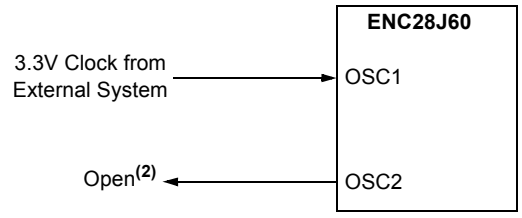
FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION



Note 1: A series resistor, RS, may be required for AT strip cut crystals.

2: The feedback resistor, RF, is typically in the range of 2 to 10 MΩ.

FIGURE 2-2: EXTERNAL CLOCK SOURCE(1)



Note 1: Duty cycle restrictions must be observed.

2: A resistor to ground may be used to reduce system noise. This may increase system current.

2.2 Oscillator Start-up Timer

The ENC28J60 contains an Oscillator Start-up Timer (OST) to ensure that the oscillator and integrated PHY have stabilized before use. The OST does not expire until 7500 OSC1 clock cycles (300 μs) pass after Power-on Reset or wake-up from Power-Down mode occurs. During the delay, all Ethernet registers and buffer memory may still be read and written to through the SPI bus. However, software should not attempt to transmit any packets (set ECON1.TXRTS), enable reception of packets (set ECON1.RXEN) or access any MAC, MII or PHY registers during this period.

When the OST expires, the CLKRDY bit in the ESTAT register will be set. The application software should poll this bit as necessary to determine when normal device operation can begin.

Note: After a Power-on Reset, or the ENC28J60 is removed from Power-Down mode, the CLKRDY bit must be polled before transmitting packets, enabling packet reception or accessing any MAC, MII or PHY registers.

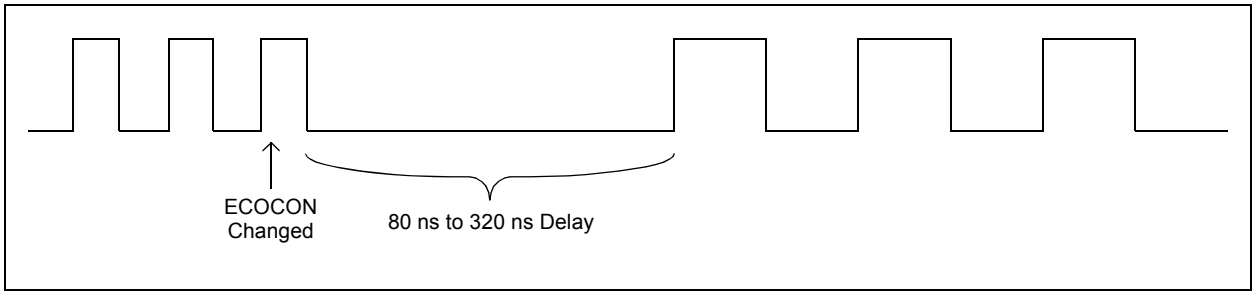
2.3 CLKOUT Pin

The Clock Out (CLKOUT) pin is provided to the system designer for use as the host controller clock or as a clock source for other devices in the system. The CLKOUT has an internal prescaler which can divide the output by 1, 2, 3, 4 or 8. The CLKOUT function is enabled and the prescaler is selected via the ECOCON register (Register 2-1).

To create a clean clock signal, the CLKOUT pin is held low for a period when power is first applied. After the Power-on Reset ends, the OST will begin counting. When the OST expires, the CLKOUT pin will begin outputting its default frequency of 6.25 MHz (main clock divided by 4). At any future time that the ENC28J60 is reset by software or the $\overline{\text{RESET}}$ pin, the CLKOUT function will not be altered (ECOCON will not change value). Additionally, Power-Down mode may be entered and the CLKOUT function will continue to operate. When Power-Down mode is cancelled, the OST will be reset but the CLKOUT function will continue. When the CLKOUT function is disabled (ECOCON = 0), the CLKOUT pin is driven low.

The CLKOUT function is designed to ensure that minimum timings are preserved when the CLKOUT pin function is enabled, disabled or the prescaler value is changed. No high or low pulses will be outputted which exceed the frequency specified by the ECOCON configuration. However, when switching frequencies, a delay between two and eight OSC1 clock periods will occur where no clock pulses will be produced (see Figure 2-3). During this period, CLKOUT will be held low.

FIGURE 2-3: CLKOUT TRANSITION



REGISTER 2-1: ECOCON: CLOCK OUTPUT CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	COCON2	COCON1	COCON0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **COCON<2:0>**: Clock Output Configuration bits

11x = Reserved for factory test, do not use; glitch prevention is not assured
101 = CLKOUT outputs main clock divided by 8 (3.125 MHz)
100 = CLKOUT outputs main clock divided by 4 (6.25 MHz)
011 = CLKOUT outputs main clock divided by 3 (8.333333 MHz)
010 = CLKOUT outputs main clock divided by 2 (12.5 MHz)
001 = CLKOUT outputs main clock divided by 1 (25 MHz)
000 = CLKOUT is disabled, the pin is driven low

2.4 Magnetics, Termination and Other External Components

To complete the Ethernet interface, the ENC28J60 requires several standard components to be installed externally. These components should be connected as shown in Figure 2-4.

The internal analog circuitry in the PHY module requires that an external 2.32 kΩ, 1% resistor be attached from RBIAS to ground. The resistor influences the TPOUT+/- signal amplitude. The resistor should be placed as close as possible to the chip with no immediately adjacent signal traces to prevent noise capacitively coupling into the pin and affecting the transmit behavior. It is recommended that the resistor be a surface mount type.

Some of the device's digital logic operates at a nominal 2.5V. An on-chip voltage regulator is incorporated to generate this voltage. The only external component required is an external filter capacitor, connected from VCAP to ground. The capacitor must have low equivalent series resistance (ESR), with a typical value of 10 μF, and a minimum value of 1 μF. The internal regulator is not designed to drive external loads.

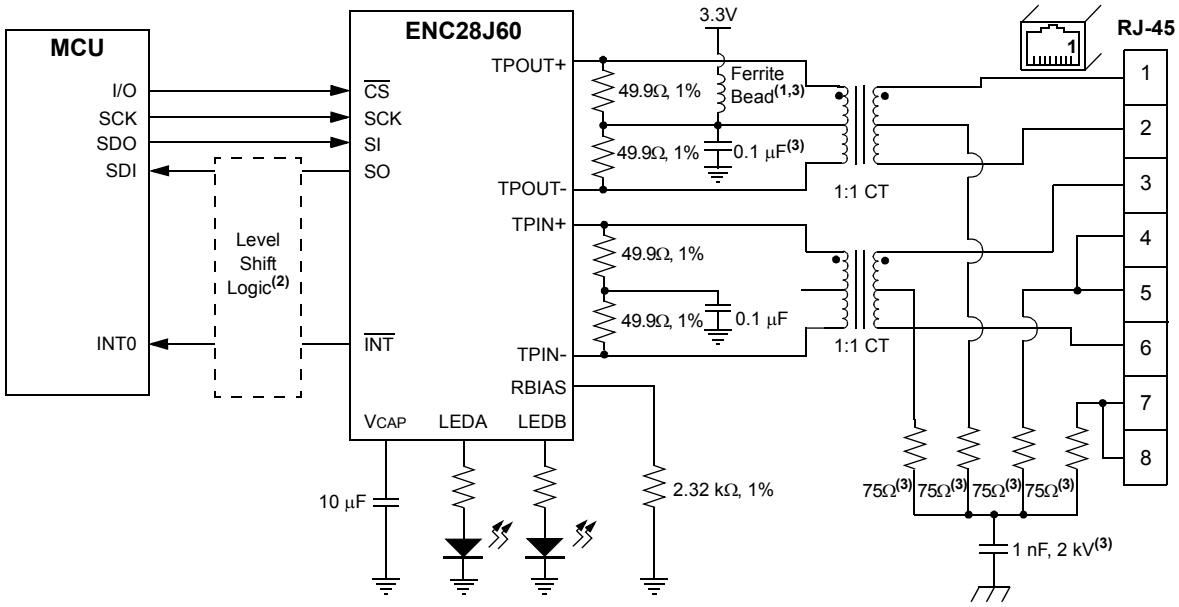
On the TPIN+/TPIN- and TPOUT+/TPOUT- pins, 1:1 center taped pulse transformers, rated for Ethernet operations, are required. When the Ethernet module is enabled, current is continually sunk through both TPOUT pins. When the PHY is actively transmitting, a differential voltage is created on the Ethernet cable by varying the relative current sunk by TPOUT+ compared to TPOUT-.

A common-mode choke on the TPOUT interface, placed between the TPOUT pins and the Ethernet transformer (not shown), is not recommended. If a common-mode choke is used to reduce EMI emissions, it should be placed between the Ethernet transformer and pins 1 and 2 of the RJ-45 connector. Many Ethernet transformer modules include common-mode chokes inside the same device package. The transformers should have at least the isolation rating specified in Table 16-5 to protect against static voltages and meet IEEE 802.3 isolation requirements (see **Section 16.0 "Electrical Characteristics"** for specific transformer requirements). Both transmit and receive interfaces additionally require two resistors and a capacitor to properly terminate the transmission line, minimizing signal reflections.

All power supply pins must be externally connected to the same power source. Similarly, all ground references must be externally connected to the same ground node. Each VDD and VSS pin pair should have a 0.1 μF ceramic bypass capacitor (not shown in the schematic) placed as close to the pins as possible.

Since relatively high currents are necessary to operate the twisted-pair interface, all wires should be kept as short as possible. Reasonable wire widths should be used on power wires to reduce resistive loss. If the differential data lines cannot be kept short, they should be routed in such a way as to have a 100Ω characteristic impedance.

FIGURE 2-4: ENC28J60 ETHERNET TERMINATION AND EXTERNAL CONNECTIONS



Note 1: Ferrite Bead should be rated for at least 80 mA.

2: Required only if the microcontroller is operating at 5V. See **Section 2.5 "I/O Levels"** for more information.

3: These components are installed for EMI reduction purposes.

2.5 I/O Levels

The ENC28J60 is a 3.3V part; however, it was designed to be easily integrated into 5V systems. The SPI $\overline{CS}$, SCK and SI inputs, as well as the $\overline{RESET}$ pin, are all 5V tolerant. On the other hand, if the host controller is operated at 5V, it quite likely will not be within specifications when its SPI and interrupt inputs are driven by the 3.3V CMOS outputs on the ENC28J60. A unidirectional level translator would be necessary.

An economical 74HCT08 (quad AND gate), 74ACT125 (quad 3-state buffer) or many other 5V CMOS chips with TTL level input buffers may be used to provide the necessary level shifting. The use of 3-state buffers permits easy integration into systems which share the SPI bus with other devices. Figure 2-5 and Figure 2-6 show example translation schemes.

FIGURE 2-5: LEVEL SHIFTING USING AND GATES

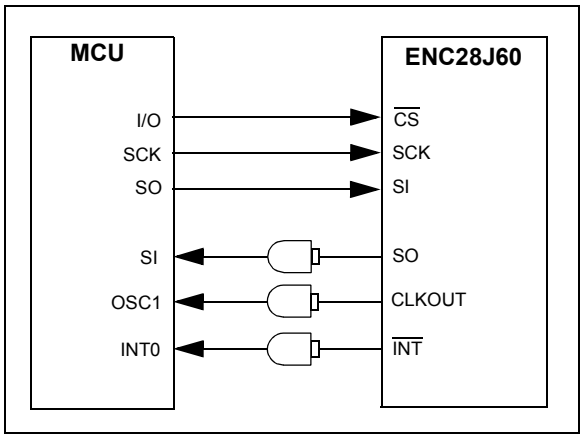
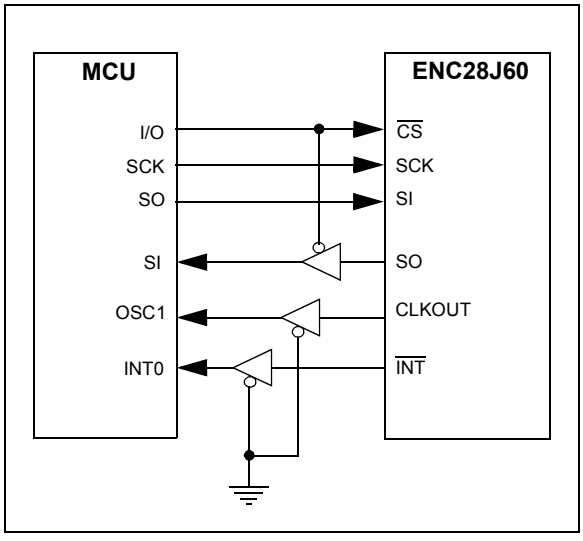


FIGURE 2-6: LEVEL SHIFTING USING 3-STATE BUFFERS

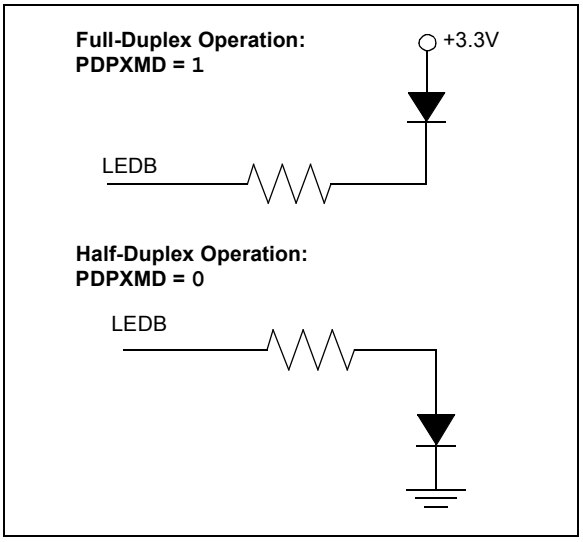


2.6 LED Configuration

The LEDA and LEDB pins support automatic polarity detection on Reset. The LEDs can be connected such that the pin must source current to turn the LED on, or alternately connected such that the pin must sink current to turn the LED on. Upon system Reset, the ENC28J60 will detect how the LED is connected and begin driving the LED to the default state configured by the PHLCON register. If the LED polarity is changed while the ENC28J60 is operating, the new polarity will not be detected until the next system Reset occurs.

LEDB is unique in that the connection of the LED is automatically read on Reset and determines how to initialize the PHCON1.PDPXMD bit. If the pin sources current to illuminate the LED, the bit is cleared on Reset and the PHY defaults to half-duplex operation. If the pin sinks current to illuminate the LED, the bit is set on Reset and the PHY defaults to full-duplex operation. Figure 2-7 shows the two available options. If no LED is attached to the LEDB pin, the PDPXMD bit will reset to an indeterminate value.

FIGURE 2-7: LEDB POLARITY AND RESET CONFIGURATION OPTIONS



The LEDs can also be configured separately to control their operating polarity (on or off when active), blink rate and blink stretch interval. The options are controlled by the LACFG<3:0> and LBCFG<3:0> bits. Typical values for blink stretch are listed in Table 2-1.

TABLE 2-1: LED BLINK STRETCH LENGTH

Stretch Length	Typical Stretch (ms)
TNSTRCH (normal)	40
TMSTRCH (medium)	70
TLSTRCH (long)	140

REGISTER 2-2: PHLCON: PHY MODULE LED CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
r	r	r	r	LACFG3	LACFG2	LACFG1	LACFG0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-x
LBCFG3	LBCFG2	LBCFG1	LBCFG0	LFRQ1	LFRQ0	STRCH	r
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Reserved:** Write as '0'

bit 13-12 **Reserved:** Write as '1'

bit 11-8 **LACFG<3:0>:** LEDA Configuration bits
1111 = Reserved
1110 = Display duplex status and collision activity (always stretched)
1101 = Display link status and transmit/receive activity (always stretched)
1100 = Display link status and receive activity (always stretched)
1011 = Blink slow
1010 = Blink fast
1001 = Off
1000 = On
0111 = Display transmit and receive activity (stretchable)
0110 = Reserved
0101 = Display duplex status
0100 = Display link status
0011 = Display collision activity (stretchable)
0010 = Display receive activity (stretchable)
0001 = Display transmit activity (stretchable)
0000 = Reserved

bit 7-4 **LBCFG<3:0>:** LEDB Configuration bits
1110 = Display duplex status and collision activity (always stretched)
1101 = Display link status and transmit/receive activity (always stretched)
1100 = Display link status and receive activity (always stretched)
1011 = Blink slow
1010 = Blink fast
1001 = Off
1000 = On
0111 = Display transmit and receive activity (stretchable)
0110 = Reserved
0101 = Display duplex status
0100 = Display link status
0011 = Display collision activity (stretchable)
0010 = Display receive activity (stretchable)
0001 = Display transmit activity (stretchable)
0000 = Reserved

bit 3-2 **LFRQ<1:0>:** LED Pulse Stretch Time Configuration bits (see Table 2-1)
11 = Reserved
10 = Stretch LED events by T_{LSTRCH}
01 = Stretch LED events by T_{MSTRCH}
00 = Stretch LED events by T_{NSTRCH}

bit 1 **STRCH:** LED Pulse Stretching Enable bit
1 = Stretchable LED events will cause lengthened LED pulses based on LFRQ<1:0> configuration
0 = Stretchable LED events will only be displayed while they are occurring

bit 0 **Reserved:** Write as '0'

NOTES:

3.0 MEMORY ORGANIZATION

All memory in the ENC28J60 is implemented as static RAM. There are three types of memory in the ENC28J60:

- Control Registers
- Ethernet Buffer
- PHY Registers

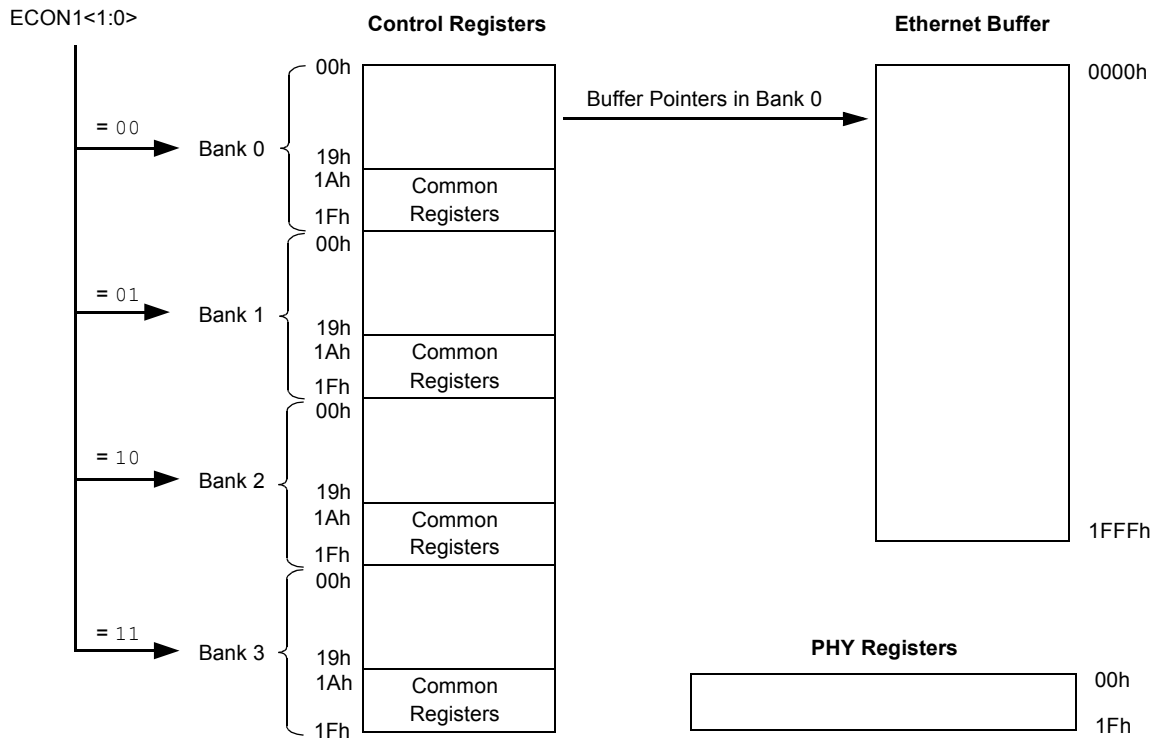
The Control registers' memory contains the registers that are used for configuration, control and status retrieval of the ENC28J60. The Control registers are directly read and written to by the SPI interface.

The Ethernet buffer contains transmit and receive memory used by the Ethernet controller in a single memory space. The sizes of the memory areas are programmable by the host controller using the SPI interface. The Ethernet buffer memory can only be accessed via the read buffer memory and write buffer memory SPI commands (see **Section 4.2.2 "Read Buffer Memory Command"** and **Section 4.2.4 "Write Buffer Memory Command"**).

The PHY registers are used for configuration, control and status retrieval of the PHY module. The registers are not directly accessible through the SPI interface; they can only be accessed through Media Independent Interface Management (MIIM) implemented in the MAC.

Figure 3-1 shows the data memory organization for the ENC28J60.

FIGURE 3-1: ENC28J60 MEMORY ORGANIZATION



Note: Memory areas are not shown to scale. The size of the control memory space has been scaled to show detail.

3.1 Control Registers

The Control registers provide the main interface between the host controller and the on-chip Ethernet controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

The Control register memory is partitioned into four banks, selectable by the bank select bits, BSEL<1:0>, in the ECON1 register. Each bank is 32 bytes long and addressed by a 5-bit address value.

The last five locations (1Bh to 1Fh) of all banks point to a common set of registers: EIE, EIR, ESTAT, ECON2 and ECON1. These are key registers used in controlling and monitoring the operation of the device. Their common mapping allows easy access without switching the bank. The ECON1 and ECON2 registers are discussed later in this section.

Some of the available addresses are unimplemented. Any attempts to write to these locations are ignored while reads return '0's. The register at address 1Ah in each bank is reserved; read and write operations should not be performed on this register. All other reserved registers may be read, but their contents must not be changed. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

Control registers for the ENC28J60 are generically grouped as ETH, MAC and MII registers. Register names starting with "E" belong to the ETH group. Similarly, registers names starting with "MA" belong to the MAC group and registers prefixed with "MI" belong to the MII group.

TABLE 3-1: ENC28J60 CONTROL REGISTER MAP

Bank 0 Address	Name	Bank 1 Address	Name	Bank 2 Address	Name	Bank 3 Address	Name
00h	ERDPTL	00h	EHT0	00h	MACON1	00h	MAADR5
01h	ERDPTH	01h	EHT1	01h	Reserved	01h	MAADR6
02h	EWRPTL	02h	EHT2	02h	MACON3	02h	MAADR3
03h	EWRPTH	03h	EHT3	03h	MACON4	03h	MAADR4
04h	ETXSTL	04h	EHT4	04h	MABBIPG	04h	MAADR1
05h	ETXSTH	05h	EHT5	05h	—	05h	MAADR2
06h	ETXNDL	06h	EHT6	06h	MAIPGL	06h	EBSTSD
07h	ETXNDH	07h	EHT7	07h	MAIPGH	07h	EBSTCON
08h	ERXSTL	08h	EPMM0	08h	MACLCON1	08h	EBSTCSL
09h	ERXSTH	09h	EPMM1	09h	MACLCON2	09h	EBSTCSH
0Ah	ERXNDL	0Ah	EPMM2	0Ah	MAMXFLL	0Ah	MISTAT
0Bh	ERXNDH	0Bh	EPMM3	0Bh	MAMXFLH	0Bh	—
0Ch	ERXRDPTL	0Ch	EPMM4	0Ch	Reserved	0Ch	—
0Dh	ERXRDPTH	0Dh	EPMM5	0Dh	Reserved	0Dh	—
0Eh	ERXWRPTL	0Eh	EPMM6	0Eh	Reserved	0Eh	—
0Fh	ERXWRPTH	0Fh	EPMM7	0Fh	—	0Fh	—
10h	EDMASTL	10h	EPMCSL	10h	Reserved	10h	—
11h	EDMASTH	11h	EPMCSH	11h	Reserved	11h	—
12h	EDMANDL	12h	—	12h	MICMD	12h	EREVID
13h	EDMANDH	13h	—	13h	—	13h	—
14h	EDMADSTL	14h	EPMOL	14h	MIREGADR	14h	—
15h	EDMADSTH	15h	EPMOH	15h	Reserved	15h	ECOCON
16h	EDMACSL	16h	Reserved	16h	MIWRL	16h	Reserved
17h	EDMACSH	17h	Reserved	17h	MIWRH	17h	EFLOCON
18h	—	18h	ERXFCON	18h	MIRDL	18h	EPAUSL
19h	—	19h	EPKTCNT	19h	MIRDH	19h	EPAUSH
1Ah	Reserved	1Ah	Reserved	1Ah	Reserved	1Ah	Reserved
1Bh	EIE	1Bh	EIE	1Bh	EIE	1Bh	EIE
1Ch	EIR	1Ch	EIR	1Ch	EIR	1Ch	EIR
1Dh	ESTAT	1Dh	ESTAT	1Dh	ESTAT	1Dh	ESTAT
1Eh	ECON2	1Eh	ECON2	1Eh	ECON2	1Eh	ECON2
1Fh	ECON1	1Fh	ECON1	1Fh	ECON1	1Fh	ECON1

TABLE 3-2: ENC28J60 CONTROL REGISTER SUMMARY

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset	Details on Page
EIE	INTIE	PKTIE	DMAIE	LINKIE	TXIE	r	TXERIE	RXERIE	0000 0000	65
EIR	—	PKTIF	DMAIF	LINKIF	TXIF	r	TXERIF	RXERIF	-000 0000	66
ESTAT	INT	BUFER	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY(1)	0000 -000	64
ECON2	AUTOINC	PKTDEC	PWRSV	r	VRPS	—	—	—	1000 0---	16
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	0000 0000	15
ERDPTL	Read Pointer Low Byte ERDPT<7:0>								1111 1010	17
ERDPTH	—	—	—	Read Pointer High Byte (ERDPT<12:8>)					---0 0101	17
EWRPTL	Write Pointer Low Byte (EWRPT<7:0>)								0000 0000	17
EWRPTH	—	—	—	Write Pointer High Byte (EWRPT<12:8>)					---0 0000	17
ETXSTL	TX Start Low Byte (ETXST<7:0>)								0000 0000	17
ETXSTH	—	—	—	TX Start High Byte (ETXST<12:8>)					---0 0000	17
ETXNDL	TX End Low Byte (ETXND<7:0>)								0000 0000	17
ETXNDH	—	—	—	TX End High Byte (ETXND<12:8>)					---0 0000	17
ERXSTL	RX Start Low Byte (ERXST<7:0>)								1111 1010	17
ERXSTH	—	—	—	RX Start High Byte (ERXST<12:8>)					---0 0101	17
ERXNDL	RX End Low Byte (ERXND<7:0>)								1111 1111	17
ERXNDH	—	—	—	RX End High Byte (ERXND<12:8>)					---1 1111	17
ERXRDPTL	RX RD Pointer Low Byte (ERXRDPT<7:0>)								1111 1010	17
ERXRDPTH	—	—	—	RX RD Pointer High Byte (ERXRDPT<12:8>)					---0 0101	17
ERXWRPTL	RX WR Pointer Low Byte (ERXWRPT<7:0>)								0000 0000	17
ERXWRPTH	—	—	—	RX WR Pointer High Byte (ERXWRPT<12:8>)					---0 0000	17
EDMASTL	DMA Start Low Byte (EDMAST<7:0>)								0000 0000	71
EDMASTH	—	—	—	DMA Start High Byte (EDMAST<12:8>)					---0 0000	71
EDMANDL	DMA End Low Byte (EDMAND<7:0>)								0000 0000	71
EDMANDH	—	—	—	DMA End High Byte (EDMAND<12:8>)					---0 0000	71
EDMADSTL	DMA Destination Low Byte (EDMADST<7:0>)								0000 0000	71
EDMADSTH	—	—	—	DMA Destination High Byte (EDMADST<12:8>)					---0 0000	71
EDMACSL	DMA Checksum Low Byte (EDMACS<7:0>)								0000 0000	72
EDMACSH	DMA Checksum High Byte (EDMACS<15:8>)								0000 0000	72
EHT0	Hash Table Byte 0 (EHT<7:0>)								0000 0000	52
EHT1	Hash Table Byte 1 (EHT<15:8>)								0000 0000	52
EHT2	Hash Table Byte 2 (EHT<23:16>)								0000 0000	52
EHT3	Hash Table Byte 3 (EHT<31:24>)								0000 0000	52
EHT4	Hash Table Byte 4 (EHT<39:32>)								0000 0000	52
EHT5	Hash Table Byte 5 (EHT<47:40>)								0000 0000	52
EHT6	Hash Table Byte 6 (EHT<55:48>)								0000 0000	52
EHT7	Hash Table Byte 7 (EHT<63:56>)								0000 0000	52
EPMM0	Pattern Match Mask Byte 0 (EPMM<7:0>)								0000 0000	51
EPMM1	Pattern Match Mask Byte 1 (EPMM<15:8>)								0000 0000	51
EPMM2	Pattern Match Mask Byte 2 (EPMM<23:16>)								0000 0000	51
EPMM3	Pattern Match Mask Byte 3 (EPMM<31:24>)								0000 0000	51
EPMM4	Pattern Match Mask Byte 4 (EPMM<39:32>)								0000 0000	51
EPMM5	Pattern Match Mask Byte 5 (EPMM<47:40>)								0000 0000	51
EPMM6	Pattern Match Mask Byte 6 (EPMM<55:48>)								0000 0000	51
EPMM7	Pattern Match Mask Byte 7 (EPMM<63:56>)								0000 0000	51

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify.

Note 1: CLKRDY resets to '0' on Power-on Reset but is unaffected on all other Resets.

2: EREVID is a read-only register.

3: ECOCON resets to '---- -100' on Power-on Reset and '---- -uuu' on all other Resets.

TABLE 3-2: ENC28J60 CONTROL REGISTER SUMMARY (CONTINUED)

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset	Details on Page
EPMCSL	Pattern Match Checksum Low Byte (EPMCS<7:0>)								0000 0000	51
EPMCSH	Pattern Match Checksum High Byte (EPMCS<15:0>)								0000 0000	51
EPMOL	Pattern Match Offset Low Byte (EPMO<7:0>)								0000 0000	51
EPMOH	—	—	—	Pattern Match Offset High Byte (EPMO<12:8>)					---0 0000	51
ERXFCON	UCEN	ANDOR	CRCEN	PMEN	MPEN	HTEN	MCEN	BCEN	1010 0001	48
EPKTCNT	Ethernet Packet Count								0000 0000	43
MACON1	—	—	—	r	TXPAUS	RXPAUS	PASSALL	MARXEN	---0 0000	34
MACON3	PADCFG2	PADCFG1	PADCFG0	TXCRCEN	PHDREN	HFRMEN	FRMLNEN	FULDPX	0000 0000	35
MACON4	—	DEFER	BPEN	NOBKOFF	—	—	r	r	-000 --00	36
MABBIPG	—	Back-to-Back Inter-Packet Gap (BBIPG<6:0>)							-000 0000	36
MAIPGL	—	Non-Back-to-Back Inter-Packet Gap Low Byte (MAIPGL<6:0>)							-000 0000	34
MAIPGH	—	Non-Back-to-Back Inter-Packet Gap High Byte (MAIPGH<6:0>)							-000 0000	34
MACLCON1	—	—	—	—	Retransmission Maximum (RETMAX<3:0>)				---- 1111	34
MACLCON2	—	—	Collision Window (COLWIN<5:0>)						--11 0111	34
MAMXFLL	Maximum Frame Length Low Byte (MAMXFL<7:0>)								0000 0000	34
MAMXFLH	Maximum Frame Length High Byte (MAMXFL<15:8>)								0000 0110	34
MICMD	—	—	—	—	—	—	MIISCAN	MIIRD	---- --00	21
MIREGADR	—	—	—	MII Register Address (MIREGADR<4:0>)					---0 0000	19
MIWRL	MII Write Data Low Byte (MIWR<7:0>)								0000 0000	19
MIWRH	MII Write Data High Byte (MIWR<15:8>)								0000 0000	19
MIRDL	MII Read Data Low Byte (MIRD<7:0>)								0000 0000	19
MIRDH	MII Read Data High Byte(MIRD<15:8>)								0000 0000	19
MAADR5	MAC Address Byte 5 (MAADR<15:8>)								0000 0000	34
MAADR6	MAC Address Byte 6 (MAADR<7:0>)								0000 0000	34
MAADR3	MAC Address Byte 3 (MAADR<31:24>), OUI Byte 3								0000 0000	34
MAADR4	MAC Address Byte 4 (MAADR<23:16>)								0000 0000	34
MAADR1	MAC Address Byte 1 (MAADR<47:40>), OUI Byte 1								0000 0000	34
MAADR2	MAC Address Byte 2 (MAADR<39:32>), OUI Byte 2								0000 0000	34
EBSTSD	Built-in Self-Test Fill Seed (EBSTSD<7:0>)								0000 0000	76
EBSTCON	PSV2	PSV1	PSV0	PSEL	TMSEL1	TMSEL0	TME	BISTST	0000 0000	75
EBSTCSL	Built-in Self-Test Checksum Low Byte (EBSTCS<7:0>)								0000 0000	76
EBSTCSH	Built-in Self-Test Checksum High Byte (EBSTCS<15:8>)								0000 0000	76
MISTAT	—	—	—	—	r	NVALID	SCAN	BUSY	---- 0000	21
EREVID(2)	—	—	—	Ethernet Revision ID (EREVID<4:0>)					---q qqqq	22
ECOCON(3)	—	—	—	—	—	COCON2	COCON1	COCON0	---- -100	6
EFLOCON	—	—	—	—	—	FULDPXS	FCEN1	FCEN0	---- -000	56
EPAUSL	Pause Timer Value Low Byte (EPAUS<7:0>)								0000 0000	57
EPAUSH	Pause Timer Value High Byte (EPAUS<15:8>)								0001 0000	57

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify.

Note 1: CLKRDY resets to '0' on Power-on Reset but is unaffected on all other Resets.

2: EREVID is a read-only register.

3: ECOCON resets to '---- -100' on Power-on Reset and '---- -uuu' on all other Resets.

3.1.1 ECON1 REGISTER

The ECON1 register, shown in Register 3-1, is used to control the main functions of the ENC28J60. Receive enable, transmit request, DMA control and bank select bits can all be found in ECON1.

REGISTER 3-1: ECON1: ETHERNET CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TXRST:** Transmit Logic Reset bit
1 = Transmit logic is held in Reset
0 = Normal operation

bit 6 **RXRST:** Receive Logic Reset bit
1 = Receive logic is held in Reset
0 = Normal operations

bit 5 **DMAST:** DMA Start and Busy Status bit
1 = DMA copy or checksum operation is in progress
0 = DMA hardware is Idle

bit 4 **CSUMEN:** DMA Checksum Enable bit
1 = DMA hardware calculates checksums
0 = DMA hardware copies buffer memory

bit 3 **TXRTS:** Transmit Request to Send bit
1 = The transmit logic is attempting to transmit a packet
0 = The transmit logic is Idle

bit 2 **RXEN:** Receive Enable bit
1 = Packets which pass the current filter configuration will be written into the receive buffer
0 = All packets received will be ignored

bit 1-0 **BSEL<1:0>:** Bank Select bits
11 = SPI accesses registers in Bank 3
10 = SPI accesses registers in Bank 2
01 = SPI accesses registers in Bank 1
00 = SPI accesses registers in Bank 0

3.1.2 ECON2 REGISTER

The ECON2 register, shown in Register 3-2, is used to control other main functions of the ENC28J60.

REGISTER 3-2: ECON2: ETHERNET CONTROL REGISTER 2

R/W-1	R/W-0(1)	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
AUTOINC	PKTDEC	PWRSV	r	VRPS	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **AUTOINC:** Automatic Buffer Pointer Increment Enable bit
1 = Automatically increment ERDPT or EWRPT on reading from or writing to EDATA
0 = Do not automatically change ERDPT and EWRPT after the buffer is accessed

bit 6 **PKTDEC:** Packet Decrement bit(1)
1 = Decrement the EPKTCNT register by one
0 = Leave EPKTCNT unchanged

bit 5 **PWRSV:** Power Save Enable bit
1 = MAC, PHY and control logic are in Low-Power Sleep mode
0 = Normal operation

bit 4 **Reserved:** Maintain as '0'

bit 3 **VRPS:** Voltage Regulator Power Save Enable bit
When PWRSV = 1:
1 = Internal voltage regulator is in Low-Current mode
0 = Internal voltage regulator is in Normal Current mode
When PWRSV = 0:
The bit is ignored; the regulator always outputs as much current as the device requires.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared once it is set.

3.2 Ethernet Buffer

The Ethernet buffer contains transmit and receive memory used by the Ethernet controller. The entire buffer is 8 Kbytes, divided into separate receive and transmit buffer spaces. The sizes and locations of transmit and receive memory are fully programmable by the host controller using the SPI interface.

The relationship of the buffer spaces is shown in Figure 3-2.

3.2.1 RECEIVE BUFFER

The receive buffer constitutes a circular FIFO buffer managed by hardware. The register pairs, ERXSTH:ERXSTL and ERXNDH:ERXNDL, serve as pointers to define the buffer's size and location within the memory. The byte pointed to by ERXST and the byte pointed to by ERXND are both included in the FIFO buffer.

As bytes of data are received from the Ethernet interface, they are written into the receive buffer sequentially. However, after the memory pointed to by ERXND is written to, the hardware will automatically write the next byte of received data to the memory pointed to by ERXST. As a result, the receive hardware will never write outside the boundaries of the FIFO.

The host controller may program the ERXST and ERXND Pointers when the receive logic is not enabled. The pointers must not be modified while the receive logic is enabled (ECON1.RXEN is set). If desired, the Pointers may span the 1FFFh to 0000h memory boundary; the hardware will still operate as a FIFO.

The ERXWRPTH:ERXWRPTL registers define a location within the FIFO where the hardware will write bytes that it receives. The pointer is read-only and is automatically updated by the hardware whenever a new packet is successfully received. The pointer is useful for determining how much free space is available within the FIFO.

The ERXRDPT registers define a location within the FIFO where the receive hardware is forbidden to write to. In normal operation, the receive hardware will write data up to, but not including, the memory pointed to by ERXRDPT. If the FIFO fills up with data and new data continues to arrive, the hardware will not overwrite the previously received data. Instead, the new data will be thrown away and the old data will be preserved. In order to continuously receive new data, the host controller must periodically advance this pointer whenever it finishes processing some, or all, of the old received data.

3.2.2 TRANSMIT BUFFER

Any space within the 8-Kbyte memory, which is not programmed as part of the receive FIFO buffer, is considered to be the transmit buffer. The responsibility of managing where packets are located in the transmit buffer belongs to the host controller. Whenever the host controller decides to transmit a packet, the ETXST and ETXND Pointers are programmed with addresses specifying where, within the transmit buffer, the particular packet to transmit is located. The hardware does not check that the start and end addresses do not overlap with the receive buffer. To prevent buffer corruption, the host controller must make sure to not transmit a packet while the ETXST and ETXND Pointers are overlapping the receive buffer, or while the ETXND Pointer is too close to the receive buffer. See **Section 7.1 "Transmitting Packets"** for more information.

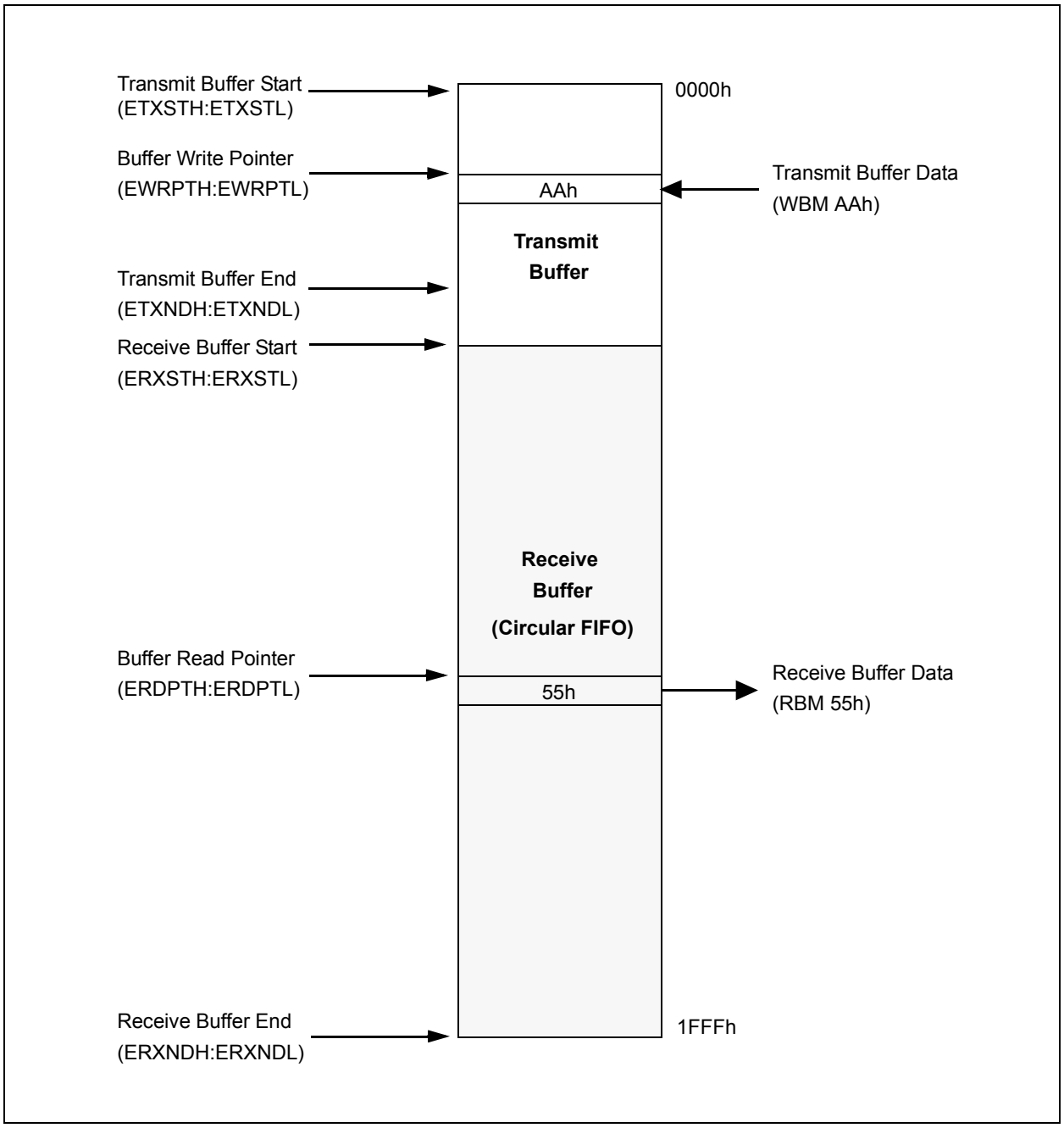
3.2.3 READING AND WRITING TO THE BUFFER

The Ethernet buffer contents are accessed from the host controller though separate Read and Write Pointers (ERDPT and EWRPT) combined with the read buffer memory and write buffer memory SPI commands. While sequentially reading from the receive buffer, a wrapping condition will occur at the end of the receive buffer. While sequentially writing to the buffer, no wrapping conditions will occur. See **Section 4.2.2 "Read Buffer Memory Command"** and **Section 4.2.4 "Write Buffer Memory Command"** for more information.

3.2.4 DMA ACCESS TO THE BUFFER

The integrated DMA controller must read from the buffer when calculating a checksum and it must read and write to the buffer when copying memory. The DMA follows the same wrapping rules that SPI accesses do. While it sequentially reads, it will be subject to a wrapping condition at the end of the receive buffer. All writes it does will not be subject to any wrapping conditions. See **Section 13.0 "Direct Memory Access Controller"** for more information.

FIGURE 3-2: ETHERNET BUFFER ORGANIZATION



3.3 PHY Registers

The PHY registers provide configuration and control of the PHY module, as well as status information about its operation. All PHY registers are 16 bits in width. There are a total of 32 PHY addresses; however, only 9 locations are implemented. Writes to unimplemented locations are ignored and any attempts to read these locations will return '0'. All reserved locations should be written as '0'; their contents should be ignored when read.

Unlike the ETH, MAC and MII control registers, or the buffer memory, the PHY registers are not directly accessible through the SPI control interface. Instead, access is accomplished through a special set of MAC control registers that implement Media Independent Interface Management (MIIM). These control registers are referred to as the MII registers. The registers that control access to the PHY registers are shown in Register 3-3 and Register 3-4.

3.3.1 READING PHY REGISTERS

When a PHY register is read, the entire 16 bits are obtained.

To read from a PHY register:

1. Write the address of the PHY register to read from into the MIREGADR register.
2. Set the MICMD.MIIRD bit. The read operation begins and the MISTAT.BUSY bit is set.
3. Wait 10.24 μs. Poll the MISTAT.BUSY bit to be certain that the operation is complete. While busy, the host controller should not start any MIISCAN operations or write to the MIWRH register.
   When the MAC has obtained the register contents, the BUSY bit will clear itself.
4. Clear the MICMD.MIIRD bit.
5. Read the desired data from the MIRDL and MIRDH registers. The order that these bytes are accessed is unimportant.

3.3.2 WRITING PHY REGISTERS

When a PHY register is written to, the entire 16 bits is written at once; selective bit writes are not implemented. If it is necessary to reprogram only select bits in the register, the controller must first read the PHY register, modify the resulting data and then write the data back to the PHY register.

To write to a PHY register:

1. Write the address of the PHY register to write to into the MIREGADR register.
2. Write the lower 8 bits of data to write into the MIWRL register.
3. Write the upper 8 bits of data to write into the MIWRH register. Writing to this register automatically begins the MIIM transaction, so it must be written to after MIWRL. The MISTAT.BUSY bit becomes set.

The PHY register will be written after the MIIM operation completes, which takes 10.24 μs. When the write operation has completed, the BUSY bit will clear itself. The host controller should not start any MIISCAN or MIIRD operations while busy.

3.3.3 SCANNING A PHY REGISTER

The MAC can be configured to perform automatic back-to-back read operations on a PHY register. This can significantly reduce the host controller complexity when periodic status information updates are desired. To perform the scan operation:

1. Write the address of the PHY register to read from into the MIREGADR register.
2. Set the MICMD.MIISCAN bit. The scan operation begins and the MISTAT.BUSY bit is set. The first read operation will complete after 10.24 μs. Subsequent reads will be done at the same interval until the operation is cancelled. The MISTAT.NVALID bit may be polled to determine when the first read operation is complete.

After setting the MIISCAN bit, the MIRDL and MIRDH registers will automatically be updated every 10.24 μs. There is no status information which can be used to determine when the MIRD registers are updated. Since the host controller can only read one MII register at a time through the SPI, it must not be assumed that the values of MIRDL and MIRDH were read from the PHY at exactly the same time.

When the MIISCAN operation is in progress, the host controller must not attempt to write to MIWRH or start an MIIRD operation. The MIISCAN operation can be cancelled by clearing the MICMD.MIISCAN bit and then polling the MISTAT.BUSY bit. New operations may be started after the BUSY bit is cleared.

TABLE 3-3: ENC28J60 PHY REGISTER SUMMARY

Addr	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
00h	PHCON1	PRST	PLOOPBK	—	—	PPWRSV	r	—	PDPXMD(1)	r	—	—	—	—	—	—	—	00-- 00-q 0--- ----
01h	PHSTAT1	—	—	—	PFDPX	PHDPX	—	—	—	—	—	—	—	—	LLSTAT	JBSTAT	—	---1 1--- ---- -00-
02h	PHID1	PHY Identifier (OUI3:OUI18) = 0083h																0000 0000 1000 0011
03h	PHID2	PHY Identifier (OUI19:OUI24) = 000101						PHY P/N (PPN<5:0>) = 00h						PHY Revision (PREV<3:0>) = 00h				0001 0100 0000 0000
10h	PHCON2	—	FRCLNK	TXDIS	r	r	JABBER	r	HDLDIS	r	r	r	r	r	r	r	r	-000 0000 0000 0000
11h	PHSTAT2	—	—	TXSTAT	RXSTAT	COLSTAT	LSTAT	DPXSTAT(1)	—	—	—	PLRITY	—	—	—	—	—	--00 00q- --0- ----
12h	PHIE	r	r	r	r	r	r	r	r	r	r	r	PLNKIE	r	r	PGEIE	r	0000 0000 0000 0000
13h	PHIR	r	r	r	r	r	r	r	r	r	r	r	PLNKIF	r	PGIF	r	r	xxxx xxxx xx00 00x0
14h	PHLCON	r	r	r	r	LACFG3	LACFG2	LACFG1	LACFG0	LBCFG3	LBCFG2	LBCFG1	LBCFG0	LFRQ1	LFRQ0	STRCH	r	0011 0100 0010 001x

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved, do not modify.

Note 1: Reset values of the Duplex mode/status bits depend on the connection of the LED to the LEDB pin (see **Section 2.6 "LED Configuration"** for additional details).

REGISTER 3-3: MICMD: MII COMMAND REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	MIISCAN	MIIRD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **MIISCAN:** MII Scan Enable bit
1 = PHY register at MIREGADR is continuously read and the data is placed in MIRD
0 = No MII Management scan operation is in progress

bit 0 **MIIRD:** MII Read Enable bit
1 = PHY register at MIREGADR is read once and the data is placed in MIRD
0 = No MII Management read operation is in progress

REGISTER 3-4: MISTAT: MII STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	r	NVALID	SCAN	BUSY
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **Reserved:** Maintain as '0'

bit 2 **NVALID:** MII Management Read Data Not Valid bit
1 = The contents of MIRD are not valid yet
0 = The MII Management read cycle has completed and MIRD has been updated

bit 1 **SCAN:** MII Management Scan Operation bit
1 = MII Management scan operation is in progress
0 = No MII Management scan operation is in progress

bit 0 **BUSY:** MII Management Busy bit
1 = A PHY register is currently being read or written to
0 = The MII Management interface is Idle

3.3.4 PHSTAT REGISTERS

The PHSTAT1 and PHSTAT2 registers contain read-only bits that show the current status of the PHY module's operations, particularly the conditions of the communications link to the rest of the network.

The PHSTAT1 register (Register 3-5) contains the LLSTAT bit; it clears and latches low if the physical layer link has gone down since the last read of the register. Periodic polling by the host controller can be used to determine exactly when the link fails. It may be particularly useful if the link change interrupt is not used.

The PHSTAT1 register also contains a jabber status bit. An Ethernet controller is said to be "jabbering" if it continuously transmits data without stopping and allowing other nodes to share the medium. Generally, the jabber condition indicates that the local controller may be grossly violating the maximum packet size defined by the IEEE specification. This bit latches high to indicate that a jabber condition has occurred since the last read of the register.

The PHSTAT2 register (Register 3-6) contains status bits which report if the PHY module is linked to the network and whether or not it is transmitting or receiving.

3.3.5 PHID1 AND PHID2 REGISTERS

The PHID1 and PHID2 registers are read-only registers. They hold constant data that helps identify the Ethernet controller and may be useful for debugging purposes. This includes:

- The part number of the PHY module (PPN5:PPN0)
- The revision level of the PHY module (PREV3:PREV0); and
- The PHY identifier, as part of Microchip's corporate Organizationally Unique Identifier (OUI) (OUI3:OUI24)

The PHY part number and revision are part of PHID2. The upper two bytes of the PHY identifier are located in PHID1, with the remainder in PHID2. The exact locations within registers are shown in Table 3-3.

The 22 bits of the OUI contained in the PHY Identifier (OUI3:OUI24, corresponding to PHID1<15:0> and PHID2<15:10>) are concatenated with '00' as the first two digits (OUI1 and OUI2) to generate the entire OUI. For convenience, this 24-bit string is usually interpreted in hexadecimal; the resulting OUI for Microchip Technology is 0004A3h.

Revision information is also stored in EREVID. This is a read-only control register which contains a 5-bit identifier for the specific silicon revision level of the device. Details of this register are shown in Table 3-2.

REGISTER 3-5: PHSTAT1: PHYSICAL LAYER STATUS REGISTER 1

U-0	U-0	U-0	R-1	R-1	U-0	U-0	U-0
—	—	—	PFDPX	PHDPX	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/LL-0	R/LH-0	U-0
—	—	—	—	—	LLSTAT	JBSTAT	—
bit 7							bit 0

Legend:	1 = Bit is set		
R = Read-only bit	0 = Bit is cleared	U = Unimplemented bit, read as '0'	
-n = Value at POR	R/LH = Read-only latch bit	R/LL = Bit latches low	LH = Bit latches high

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **PFDPX:** PHY Full-Duplex Capable bit
1 = PHY is capable of operating at 10 Mbps in Full-Duplex mode (this bit is always set)

bit 11 **PHDPX:** PHY Half-Duplex Capable bit
1 = PHY is capable of operating at 10 Mbps in Half-Duplex mode (this bit is always set)

bit 10-3 **Unimplemented:** Read as '0'

bit 2 **LLSTAT:** PHY Latching Link Status bit
1 = Link is up and has been up continously since PHSTAT1 was last read
0 = Link is down or was down for a period since PHSTAT1 was last read

bit 1 **JBSTAT:** PHY Latching Jabber Status bit
1 = PHY has detected a transmission meeting the jabber criteria since PHSTAT1 was last read
0 = PHY has not detected any jabbering transmissions since PHSTAT1 was last read

bit 0 **Unimplemented:** Read as '0'

REGISTER 3-6: PHSTAT2: PHYSICAL LAYER STATUS REGISTER 2

U-0	U-0	R-0	R-0	R-0	R-0	R-x	U-0
—	—	TXSTAT	RXSTAT	COLSTAT	LSTAT	DPXSTAT(1)	—
bit 15							bit 8

U-0	U-0	R-0	U-0	U-0	U-0	U-0	U-0
—	—	PLRITY	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **TXSTAT:** PHY Transmit Status bit
1 = PHY is transmitting data
0 = PHY is not transmitting data

bit 12 **RXSTAT:** PHY Receive Status bit
1 = PHY is receiving data
0 = PHY is not receiving data

bit 11 **COLSTAT:** PHY Collision Status bit
1 = A collision is occuring
0 = A collision is not occuring

bit 10 **LSTAT:** PHY Link Status bit (non-latching)
1 = Link is up
0 = Link is down

bit 9 **DPXSTAT:** PHY Duplex Status bit(1)
1 = PHY is configured for full-duplex operation (PHCON1<8> is set)
0 = PHY is configured for half-duplex operation (PHCON1<8> is clear)

bit 8-6 **Unimplemented:** Read as '0'

bit 5 **PLRITY:** Polarity Status bit
1 = The polarity of the signal on TPIN+/TPIN- is reversed
0 = The polarity of the signal on TPIN+/TPIN- is correct

bit 4-0 **Unimplemented:** Read as '0'

Note 1: Reset values of the Duplex mode/status bit depends on the connection of the LED to the LEDB pin (see **Section 2.6 "LED Configuration"** for additional details).

4.0 SERIAL PERIPHERAL INTERFACE (SPI)

4.1 Overview

The ENC28J60 is designed to interface directly with the Serial Peripheral Interface (SPI) port available on many microcontrollers. The implementation used on this device supports SPI mode 0,0 only. In addition, the SPI port requires that SCK be at Idle in a low state; selectable clock polarity is not supported.

Commands and data are sent to the device via the SI pin, with data being clocked in on the rising edge of SCK. Data is driven out by the ENC28J60 on the SO line, on the falling edge of SCK. The $\overline{CS}$ pin must be held low while any operation is performed and returned high when finished.

FIGURE 4-1: SPI INPUT TIMING

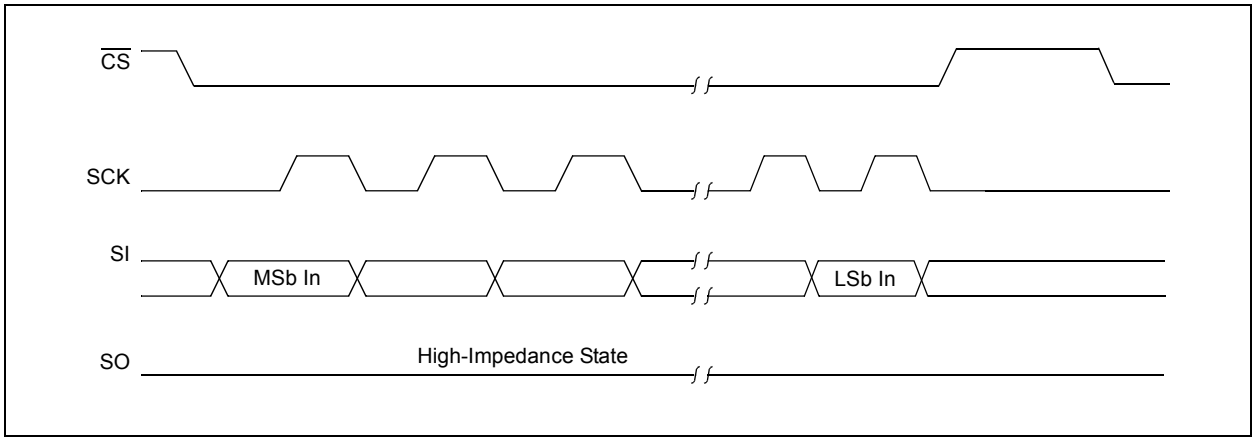


FIGURE 4-2: SPI OUTPUT TIMING