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ENC424J600/624J600

Data Sheet

Stand-Alone 10/100 Ethernet Controller
with SPI or Parallel Interface

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ENC424J600/624J600

Stand-Alone 10/100 Ethernet Controller with SPI or Parallel Interface

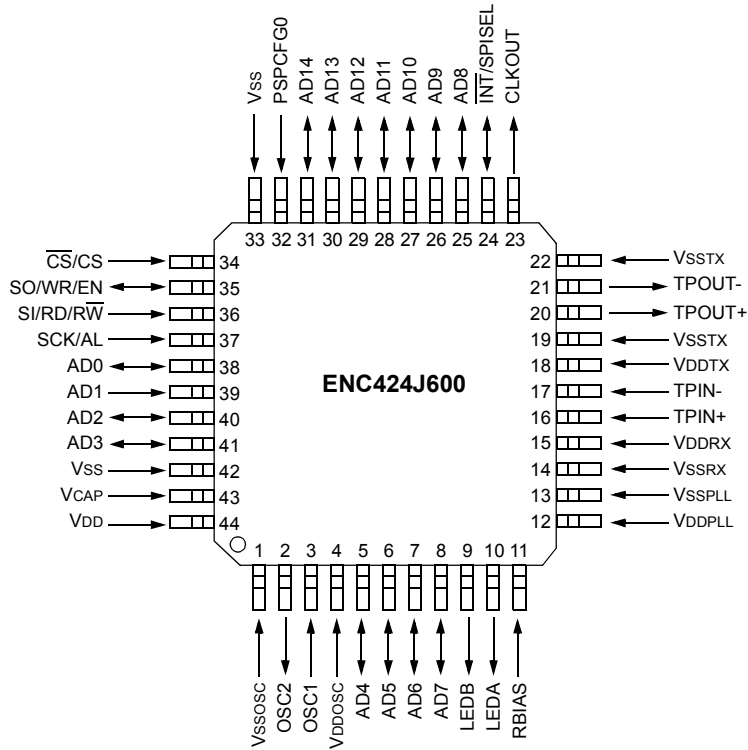
- IEEE 802.3™ Compliant Fast Ethernet Controller
- Integrated MAC and 10/100Base-T PHY
- Hardware Security Acceleration Engines
- 24-Kbyte Transmit/Receive Packet Buffer SRAM
- Supports one 10/100Base-T Port with Automatic Polarity Detection and Correction
- Supports Auto-Negotiation
- Support for Pause Control Frames, including Automatic Transmit and Receive Flow Control
- Supports Half and Full-Duplex Operation
- Programmable Automatic Retransmit on Collision
- Programmable Padding and CRC Generation
- Programmable Automatic Rejection of Erroneous and Runt Packets
- Factory Preprogrammed Unique MAC Address
- MAC:
 - Support for Unicast, Multicast and Broadcast packets
 - Supports promiscuous reception
 - Programmable pattern matching
 - Programmable filtering on multiple packet formats, including Magic Packet™, Unicast, Multicast, Broadcast, specific packet match, destination address hash match or any packet
- PHY:
 - Wave shaping output filter
 - Internal Loopback mode
 - Energy Detect Power-Down mode
- Available MCU Interfaces:
 - 14 Mbit/s SPI interface with enhanced set of opcodes (44-pin and 64-pin packages)
 - 8-bit multiplexed parallel interface (44-pin and 64-pin packages)
 - 8-bit or 16-bit multiplexed or demultiplexed parallel interface (64-pin package only)
- Security Engines:
 - High-performance, modular exponentiation engine with up to 1024-bit operands
 - Supports RSA® and Diffie-Hellman key exchange algorithms
 - High-performance AES encrypt/decrypt engine with 128-bit, 192-bit or 256-bit key
 - Hardware AES ECB, CBC, CFB and OFB mode capability
 - Software AES CTR mode capability
 - Fast MD5 hash computations
 - Fast SHA-1 hash computations
- Buffer:
 - Configurable transmit/receive buffer size
 - Hardware-managed circular receive FIFO
 - 8-bit or 16-bit random and sequential access
 - High-performance internal DMA for fast memory copying
 - High-performance hardware IP checksum calculations
 - Accessible in low-power modes
 - Space can be reserved for general purpose application usage in addition to transmit and receive packets
- Operational:
 - Outputs for two LED indicators with support for single and dual LED configurations
 - Transmit and receive interrupts
 - 25 MHz clock
 - 5V tolerant inputs
 - Clock out pin with programmable frequencies from 50 kHz to 33.3 MHz
 - Operating voltage range of 3.0V to 3.6V
 - Temperature range: -40°C to +85°C industrial
- Available in 44-Pin (TQFP and QFN) and 64-Pin TQFP Packages

Device	SRAM (bytes)	Pin Count	Speed (Mbps)	Security			SPI	PSP			
				ModEx 1024-Bit	MD5 SHA-1	AES 256-Bit		Multiplexed		Demultiplexed	
								8-Bit	16-Bit	8-Bit	16-Bit
ENC424J600	24K	44	10/100	Y	Y	Y	Y	N	N	N	
ENC624J600	24K	64	10/100	Y	Y	Y	Y	Y	Y	Y	

ENC424J600/624J600

Pin Diagrams

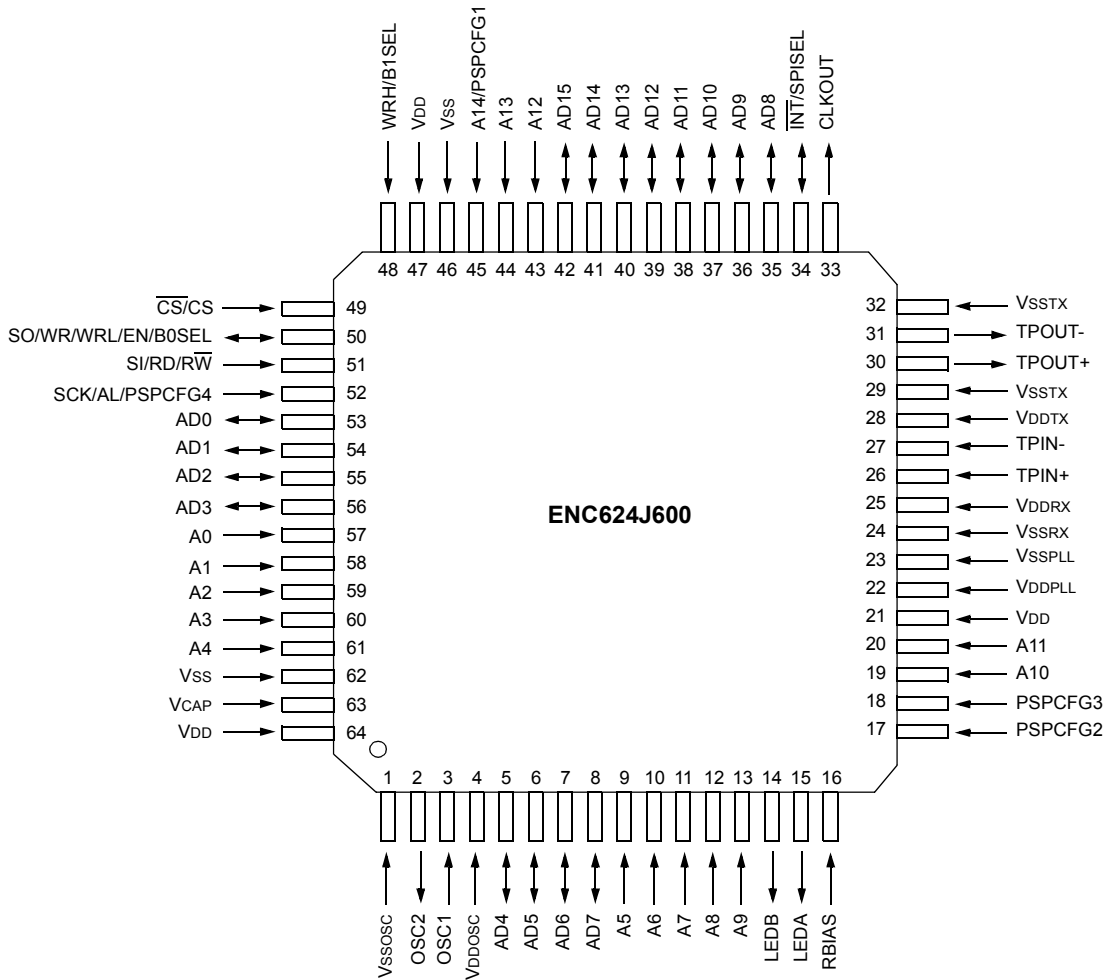
44-Pin TQFP and QFN



ENC424J600/624J600

Pin Diagrams (Continued)

64-Pin TQFP



ENC424J600/624J600

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ENC424J600/624J600

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- ENC424J600
- ENC624J600

The ENC424J600 and ENC624J600 are stand-alone, Fast Ethernet controllers with an industry standard Serial Peripheral Interface (SPI) or a flexible parallel interface. They are designed to serve as an Ethernet network interface for any microcontroller equipped with SPI or a standard parallel port.

ENC424J600/624J600 devices meet all of the IEEE 802.3 specifications applicable to 10Base-T and 100Base-TX Ethernet, including many optional clauses, such as auto-negotiation. They incorporate a number of packet filtering schemes to limit incoming packets. They also provide an internal, 16-bit wide DMA for fast data throughput and support for hardware IP checksum calculations.

For applications that require the security and authentication features of SSL, TLS and other protocols related to cryptography, a block of security engines is provided. The engines perform RSA, Diffie-Hellman, AES, MD5 and SHA-1 algorithm computations, allowing reduced code size, faster connection establishment and throughput, and reduced firmware development effort.

Communication with the microcontroller is implemented via the SPI or parallel interface, with data rates ranging from 14 Mbit/s (SPI) to 160 Mbit/s (demultiplexed, 16-bit parallel interface). Dedicated pins are used for LED link and activity indication and for transmit/receive/DMA interrupts.

A generous 24-Kbyte on-chip RAM buffer is available for TX and RX operations. It may also be used by the host microcontroller for general purpose storage. Communication protocols, such as TCP, can use this memory for saving data which may need to be retransmitted.

For easy end product manufacturability, each ENC624J600 family device is preprogrammed with a unique nonvolatile MAC address. In most cases, this allows the end device to avoid a serialized programming step.

The only functional difference between the ENC424J600 (44-pin) and ENC624J600 (64-pin) devices are the number of parallel interface options they support. These differences, along with a summary of their common features, are provided in Table 1-1. A general block diagram for the devices is shown in Figure 1-1.

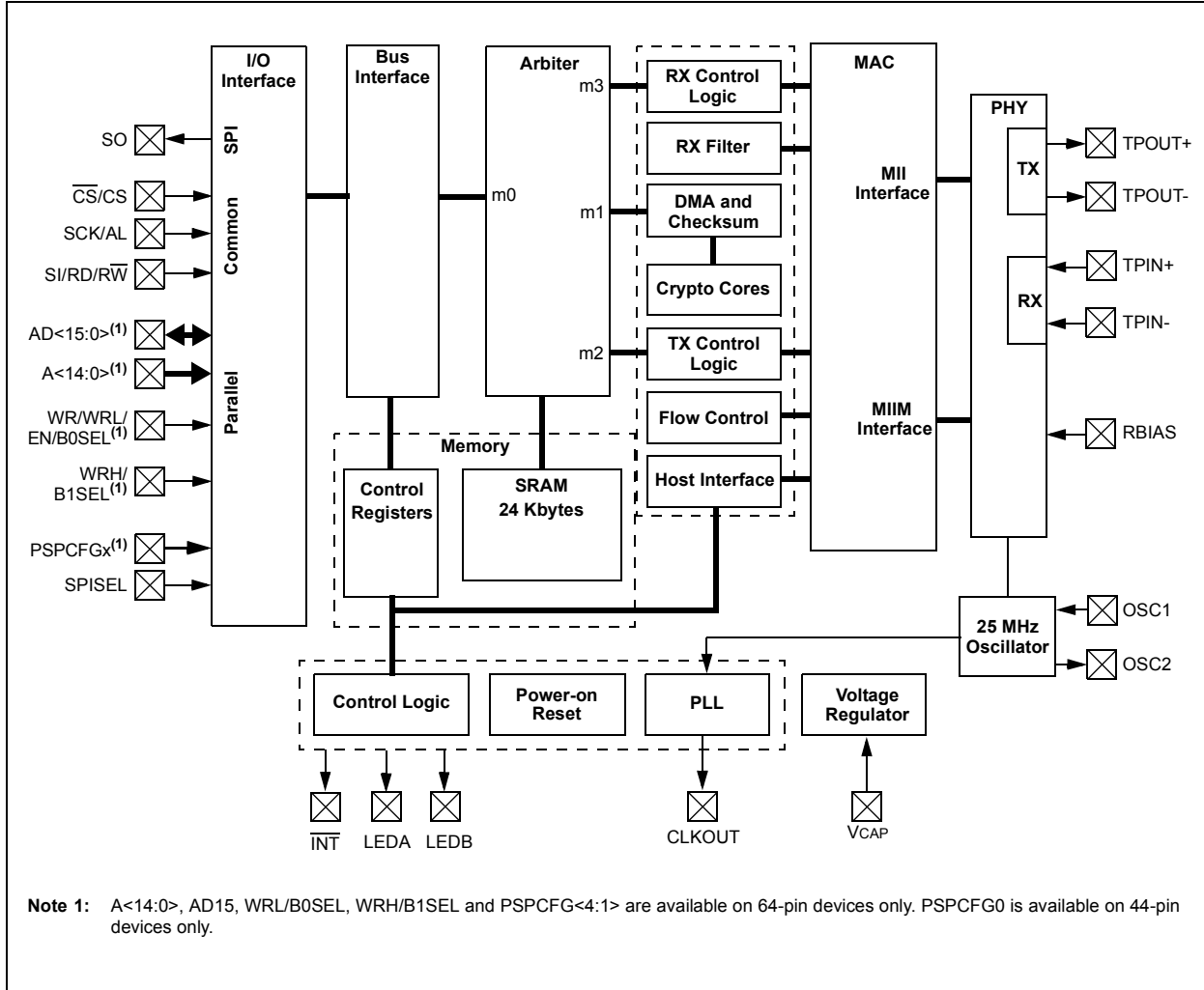
A list of the pin features, sorted by function, is presented in Table 1-2.

TABLE 1-1: DEVICE FEATURES FOR ENC424J600/624J600

Feature	ENC424J600	ENC624J600
Pin Count	44	64
Ethernet Operating Speed	10/100 Mbps (auto-negotiate, auto-sense or manual)	
Ethernet Duplex Modes	Half and Full (auto-negotiate and manual)	
Ethernet Flow Control	Pause and Backpressure (auto and manual)	
Buffer Memory (bytes)	24K (organized as 12K word x 16)	
Internal Interrupt Sources	11 (mappable to a single external interrupt flag)	
Serial Host Interface (SPI)	Yes	Yes
Parallel Host Interface:		
Operating modes	2	8
Multiplexed, 8-bit	Yes	Yes
16-bit	No	Yes
Demultiplexed, 8-bit	No	Yes
16-bit	No	Yes
Cryptographic Security Options:		
AES, 128/192/256-bit	Yes	Yes
MD5/SHA-1	Yes	Yes
Modular Exponentiation, 1024-bit	Yes	Yes
Receive Filter Options	Accept or reject packets with CRC match/mismatch, runt error collect or reject, Unicast, Not-Me Unicast, Multicast, Broadcast, Magic Packet™, Pattern Table and Hash Table	
Packages	44-Pin TQFP, QFN	64-Pin TQFP

ENC424J600/624J600

FIGURE 1-1: ENC424J600/624J600 BLOCK DIAGRAM



ENC424J600/624J600

TABLE 1-2: ENC424J600/624J600 PINOUT DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Input Buffer	Description
	44-Pin	64-Pin			
AD0	38	53	I/O	CMOS	PSP Multiplexed Address Input and/or Bidirectional Data Bus
AD1	39	54	I/O	CMOS	
AD2	40	55	I/O	CMOS	
AD3	41	56	I/O	CMOS	
AD4	5	5	I/O	CMOS	
AD5	6	6	I/O	CMOS	
AD6	7	7	I/O	CMOS	
AD7	8	8	I/O	CMOS	
AD8	25	35	I/O	CMOS	
AD9	26	36	I/O	CMOS	
AD10	27	37	I/O	CMOS	
AD11	28	38	I/O	CMOS	
AD12	29	39	I/O	CMOS	
AD13	30	40	I/O	CMOS	
AD14	31	41	I/O	CMOS	
AD15	—	42	I/O	CMOS	
A0	—	57	I	CMOS	PSP Demultiplexed Address Input Bus
A1	—	58	I	CMOS	
A2	—	59	I	CMOS	
A3	—	60	I	CMOS	
A4	—	61	I	CMOS	
A5	—	9	I	CMOS	
A6	—	10	I	CMOS	
A7	—	11	I	CMOS	
A8	—	12	I	CMOS	
A9	—	13	I	CMOS	
A10	—	19	I	CMOS	
A11	—	20	I	CMOS	
A12	—	43	I	CMOS	
A13	—	44	I	CMOS	
A14	—	45	I	CMOS	
AL	37	52	I	CMOS	PSP Address Latch
B0SEL	—	50	I	CMOS	PSP Byte 0 Select
B1SEL	—	48	I	CMOS	PSP Byte 1 Select
CLKOUT	23	33	O	—	Programmable Clock Output for External Use
$\overline{\text{CS}}$	34	49	I	CMOS	SPI Chip Select (active-low)
CS	34	49	I	CMOS	PSP Chip Select (active-high)
EN	35	50	I	CMOS	PSP R/W Enable strobe
$\overline{\text{INT}}$	24	34	O	—	Interrupt Output (active-low)
LEDA	10	15	O	—	Programmable Ethernet Status/Activity LED
LEDB	9	14	O	—	Programmable Ethernet Status/Activity LED

Legend: I = Input; O = Output; P = Power; CMOS = CMOS compatible input buffer; ANA = Analog level input/output

ENC424J600/624J600

TABLE 1-2: ENC424J600/624J600 PINOUT DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Input Buffer	Description
	44-Pin	64-Pin			
OSC1	3	3	I	ANA	25 MHz Crystal Oscillator/Clock Input
OSC2	2	2	O	—	25 MHz Crystal Oscillator Output
PSPCFG0	32	—	I	CMOS	PSP Mode Select 0
PSPCFG1	—	45	I	CMOS	PSP Mode Select 1
PSPCFG2	—	17	I	CMOS	PSP Mode Select 2
PSPCFG3	—	18	I	CMOS	PSP Mode Select 3
PSPCFG4	—	52	I	CMOS	PSP Mode Select 4
RBIAS	11	16	I	ANA	PHY Bias (external resistor) Connection
RD	36	51	I	CMOS	PSP Read Strobe
RW	36	51	I	CMOS	PSP Combined Read/Write Signal
SCK	37	52	I	CMOS	SPI Serial Clock Input
SI	36	51	I	CMOS	SPI Serial Data Input (from Master)
SO	35	50	O	—	SPI Serial Data Out (to Master)
SPISEL	24	34	I	CMOS	SPI/PSP Interface Select
TPIN-	17	27	I	ANA	Differential Ethernet Receive Minus Signal Input
TPIN+	16	26	I	ANA	Differential Ethernet Receive Plus Signal Input
TPOUT-	21	31	O	—	Differential Ethernet Transmit Minus Signal Output
TPOUT+	20	30	O	—	Differential Ethernet Transmit Plus Signal Output
VCAP	43	63	P	—	Regulator External Capacitor connection
VDD	44	21, 47, 64	P	—	Positive 3.3V Power Supply for Digital Logic
VDDOSC	4	4	P	—	Positive 3.3V Power Supply for 25 MHz Oscillator
VDDPLL	12	22	P	—	Positive 3.3V Power Supply for PHY PLL Circuitry
VDDRX	15	25	P	—	Positive 3.3V Power Supply for PHY RX Circuitry
VDDTX	18	28	P	—	Positive 3.3V Power Supply for PHY TX Circuitry
VSS	33, 42	46, 62	P	—	Ground Reference for Digital Logic
VSSOSC	1	1	P	—	Ground Reference for 25 MHz Oscillator
VSSPLL	13	23	P	—	Ground Reference for PHY PLL Circuitry
VSSRX	14	24	P	—	Ground Reference for PHY RX Circuitry
VSSTX	19, 22	29, 32	P	—	Ground Reference for PHY TX Circuitry
WR	35	50	I	CMOS	PSP Write Strobe
WRH	—	48	I	CMOS	PSP Write High Strobe
WRL	—	50	I	CMOS	PSP Write Low Strobe

Legend: I = Input; O = Output; P = Power; CMOS = CMOS compatible input buffer; ANA = Analog level input/output

2.0 EXTERNAL CONNECTIONS

2.1 Oscillator

ENC424J600/624J600 devices are designed to operate from a fixed 25 MHz clock input. This clock can be generated by an external CMOS clock oscillator or a parallel resonant, fundamental mode 25 MHz crystal attached to the OSC1 and OSC2 pins. Use of a crystal, rated for series resonant operation, will oscillate at an incorrect frequency. To comply with IEEE 802.3 Ethernet timing requirements, the clock must have no more than ± 50 ppm of total error; avoid using resonators or clock generators that exceed this margin.

When clocking the device using a crystal, follow the connections shown in Figure 2-1. When using a CMOS clock oscillator or other external clock source, follow Figure 2-2.

FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION

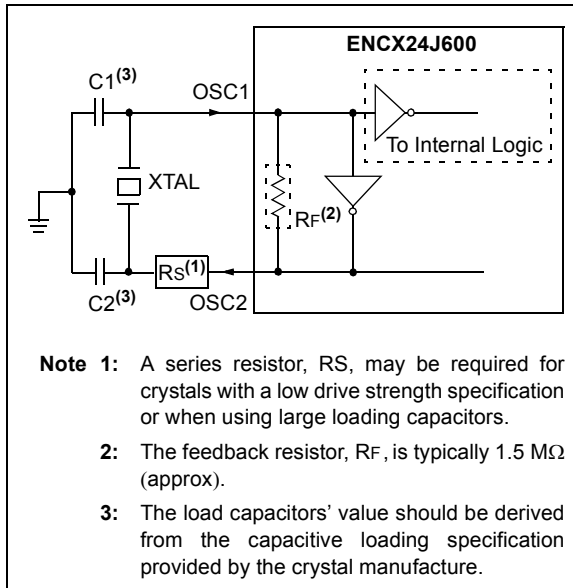
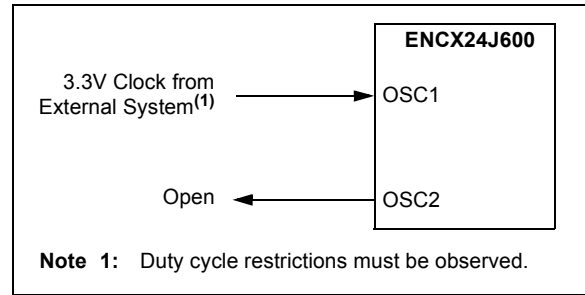


FIGURE 2-2: EXTERNAL CLOCK SOURCE



2.2 CLKOUT Pin

The Clock Out pin (CLKOUT) is provided for use as the host controller clock or as a clock source for other devices in the system. Its use is optional.

The 25 MHz clock applied to OSC1 is multiplied by a PLL to internally generate a 100 MHz base clock. This 100 MHz clock is driven through a configurable postscaler to yield a wide range of different CLKOUT frequencies. The PLL multiplication adds clock jitter, subject to the PLL jitter specification in **Section 17.0 "Electrical Characteristics"**. However, the postscaler ensures that the clock will have a nearly ideal duty cycle.

The CLKOUT function is enabled and the postscaler is selected via the COCON<3:0> bits (ECON2<11:8>). To create a clean clock signal, the CLKOUT output and COCON bits are unaffected by all resets and power-down modes. The CLKOUT function is enabled out of POR and defaults to producing a 4 MHz clock. This allows the device to directly clock the host processor.

When the COCON bits are written with a new configuration, the CLKOUT output transitions to the new frequency without producing any glitches. No high or low pulses with a shorter period than the original or new clock are generated.

ENC424J600/624J600

2.3 Voltage and Bias Pin

2.3.1 VDD AND VSS PINS

To reduce on-die noise levels and provide for the high-current demands of Ethernet, there are many power pins on ENC424J600/624J600 devices:

- VDD and VSS
- VDDOSC and VSSOSC
- VDDPLL and VSSPLL
- VDDRX and VSSRX
- VDDTX and VSSTX

Each VDD and VSS pin pair above should have a 0.1 μF ceramic bypass capacitor placed as close to the pins as possible. For best EMI emission suppression, other smaller capacitors, such as 0.001 μF , should be placed immediately across VDDTX/VSSTX and VDDPLL/VSSPLL.

All VDD power supply pins must be externally connected to the same 3.3V $\pm 10\%$ power source. Similarly, all VSS supply references must be externally connected to the same ground node. If a ground connection appears on two pins (e.g., VSSTX), connect both pins; do not allow either to float. In addition, it is recommended that the exposed bottom metal pad on the 44-pin QFN package be tied to VSS.

Placing ferrite beads or inductors between any two of the supply pins (e.g., between VDDOSC and VDDRX) is not recommended. However, it is acceptable to isolate all of the VDD supplies from the main circuit power supply through a single ferrite bead or inductor, if desired for supply noise suppression reasons. Such isolation is generally not necessary.

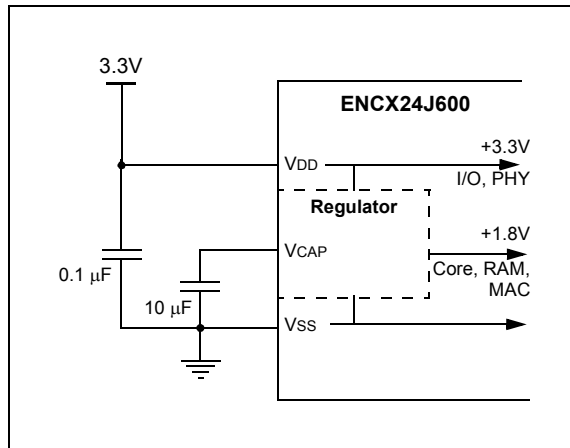
2.3.2 VCAP PIN

Most of the device's digital logic operates at a nominal 1.8V. This voltage is supplied by an on-chip voltage regulator, which generates the digital supply voltage from the VDD rail. The only external component required is an external filter capacitor, connected from the VCAP pin to ground, as shown in Figure 2-3. A value of at least 10 μF is recommended.

The capacitor must also have a relatively low Equivalent Series Resistance (ESR). It is recommended that a low-ESR capacitor (ceramic, tantalum or similar) should be used and high-ESR capacitors (such as aluminum electrolytic) should be avoided.

The internal regulator is not designed to drive external loads; therefore, do not attach other circuitry to VCAP.

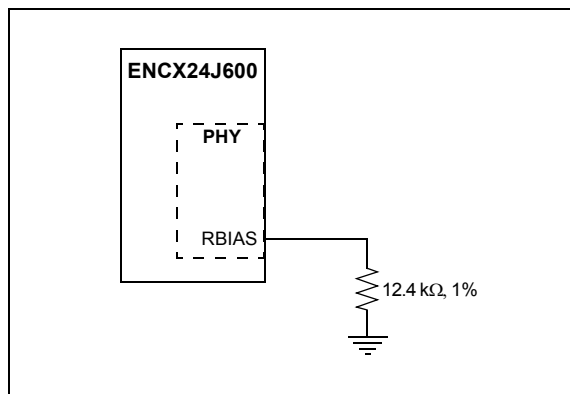
FIGURE 2-3: VCAP CONNECTIONS



2.3.3 RBIAS PIN

The internal analog circuitry in the PHY module requires that an external 12.4 k Ω , 1% resistor be attached from RBIAS to ground, as shown in Figure 2-4. The resistor influences the TPOUT+/- signal amplitude. The RBIAS resistor should be placed as close as possible to the chip with no immediately adjacent signal traces in order to prevent noise capacitively coupling into the pin and affecting the transmit behavior. It is recommended that the resistor be a surface mount type.

FIGURE 2-4: RBIAS RESISTOR



2.4 Ethernet Signal Pins and External Magnetics

Typical applications for ENC424J600/624J600 devices require an Ethernet transformer module, and a few resistors and capacitors to implement a complete IEEE 802.3 compliant 10/100 Ethernet interface, as shown in Figure 2-5.

The Ethernet transmit interface consists of two pins: TPOUT+ and TPOUT-. These pins implement a differential pair and a current-mode transmitter. To generate an Ethernet waveform, ordinary applications require the use of a 1:1 center tapped pulse transformer, rated for 10/100 or 10/100/1000 Ethernet operations. When the Ethernet module is enabled and linked with a partner, current is continually sunk through both TPOUT pins. When the PHY is actively transmitting, a differential voltage is created on the Ethernet cable by varying the relative current sunk by TPOUT+ compared to TPOUT-.

The Ethernet receive interface similarly consists of a differential pair: TPIN+ and TPIN-. To meet IEEE 802.3 compliance and help protect against electrostatic discharge, these pins are normally isolated from the Ethernet cable by a 1:1 center tapped transformer (available in the same package as the TX transformer).

Internally, the PHY uses a high-speed ADC to sample the receive waveform and decodes it using a DSP. The PHY implements many robustness features, including

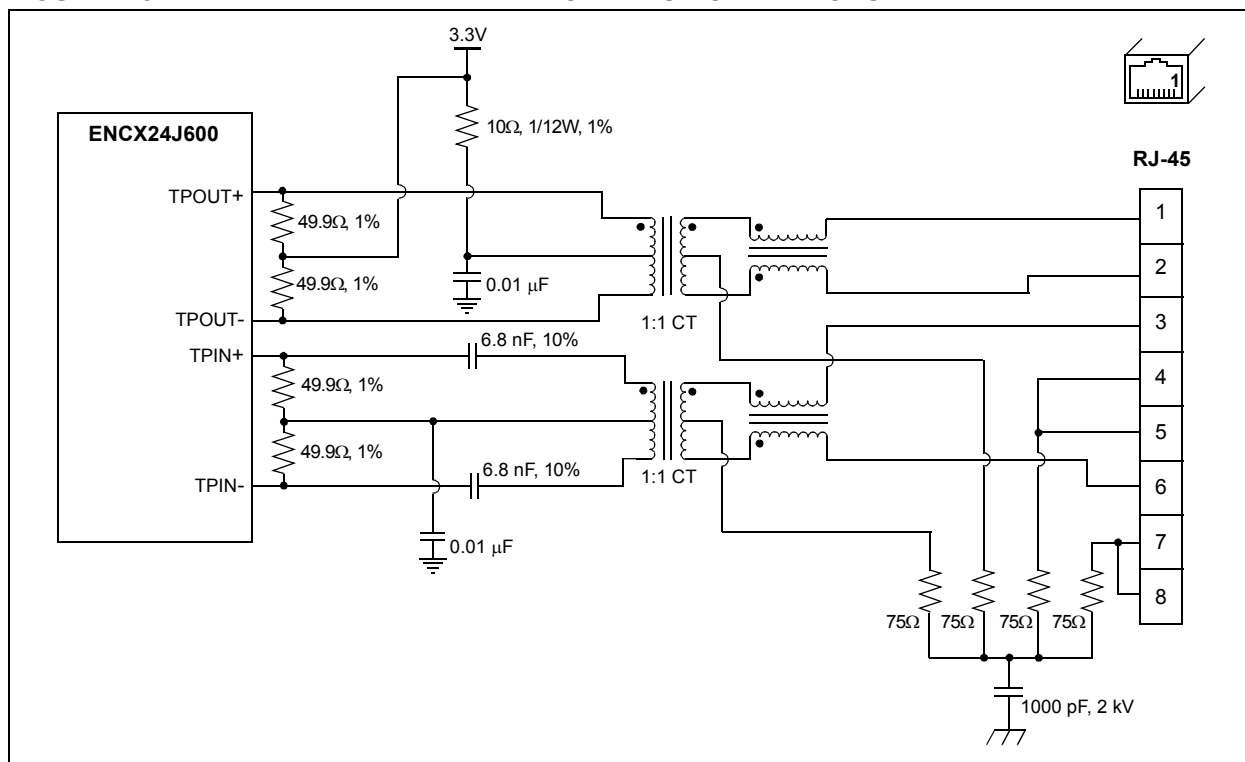
baseline wander correction (applicable to 100Base-TX) and automatic RX polarity correction (applicable to 10Base-T).

Four 49.9Ω, 1% resistors are required for proper termination of the TX and RX transmission lines. If the board layout necessitates long traces between the ENC424J600 and Ethernet transformers, the termination resistors should be placed next to the silicon instead of the transformers.

On the receive signal path, two 6.8 nF 10% capacitors are used. These capacitors, in combination with the 49.9Ω termination resistors, form an RC high-pass filter to reduce baseline wander. For best performance, these capacitors should not be omitted or changed. The various remaining capacitors provide DC current blocking and provide stability to the common-mode voltage of both of the differential pairs. The TPIN+/- pins weakly output a common-mode voltage that is acceptable to the internal ADC. For proper operation, do not attempt to externally force the TPIN+/- common-mode voltage to some other value.

The 10Ω 1% resistor provides a current path from the power supply to the center tap of the TX transformer. As mentioned previously, the TPOUT+/- pins implement a Current mode drive topology in which the pins are only capable of sinking current; they do not produce a direct voltage. This current path through the transformer generates the transmit waveform. The 10Ω resistor reduces the amount of heat that the PHY would have to dissipate, and therefore, must have a power rating of 1/12W or better.

FIGURE 2-5: TYPICAL ETHERNET MAGNETICS CONNECTIONS

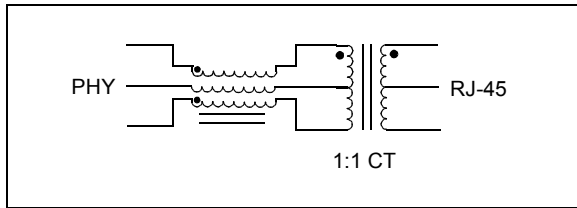


ENC424J600/624J600

2.4.1 ADDITIONAL EMI AND LAYOUT CONSIDERATIONS

To reduce EMI emissions, common-mode chokes are shown adjacent to the transformers on the cable (RJ-45) side. These chokes come standard in typical Ethernet transformer modules. Because the ENCX24J600 PHY uses a current-mode drive topology, the transmit choke must normally be located on the cable side of the transmit transformer. Orienting the magnetics such that the choke is on the PHY side of the transmit transformer usually results in a distorted, non-compliant transmit waveform. However, some magnetics which wrap the TX center tap wire around the TX choke core can also be used to generate a compliant waveform (Figure 2-6). These types of transformers may be desirable in some Power-over Ethernet (PoE) applications.

FIGURE 2-6: ALTERNATE TX CHOKE TOPOLOGY



The common-mode choke on the RX interface can be placed on either the cable side or PHY side of the receive transformer. Recommended and required magnetics characteristics are located in **Section 17.0 “Electrical Characteristics”**.

The four 75Ω resistors and high-voltage capacitor in Figure 2-5 are intended to prevent each of the twisted pairs in the Ethernet cables from floating and radiating EMI. Their implementation may require adjustment in PoE applications.

Unless the TX and RX signal pairs are kept short, they should be routed between the ENCX24J600 and the Ethernet connector following differential routing rules. Like Ethernet cables, 100Ω characteristic impedance should be targeted for the differential traces. The use of vias, which introduce impedance discontinuities, should be minimized. Other board level signals should not run immediately parallel to the TX and RX pairs to minimize capacitive coupling and crosstalk.

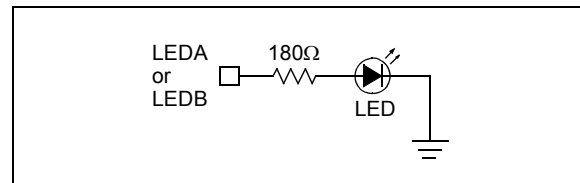
2.5 LEDA and LEDB Pins

The LEDA and LEDB pins provide dedicated LED status indicator outputs. The LEDs are intended to display link status and TX/RX activity among other programmable options; however, the use of one or both is entirely optional. The pins are driven automatically by the hardware and require no support from the host microcontroller. Aside from the LEDs themselves, a current-limiting resistor is generally the only required component.

By default on POR, LEDA displays the Ethernet link status, while LEDB displays PHY-level TX/RX activity. Because the LEDs operate at the PHY level, RX activity will be displayed on LEDB any time Ethernet packets are detected, regardless of if the packet is valid and meets the correct RX filtering criteria.

Normally, the device illuminates the LED by sourcing current out of the pin, as shown in Figure 2-7. Connecting the LED in reverse, with the anode connected to VDD and the cathode to LEDA/LEDB (through a current-limiting resistor), causes the LED to show “inverted sense” behavior, lighting the LED when it should be off and extinguishing the LED when the LED should be on.

FIGURE 2-7: SINGLE COLOR LED CONNECTION

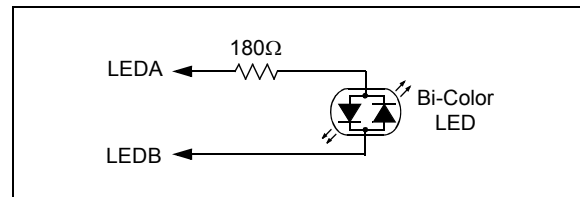


Both LEDs automatically begin operation whenever power is applied, a 25 MHz clock is present and the Ethernet magnetics are present and wired correctly. A connection to the host microcontroller via the SPI or PSP interface is not required. LEDA and LEDB can, therefore, be used as a quick indicator of successful assembly during initial prototype development.

2.5.1 USING BI-COLOR LEDs

In space constrained applications, it is frequently desirable to use a single bi-color LED to display multiple operating parameters. These LEDs are connected between LEDA and LEDB, as shown in Figure 2-8.

FIGURE 2-8: BI-COLOR LED CONNECTION



ENCX24J600 devices include two special hardware display modes to make maximal use of a bi-color LED. These modes are selected when the LACFG<3:0> and LBCFG<3:0> bits (EIDLED<15:8>) are set to ‘1111’ or ‘1110’. In these configurations, the link state turns the LED on, the speed/duplex state sets the LED color and TX/RX events cause the LED to blink off. If a link is present, no TX/RX events are occurring and the speed/duplex state is 100 Mbps/full duplex, respectively, then the LEDB pin will be driven high while LEDA will be driven low.

2.6 INT Pin

The $\overline{\text{INT}}$ pin is an active-low signal that is used to flag interrupt events to external devices. Depending on the application, it can be used to signal the host microcontroller whenever a packet has been received or transmitted, or that some other asynchronous operation has occurred. It can also be used to wake-up the microcontroller or other system components based on LAN activity; its use is optional.

The $\overline{\text{INT}}$ pin is driven high when no interrupt is pending and is driven low when an interrupt has occurred. It does not go into a high-impedance state, except during initial power-on while the multiplexed SPISEL pin function is being used.

Since ENC424J600/624J600 devices incorporate a buffer for storing transmit and receive packets, the host microcontroller never needs to perform real-time operations on the device. The microcontroller can poll the device registers to discover if the device status has changed.

2.7 Host Interface Pins

For the maximum degree of flexibility in interfacing with microcontrollers, ENC424J600/624J600 devices offer a choice between a serial interface based on the Serial Peripheral Interface (SPI) standard, and a flexible 8 or 16-bit parallel slave port (PSP) interface. Only one interface may be used at any given time.

The I/O interface is hardware selected on power-up using the SPISEL function on the $\overline{\text{INT}}$ /SPISEL pin. This is done by latching in the voltage level applied to the pin

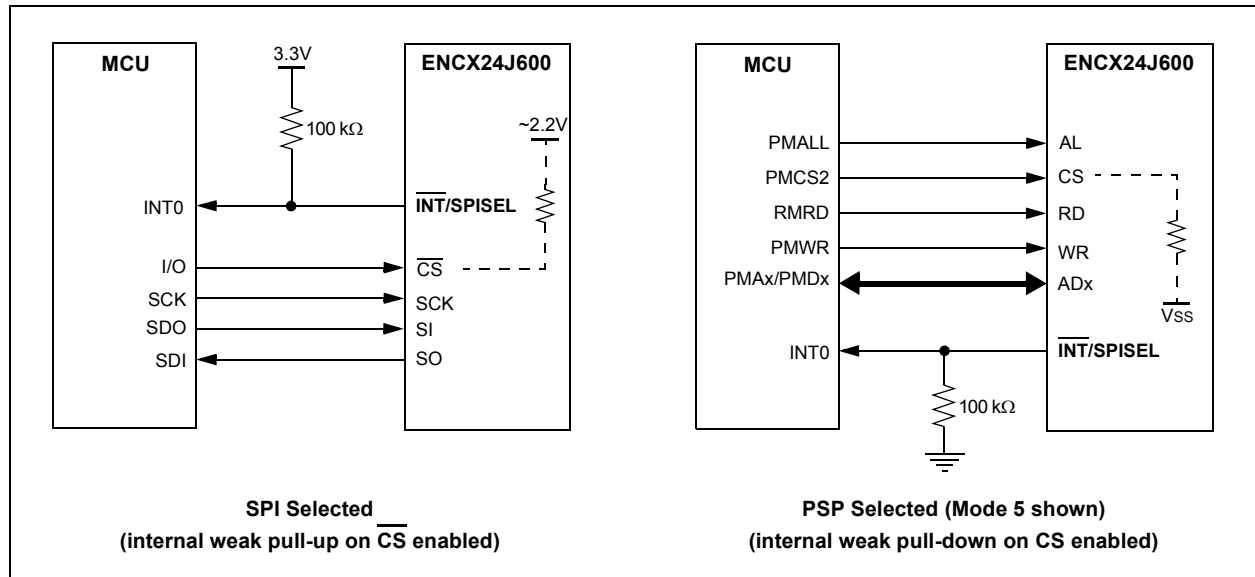
approximately 1 to 10 μs after power is applied to the device and the device exits Power-on Reset. If SPISEL is latched at a logic high state, the serial interface is enabled. If SPISEL is latched at a logic low state, the PSP interface is enabled. Figure 2-9 shows example connections required to select the SPI or PSP interface upon power-up.

To ensure the SPI interface is selected upon power-up, an external pull-up resistor to VDD must be connected to the SPISEL pin. Alternatively, if the parallel interface is to be used, a pull-down resistor to VSS must be connected to the SPISEL pin. In most circuits, it is recommended that a 100 k Ω or smaller resistor be used to ensure that the correct logic level is latched in reliably. If a large capacitance is present in the SPISEL circuit, such as from stray capacitance, a smaller pull-up or pull-down resistor may be required to compensate and ensure the correct level is sensed during power-up.

As SPISEL is multiplexed with the $\overline{\text{INT}}$ interrupt output function, a direct connection to VDD or VSS without a resistor is prohibited. If $\overline{\text{INT}}$ is connected to the host microcontroller, the microcontroller must leave this signal in a high-impedance state and not attempt to drive it to an incorrect logic state during power-up.

If the VDD supply has a slow ramp rate, the device will exit POR, exceed the 1 to 10 μs latch timer and sample the SPISEL pin state before VDD has reached the specified minimum operating voltage of the device. In this case, the device will still latch in the correct value, assuming the minimum V_{IH} (D004) or maximum V_{IL} (D006) specification is met, which is a function of VDD.

FIGURE 2-9: USING THE $\overline{\text{INT}}$ /SPISEL PIN TO SELECT THE I/O INTERFACE



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2.7.1 SPI

When enabled, the SPI interface is implemented with four pins:

- \overline{CS}
- SO
- SI
- SCK

All four of these pins must be connected to use the SPI interface.

The \overline{CS} , SI and SCK input pins are 5V tolerant. The SO pin is also 5V tolerant when in a high-impedance state. SO is always high-impedance when \overline{CS} is connected to logic high (i.e., chip not selected).

When the SPI interface is enabled, all PSP interface pins (except PSPCFG2 and PSPCFG3 on ENC624J600 devices) are unused. They are placed in a high-impedance state and their input buffers are disabled. For best ESD performance, it is recommended that the unused PSP pins be tied to either Vss or VDD. However, these pins may be left floating if it is desirable for board level layout and routing reasons.

When using an ENC624J600 device in SPI mode, it is recommended that the PSPCFG2 and PSPCFG3 pins be tied to either Vss or any logic high voltage, and not be left floating. The particular state used is unimportant.

2.7.2 PSP

Depending on the particular device, the PSP interface is implemented with up to 34 pins. The interface is highly configurable to accommodate many different

parallel interfaces; not all available pins are used in every configuration. Up to 8 different operating modes are available. These are explained in detail in **Section 5.0 “Parallel Slave Port Interface (PSP)”**.

The PSPCFG pins control which parallel interface mode is used. The values on these pins are latched upon device power-up in the same manner as the SPISEL pin. The combinations of VDD and Vss voltages on the different PSPCFG mode pins determine the PSP mode according to Table 2-1.

On ENC424J600 devices, only PSP Modes 5 and 6 (8-bit width, multiplexed data and address) are available. The mode is selected by applying Vss or VDD, respectively, to PSPCFG0.

On ENC624J600 devices, all eight PSP modes are available and are selected by connecting the PSPCFG<4:1> pins directly to VDD or ground. The mode selection is encoded such that the multiplexed pin functions, AD14 (on PSPCFG1) and SCK/AL (on PSPCFG4), are used only in the “don’t care” positions. Therefore, pull-up/pull-down resistors are not required for these pins.

All PSP pins, except for AD<15:0>, are inputs to the ENC624J600 family device and are 5V tolerant. The AD<15:0> pins are bidirectional I/Os and are 5V tolerant in Input mode. The pins are always inputs when the CS signal is low (chip not selected).

Any unused PSP pins are placed in a high-impedance state. However, it is recommended that they be tied to either Vss or a logic high voltage and not be left floating.

TABLE 2-1: PSP MODE SELECTION FOR ENC424J600/624J600 DEVICES

Interface Mode	$\overline{INT}/SPISEL$	PSPCFG					Pins Used
		0	1	2	3	4	
44-Pin							
PSP Mode 5	Pull Down	0	—	—	—	—	AL, CS, RD, WR, AD<14:0>
PSP Mode 6	Pull Down	1	—	—	—	—	AL, CS, \overline{RW} , EN, AD<14:0>
64-Pin							
PSP Mode 1	Pull Down	—	x	0	0	0	CS, RD, WR, A14:A0, AD<7:0>
PSP Mode 2	Pull Down	—	x	0	0	1	CS, \overline{RW} , EN, A14:A0, AD<7:0>
PSP Mode 3	Pull Down	—	x	1	0	0	CS, RD, WRL, WRH, A<13:0>, AD<15:0>
PSP Mode 4	Pull Down	—	x	1	0	1	CS, \overline{RW} , B0SEL, B1SEL, A<13:0>, AD<15:0>
PSP Mode 5	Pull Down	—	0	0	1	x	AL, CS, RD, WR, AD<14:0>
PSP Mode 6	Pull Down	—	1	0	1	x	AL, CS, \overline{RW} , EN, AD<14:0>
PSP Mode 9	Pull Down	—	0	1	1	x	AL, CS, RD, WRL, WRH, AD<15:0>
PSP Mode 10	Pull Down	—	1	1	1	x	AL, CS, \overline{RW} , B0SEL, B1SEL, AD<15:0>

Legend: x = don’t care, 0 = logic low (tied to Vss), 1 = logic high (tied to VDD), — = pin not present

2.7.3 $\overline{\text{CS}}$ /CS PIN

The chip select functions for the serial and parallel interfaces are shared on one common pin, $\overline{\text{CS}}$ /CS. This pin is equipped with both internal weak pull-up and weak pull-down resistors. If the SPI interface is selected ($\overline{\text{CS}}$), the pull-up resistor is automatically enabled and the pull-down resistor is disabled. If the PSP interface is chosen (CS), the pull-down resistor is automatically enabled and the pull-up resistor is disabled. This allows the $\overline{\text{CS}}$ /CS pin to stay in the unselected state when not being driven, avoiding the need for an external board level resistor on this pin.

When enabled by using SPI mode, the internal weak pull-up only pulls the $\overline{\text{CS}}$ /CS pin up to approximately $V_{DD}-1.1V$ or around 2.2V at typical conditions without any loading; it does not pull all the way to V_{DD} . When using the PSP interface, the pull-down will be enabled, which is capable of pulling all the way to V_{SS} when unloaded.

2.8 Digital I/O Levels

All digital output pins on ENC424J600/624J600 devices contain CMOS output drivers that are capable of sinking and sourcing up to 18 mA continuously. All digital inputs and I/O pins operating as inputs are 5V tolerant. These features generally mean that the ENC424J600 can connect directly to the host microcontroller without the need of any glue logic. However, some consideration may be necessary when interfacing with 5V systems.

Since the digital outputs drive only up to the V_{DD} voltage (3.3V nominally), the voltage may not be high enough to ensure a logical high is detected by 5V systems which have high input thresholds. In such cases, unidirectional level translation from the 3.3V ENC424J600 up to the 5V host microcontroller may be needed.

When using the SPI interface, an economical 74HCT08 (quad AND gate), 74ACT125 (quad 3-state buffer) or other 5V CMOS chip with TTL level input buffers may be used to provide the necessary level shifting. The use of 3-state buffers permits easy integration into systems which share the SPI bus with other devices. However, users must make certain that the propagation delay of the level translator does not reduce the maximum SPI frequency below desired levels. Figure 2-10 and Figure 2-11 show two example translation schemes.

When using the PSP interface, eight, or all sixteen of the ADx pins, may need level translation when performing read operations on the ENC424J600. The 8-bit 74ACT245 or 16-bit 74ACT16245 bus transceiver, or similar devices, may be useful in these situations.

FIGURE 2-10: LEVEL SHIFTING ON THE SPI INTERFACE USING AND GATES

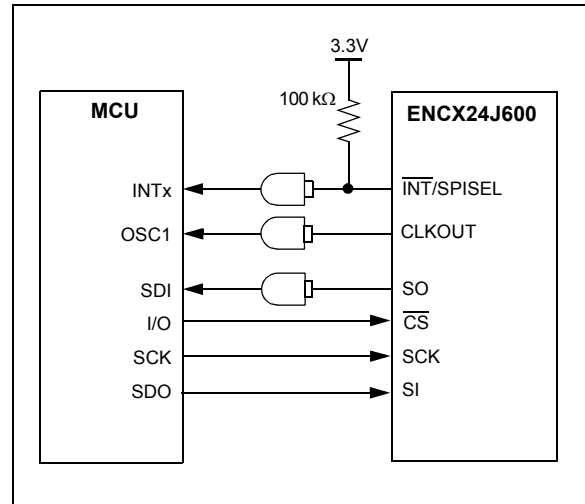
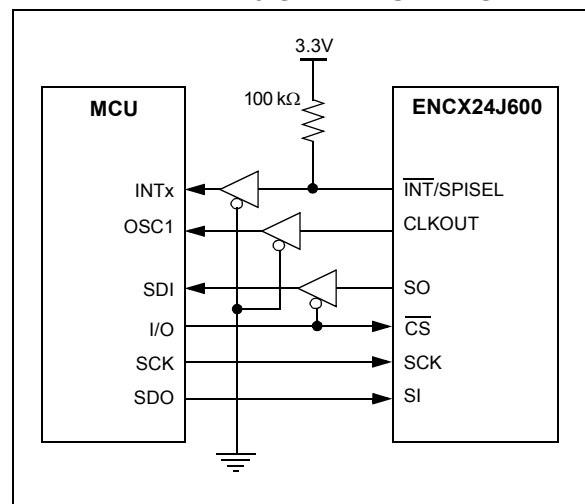


FIGURE 2-11: LEVEL SHIFTING ON THE SPI INTERFACE USING 3-STATE BUFFERS



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NOTES:

3.0 MEMORY ORGANIZATION

All memory in ENC424J600/624J600 devices is implemented as volatile RAM. Functionally, there are four unique memories:

- Special Function Registers (SFRs)
- PHY Special Function Registers
- Cryptographic Data Memory
- SRAM Buffer

The SFRs configure, control and provide status information for most of the device. They are directly accessible through the I/O interface.

The PHY SFRs configure, control and provide status information for the PHY module. They are located inside the PHY module and isolated from all other normal SFRs, so they are not directly accessible through the I/O interface.

The cryptography data memory is used to store key and data material for the modular exponentiation, AES and MD5/SHA-1 hashing engines. This memory area can only be accessed through the DMA module.

The SRAM buffer is a bulk 12K x 16-bit (24 Kbyte) RAM array used for TX and RX packet buffering, as well as general purpose storage by the host microcontroller. Although the SRAM uses a 16-bit word, it is byte-writable. This memory is indirectly accessible through pointers on all I/O interfaces. It can also be accessed directly through the PSP interfaces.

3.1 I/O Interface and Memory Map

Depending on the I/O interface selected, the four memories are arranged into two or three different memory address spaces. When the serial interface is selected, the memories are grouped into three address spaces. When one of the parallel interfaces is selected, they are arranged into two address spaces. In all cases, the PHY SFRs reside in their own memory address space.

3.1.1 SPI INTERFACE MAP

When the SPI interface is selected, the device memory map is comprised of three memory address spaces (Figure):

- the SFR area
- the main memory area
- the PHY register area

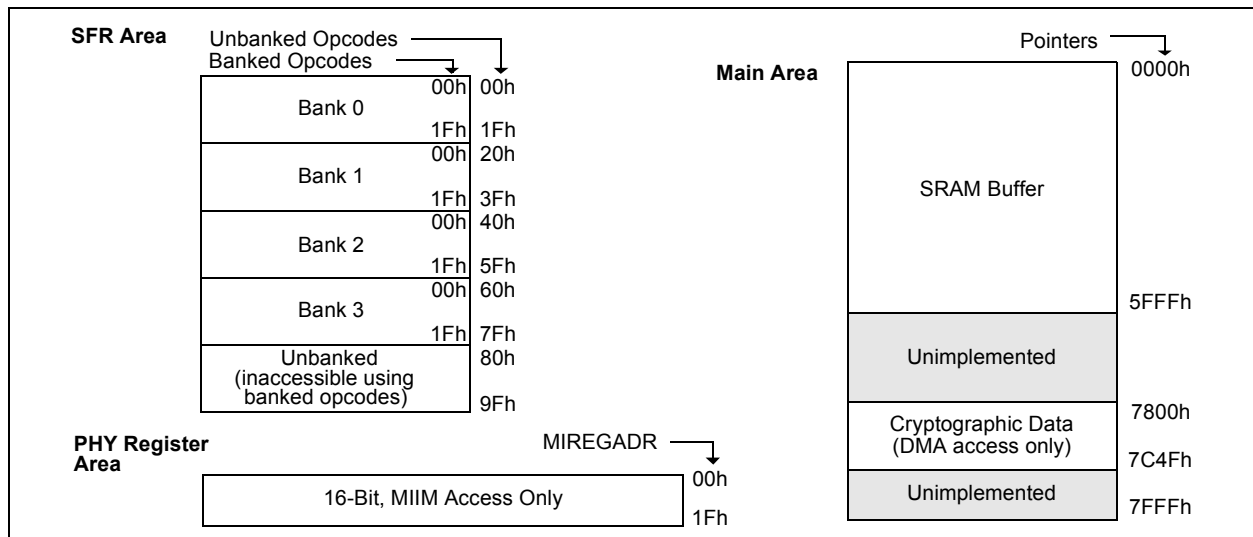
The SFR area is directly accessible to the user. This is a linear memory space that is 160 bytes long. For efficiency, the SFR area can be addressed as four banks of 32 bytes each, starting at the beginning of the space (00h), with an additional unbanked area of 32 bytes at the end of the SFR memory. Banked addressing allows SFRs to be addressed with fewer address bits being exchanged over the serial interface for each transaction. This decreases protocol overhead and enhances performance. SFRs can also be directly addressed by their 8-bit unbanked addresses using unbanked SPI commands. This allows for a simpler interface whenever transaction overhead is not critical.

The main memory area is organized as a linear, byte-addressable space of 32 Kbytes. Of this, the first 24-Kbyte area (0000h through 5FFFh) is implemented as the SRAM buffer. The buffer is accessed by the device using several SFRs as memory pointers and virtual data window registers, as described in **Section 3.5.5 “Indirect SRAM Buffer Access”**.

Addresses in the main memory area, between 7800h and 7C4Fh, are mapped to the memory for the cryptographic data modules. These addresses are not directly accessible through the SPI interface; they can only be accessed through the DMA.

The PHY SFRs are the final memory space. This is a linear, word-addressable memory space of 32 words. This area is only accessible by the MIIM interface (see **Section 3.3 “PHY Special Function Registers”** for more details).

FIGURE 3-1: ENC424J600/624J600 MEMORY MAP WITH SPI INTERFACE



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3.1.2 PSP INTERFACE MAPS

When one of the parallel interfaces is selected, the memory map is very different from the SPI map. There are two different memory address spaces (Figure 3-2):

- the main memory area
- the PHY register area

As in the serial memory map, the main memory area is a linear, byte-addressable space of 32 Kbytes, with the SRAM buffer located in the first 24-Kbyte region. The cryptographic data memory is also mapped to the same location as in the serial memory map. The main difference is that the SFRs are now located to an area with a higher address than the cryptographic data space. Additional memory areas above the SFRs are reserved for their accompanying Bit Set and Bit Clear registers.

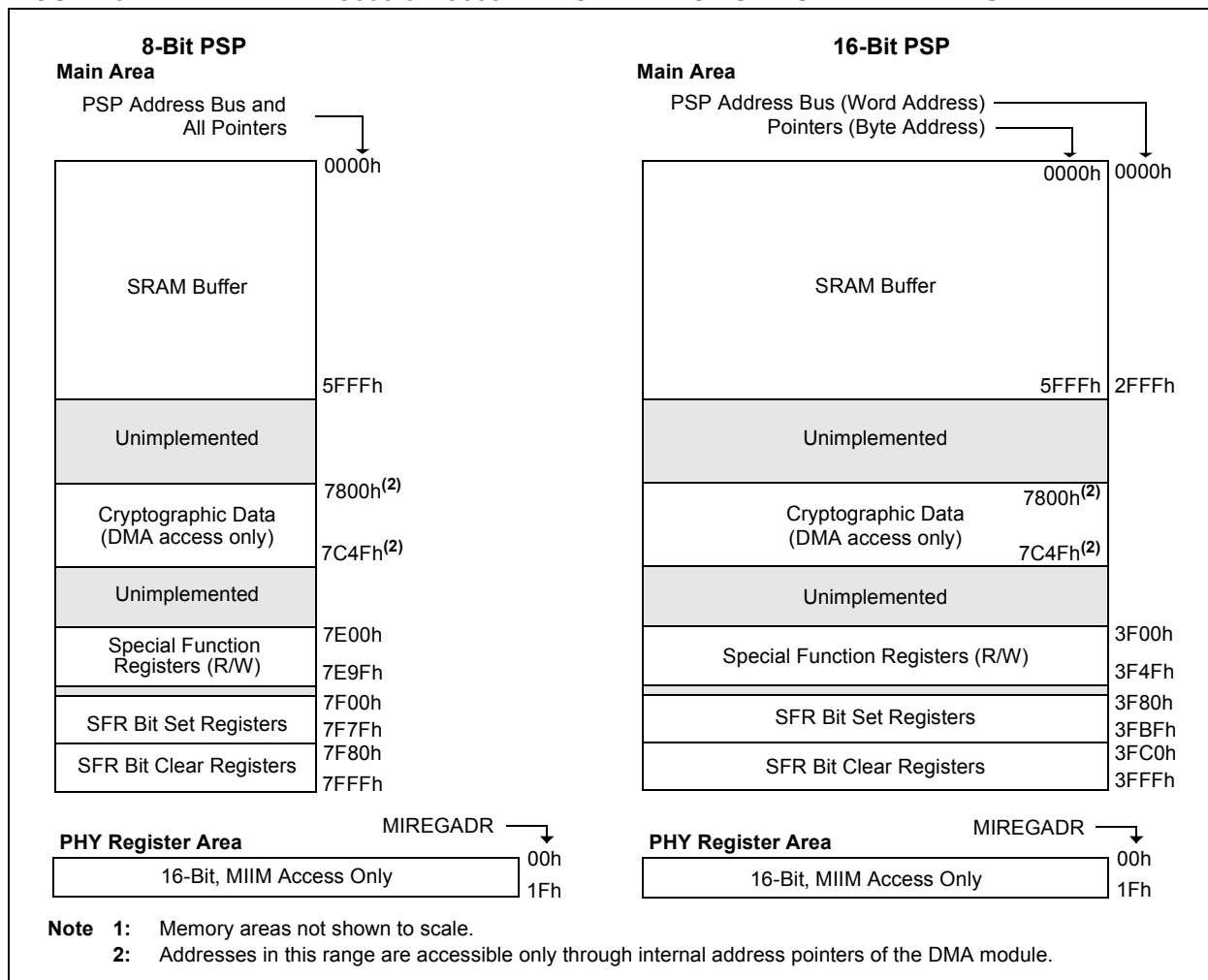
Except for the cryptographic data memory, all addresses in the main memory area are directly accessible using the PSP bus. As with the serial interface, the cryptographic memory can only be accessed through the DMA.

The difference between the 8-bit and 16-bit interfaces is how the SRAM buffer is addressed by the external address bus. In 16-bit data modes, the address bus treats the buffer as a 16-byte wide, word-addressable space, spanning 0000h to 3FFFh. In 8-bit data modes, the address bus treats the buffer as an 8-bit, byte-addressable space, ranging from 0000h to 7FFFh. In either case, the SFRs used as memory pointers still address the buffer as a byte-wide, byte-addressable space.

The PHY SFR space is implemented in the same manner as the SPI interface described above.

In both 8-bit and 16-bit PSP modes, full device functionality can be realized without using the full width of the address bus. This is because the SRAM buffer can still be read and written to by using SFR pointers. In practical terms, this can allow designers in space or pin constrained applications to only connect a subset of the A or AD address pins to the host microcontroller. For example, in the 8-Bit Multiplexed PSP Modes 5 or 6, tying pins, AD<14:9> to VDD, still allows direct address access to all SFRs. This reduces the number of pins required for connection to the host controller, including the interface control pins to 12 or 13.

FIGURE 3-2: ENC424J600/624J600 MEMORY MAPS FOR PSP INTERFACES⁽¹⁾



3.2 Special Function Registers

The SFRs provide the main interface between the host controller and the on-chip Ethernet controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

All registers are 16 bits wide. On the SPI and 8-bit PSP interfaces, which are inherently byte-oriented, the registers are split into separate high and low locations which are designated by an “H” or “L” suffix, respectively. All registers are organized in little-endian format such that the low byte is always at the lower memory address.

Some of the available addresses are unimplemented or marked as reserved. These locations should not be written to. Data read from reserved locations should be ignored. Reading from unimplemented locations will return ‘0’. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

The addresses of all user-accessible registers are provided in Tables 3-1 through 3-6. A complete bit level listing of the SFRs is presented in Table 3-7 (page 26).

3.2.1 E REGISTERS

SFRs with names starting with “E” are the primary control and pointer registers. They configure and control all of the (non-MAC) top-level features of the device, as well as manipulate the pointers that define the memory buffers. These registers can be read and written in any order, with any length, without concern for address alignment.

3.2.2 MAC REGISTERS

SFRs with names that start with “MA” or “MI” are implemented in the MAC module hardware. For this reason, their operation differs from “E” registers in two ways.

First, MAC registers support read and write operations only. Individual bit set and bit clear operations cannot be performed.

Additionally, MAC registers must always be written as a 16-bit word, regardless of the I/O interface being used. That is, on the SPI or 8-bit PSP interfaces, all write operations must be performed by writing to the low byte, followed by a write to the associated high byte. On 16-bit PSP interfaces, both write enables or byte selects must be asserted to perform the 16-bit write. Non-sequential writes, such as writing to the low byte of one MAC register, the low byte of a second MAC register and then the high byte of the first register cannot be performed.

3.2.3 SPI REGISTER MAP

As previously described, the SFR memory is partitioned into four banks plus a special region that is not bank addressable. Each bank is 32 bytes long and addressed by a 5-bit address value. All SFR memory may also be accessed via unbanked SPI opcodes which use a full 8-bit address to form a linear address map without banking.

The last 10 bytes (16h to 1Fh) of all SPI banks point to a common set of five registers: EUDAST, EUDAND, ESTAT, EIR and ECON1. These are key registers used in controlling and monitoring the operation of the device. Their common banked addresses allow easy access without switching the bank.

The SPI interface implements a comprehensive instruction set that allows for reading and writing of registers, as well as setting and clearing individual bits or bit fields within registers. The SPI instruction set is explained in detail in **Section 4.0 “Serial Peripheral Interface (SPI)”**.

The SFR map for the SPI interface is shown in Table 3-1. Registers are presented by a bank. The banked (5-bit) address applicable to the registers in each row is shown in the left most column. The unbanked (8-bit) address for each register is shown to the immediate left of the register name.

Note: SFRs in the unbanked region (80h through 9Fh) cannot be accessed using banked addressing. The use of an unbanked SFR opcode is required to perform operations on these registers.
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TABLE 3-1: ENC424J600/624J600 SFR MAP (SPI INTERFACE)

Banked Register Addresses	Bank 0 (00h offset)		Bank 1 (20h offset)		Bank 2 (40h offset)		Bank 3 (60h offset)		Unbanked ⁽¹⁾ (80h offset)	
	Unbanked Address	Name	Unbanked Address	Name	Unbanked Address	Name	Unbanked Address	Name	Unbanked Address	Name
00	00	ETXSTL	20	EHT1L	40	MACON1L	60	MAADR3L	80	EGPDATA ⁽²⁾
01	01	ETXSTH	21	EHT1H	41	MACON1H	61	MAADR3H	81	Reserved
02	02	ETXLENL	22	EHT2L	42	MACON2L	62	MAADR2L	82	ERXDATA ⁽²⁾
03	03	ETXLENH	23	EHT2H	43	MACON2H	63	MAADR2H	83	Reserved
04	04	ERXSTL	24	EHT3L	44	MABBIPGL	64	MAADR1L	84	EUDADATA ⁽²⁾
05	05	ERXSTH	25	EHT3H	45	MABBIPGH	65	MAADR1H	85	Reserved
06	06	ERXTAILL	26	EHT4L	46	MAIPGL	66	MIWRL	86	EGPRDPTL
07	07	ERXTAILH	27	EHT4H	47	MAIPGH	67	MIWRH	87	EGPRDPTH
08	08	ERXHEADL	28	EPMM1L	48	MACLCONL	68	MIRDL	88	EGPWRPTL
09	09	ERXHEADH	29	EPMM1H	49	MACLCONH	69	MIRDH	89	EGPWRPTH
0A	0A	EDMASTL	2A	EPMM2L	4A	MAMXFLL	6A	MISTATL	8A	ERXRDPPTL
0B	0B	EDMASTH	2B	EPMM2H	4B	MAMXFLH	6B	MISTATH	8B	ERXRDPPTH
0C	0C	EDMALENL	2C	EPMM3L	4C	Reserved	6C	EPAUSL	8C	ERXWRPTL
0D	0D	EDMALENH	2D	EPMM3H	4D	Reserved	6D	EPAUSH	8D	ERXWRPTH
0E	0E	EDMADSTL	2E	EPMM4L	4E	Reserved	6E	ECON2L	8E	EUDARDPTL
0F	0F	EDMADSTH	2F	EPMM4H	4F	Reserved	6F	ECON2H	8F	EUDARDPTH
10	10	EDMACSL	30	EPMCSL	50	Reserved	70	ERXWML	90	EUDAWRPTL
11	11	EDMACSH	31	EPMCSH	51	Reserved	71	ERXWMH	91	EUDAWRPTH
12	12	ETXSTATL	32	EPMOL	52	MICMDL	72	EIEL	92	Reserved
13	13	ETXSTATH	33	EPMOH	53	MICMDH	73	EIEH	93	Reserved
14	14	ETXWIREL	34	ERXFCONL	54	MIREGADRL	74	EIDLEDL	94	Reserved
15	15	ETXWIREH	35	ERXFCONH	55	MIREGADRH	75	EIDLEDH	95	Reserved
16	16	EUDASTL	36	EUDASTL	56	EUDASTL	76	EUDASTL	96	Reserved
17	17	EUDASTH	37	EUDASTH	57	EUDASTH	77	EUDASTH	97	Reserved
18	18	EUDANDL	38	EUDANDL	58	EUDANDL	78	EUDANDL	98	Reserved
19	19	EUDANDH	39	EUDANDH	59	EUDANDH	79	EUDANDH	99	Reserved
1A	1A	ESTATL	3A	ESTATL	5A	ESTATL	7A	ESTATL	9A	Reserved
1B	1B	ESTATH	3B	ESTATH	5B	ESTATH	7B	ESTATH	9B	Reserved
1C	1C	EIRL	3C	EIRL	5C	EIRL	7C	EIRL	9C	Reserved
1D	1D	EIRH	3D	EIRH	5D	EIRH	7D	EIRH	9D	Reserved
1E	1E	ECON1L	3E	ECON1L	5E	ECON1L	7E	ECON1L	9E	—
1F	1F	ECON1H	3F	ECON1H	5F	ECON1H	7F	ECON1H	9F	—

- Note** 1: Unbanked SFRs can be accessed only by unbanked SPI opcodes.
 2: When using these registers to access the SRAM buffer, use only the N-byte SRAM instructions. See **Section 4.6.2 “Unbanked SFR Operations”** and **Section 4.6.3 “SRAM Buffer Operations”** for more details.

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3.2.4 PSP REGISTER MAP

When using a PSP interface, the SFR memory is linear; all registers are directly accessible without banking. To maintain consistency with the SPI interface, the EUDAST, EUDAND, ESTAT, EIR and ECON1 registers are instantiated in four locations in the PSP memory maps. Users may opt to use any one of these four locations.

The SFR maps for the 8-bit and 16-bit PSP interfaces are shown in Table 3-2 and Table 3-3, respectively.

TABLE 3-2: ENC424J600/624J600 SFR MAP (BASE REGISTER MAP, 8-BIT PSP INTERFACE)

Addr	Name	Addr	Name	Addr	Name	Addr	Name	Addr	Name
7E00	ETXSTL	7E20	EHT1L	7E40	MACON1L	7E60	MAADR3L	7E80	EGPDATA
7E01	ETXSTH	7E21	EHT1H	7E41	MACON1H	7E61	MAADR3H	7E81	Reserved
7E02	ETXLLENL	7E22	EHT2L	7E42	MACON2L	7E62	MAADR2L	7E82	ERXDATA
7E03	ETXLLENH	7E23	EHT2H	7E43	MACON2H	7E63	MAADR2H	7E83	Reserved
7E04	ERXSTL	7E24	EHT3L	7E44	MABBIPGL	7E64	MAADR1L	7E84	EUDADATA
7E05	ERXSTH	7E25	EHT3H	7E45	MABBIPGH	7E65	MAADR1H	7E85	Reserved
7E06	ERXTAILL	7E26	EHT4L	7E46	MAIPGL	7E66	MIWRL	7E86	EGPRDPTL
7E07	ERXTAILH	7E27	EHT4H	7E47	MAIPGH	7E67	MIWRH	7E87	EGPRDPTH
7E08	ERXHEADL	7E28	EPMM1L	7E48	MACLCONL	7E68	MIRDL	7E88	EGPWRPTL
7E09	ERXHEADH	7E29	EPMM1H	7E49	MACLCONH	7E69	MIRDH	7E89	EGPWRPTH
7E0A	EDMASTL	7E2A	EPMM2L	7E4A	MAMXFLL	7E6A	MISTATL	7E8A	ERXRDPTL
7E0B	EDMASTH	7E2B	EPMM2H	7E4B	MAMXFLH	7E6B	MISTATH	7E8B	ERXRDPTH
7E0C	EDMALENL	7E2C	EPMM3L	7E4C	Reserved	7E6C	EPAUSL	7E8C	ERXWRPTL
7E0D	EDMALENH	7E2D	EPMM3H	7E4D	Reserved	7E6D	EPAUSH	7E8D	ERXWRPTH
7E0E	EDMADSTL	7E2E	EPMM4L	7E4E	Reserved	7E6E	ECON2L	7E8E	EUDARDPTL
7E0F	EDMADSTH	7E2F	EPMM4H	7E4F	Reserved	7E6F	ECON2H	7E8F	EUDARDPTH
7E10	EDMACSL	7E30	EPMCSL	7E50	Reserved	7E70	ERXWML	7E90	EUDAWRPTL
7E11	EDMACSH	7E31	EPMCSH	7E51	Reserved	7E71	ERXWMH	7E91	EUDAWRPTH
7E12	ETXSTATL	7E32	EPMOL	7E52	MICMDL	7E72	EIEL	7E92	Reserved
7E13	ETXSTATH	7E33	EPMOH	7E53	MICMDH	7E73	EIEH	7E93	Reserved
7E14	ETXWIREL	7E34	ERXFCONL	7E54	MIREGADRL	7E74	EIDLEDL	7E94	Reserved
7E15	ETXWIREH	7E35	ERXFCONH	7E55	MIREGADRH	7E75	EIDLEDH	7E95	Reserved
7E16	EUDASTL	7E36	EUDASTL	7E56	EUDASTL	7E76	EUDASTL	7E96	Reserved
7E17	EUDASTH	7E37	EUDASTH	7E57	EUDASTH	7E77	EUDASTH	7E97	Reserved
7E18	EUDANDL	7E38	EUDANDL	7E58	EUDANDL	7E78	EUDANDL	7E98	Reserved
7E19	EUDANDH	7E39	EUDANDH	7E59	EUDANDH	7E79	EUDANDH	7E99	Reserved
7E1A	ESTATL	7E3A	ESTATL	7E5A	ESTATL	7E7A	ESTATL	7E9A	Reserved
7E1B	ESTATH	7E3B	ESTATH	7E5B	ESTATH	7E7B	ESTATH	7E9B	Reserved
7E1C	EIRL	7E3C	EIRL	7E5C	EIRL	7E7C	EIRL	7E9C	Reserved
7E1D	EIRH	7E3D	EIRH	7E5D	EIRH	7E7D	EIRH	7E9D	Reserved
7E1E	ECON1L	7E3E	ECON1L	7E5E	ECON1L	7E7E	ECON1L	7E9E	—
7E1F	ECON1H	7E3F	ECON1H	7E5F	ECON1H	7E7F	ECON1H	7E9F	—

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TABLE 3-3: ENC424J600/624J600 SFR MAP (BASE REGISTER MAP, 16-BIT PSP INTERFACE)

Addr	Name	Addr	Name	Addr	Name	Addr	Name	Addr	Name
3F00	ETXST	3F10	EHT1	3F20	MACON1	3F30	MAADR3	3F40	EGPDATA
3F01	ETXLLEN	3F11	EHT2	3F21	MACON2	3F31	MAADR2	3F41	ERXDATA
3F02	ERXST	3F12	EHT3	3F22	MABBIPG	3F32	MAADR1	3F42	EUDADATA
3F03	ERXTAIL	3F13	EHT4	3F23	MAIPG	3F33	MIWR	3F43	EGPRDPT
3F04	ERXHEAD	3F14	EPMM1	3F24	MACLCON	3F34	MIRD	3F44	EGPWRPT
3F05	EDMAST	3F15	EPMM2	3F25	MAMXFL	3F35	MISTAT	3F45	ERXRPT
3F06	EDMALEN	3F16	EPMM3	3F26	Reserved	3F36	EPAUS	3F46	ERXWRPT
3F07	EDMADST	3F17	EPMM4	3F27	Reserved	3F37	ECON2	3F47	EUDARDPT
3F08	EDMACS	3F18	EPMCS	3F28	Reserved	3F38	ERXWM	3F48	EUDAWRPT
3F09	ETXSTAT	3F19	EPMO	3F29	MICMD	3F39	EIE	3F49	Reserved
3F0A	ETXWIRE	3F1A	ERXFCON	3F2A	MIREGADR	3F3A	EIDLED	3F4A	Reserved
3F0B	EUDAST	3F1B	EUDAST	3F2B	EUDAST	3F3B	EUDAST	3F4B	Reserved
3F0C	EUDAND	3F1C	EUDAND	3F2C	EUDAND	3F3C	EUDAND	3F4C	Reserved
3F0D	ESTAT	3F1D	ESTAT	3F2D	ESTAT	3F3D	ESTAT	3F4D	Reserved
3F0E	EIR	3F1E	EIR	3F2E	EIR	3F3E	EIR	3F4E	Reserved
3F0F	ECON1	3F1F	ECON1	3F2F	ECON1	3F3F	ECON1	3F4F	—

3.2.4.1 PSP Bit Set and Bit Clear Registers

A major difference between the SPI and PSP memory maps is the inclusion of companion Bit Set and Bit Clear registers for many of the E registers. Since the PSP interface allows direct access to memory locations, without a command interpreter, there are no instructions implemented to perform single bit manipulations. Instead, this interface implements separate Bit Set and Bit Clear registers, allowing users to individually work with volatile bits (such as interrupt flags) without the risk of disturbing the values of other bits. Setting the bit(s) in one of these registers sets or clears the corresponding bit(s) in the base register.

In the PSP interface, Bit Set and Bit Clear registers are located in different areas of the addressable memory space from their corresponding “base” SFRs. The address of the registers is always at a fixed offset from their corresponding base register. For the 8-bit interface, the offset is 100h (Set) or 180h (Clear). For the 16-bit interface, the offset is 80H (Set) or C0 (Clear). Symbolically, the names of the companion registers are the names of the base registers, plus the suffix form “-SET” (or “-SETH/SETL”) for Bit Set registers and “-CLR” (“-CLR/CLRL”) for Bit Clear registers.

Most SFRs have their own pair of Bit Set and Bit Clear registers. However, these SFRs do not:

- MAC registers, including MI registers for PHY access
- Read-only status registers (ERXHEAD, ETXSTAT, ETXWIRE and ESTAT)
- All of the SRAM Buffer Pointers and data windows (SFRs located at 7E80h to 7E9Fh in the 8-bit interface, or 3F40h to 3F4Fh in the 16-bit interface)

The Bit Set and Bit Clear registers for the 8-bit PSP interface are listed in Table 3-4 and Table 3-5, respectively. The registers for the 16-bit interface are listed together in Table 3-6.

TABLE 3-4: ENC424J600/624J600 SFR MAP (SET REGISTER MAP, 8-BIT PSP INTERFACE)

Bit Set Registers (7F00h to 7F7Fh) ⁽¹⁾							
Addr	Name	Addr	Name	Addr	Name	Addr	Name
7F00	ETXSTSETL	7F20	EHT1SETL	7F40	Reserved	7F60	Reserved
7F01	ETXSTSETH	7F21	EHT1SETH	7F41	Reserved	7F61	Reserved
7F02	ETXLENSETL	7F22	EHT2SETL	7F42	Reserved	7F62	Reserved
7F03	ETXLENSETH	7F23	EHT2SETH	7F43	Reserved	7F63	Reserved
7F04	ERXSTSETL	7F24	EHT3SETL	7F44	Reserved	7F64	Reserved
7F05	ERXSTSETH	7F25	EHT3SETH	7F45	Reserved	7F65	Reserved
7F06	ERXTAILSETL	7F26	EHT4SETL	7F46	Reserved	7F66	Reserved
7F07	ERXTAILSETH	7F27	EHT4SETH	7F47	Reserved	7F67	Reserved
7F08	—	7F28	EPMM1SETL	7F48	Reserved	7F68	Reserved
7F09	—	7F29	EPMM1SETH	7F49	Reserved	7F69	Reserved
7F0A	EDMASTSETL	7F2A	EPMM2SETL	7F4A	Reserved	7F6A	Reserved
7F0B	EDMASTSETH	7F2B	EPMM2SETH	7F4B	Reserved	7F6B	Reserved
7F0C	EDMALENSETL	7F2C	EPMM3SETL	7F4C	Reserved	7F6C	EPAUSSETL
7F0D	EDMALENSETH	7F2D	EPMM3SETH	7F4D	Reserved	7F6D	EPAUSSETH
7F0E	EDMADSTSETL	7F2E	EPMM4SETL	7F4E	Reserved	7F6E	ECON2SETL
7F0F	EDMADSTSETH	7F2F	EPMM4SETH	7F4F	Reserved	7F6F	ECON2SETH
7F10	EDMACSSETL	7F30	EPMCSSETL	7F50	Reserved	7F70	ERXWMSETL
7F11	EDMACSSETH	7F31	EPMCSSETH	7F51	Reserved	7F71	ERXWMSETH
7F12	—	7F32	EPMOSETL	7F52	Reserved	7F72	EIESETL
7F13	—	7F33	EPMOSETH	7F53	Reserved	7F73	EIESETH
7F14	—	7F34	ERXFCONSETL	7F54	Reserved	7F74	EIDLEDSETL
7F15	—	7F35	ERXFCONSETH	7F55	Reserved	7F75	EIDLEDSETH
7F16	EUDASTSETL	7F36	EUDASTSETL	7F56	EUDASTSETL	7F76	EUDASTSETL
7F17	EUDASTSETH	7F37	EUDASTSETH	7F57	EUDASTSETH	7F77	EUDASTSETH
7F18	EUDANDSETL	7F38	EUDANDSETL	7F58	EUDANDSETL	7F78	EUDANDSETL
7F19	EUDANDSETH	7F39	EUDANDSETH	7F59	EUDANDSETH	7F79	EUDANDSETH
7F1A	—	7F3A	—	7F5A	—	7F7A	—
7F1B	—	7F3B	—	7F5B	—	7F7B	—
7F1C	EIRSETL	7F3C	EIRSETL	7F5C	EIRSETL	7F7C	EIRSETL
7F1D	EIRSETH	7F3D	EIRSETH	7F5D	EIRSETH	7F7D	EIRSETH
7F1E	ECON1SETL	7F3E	ECON1SETL	7F5E	ECON1SETL	7F7E	ECON1SETL
7F1F	ECON1SETH	7F3F	ECON1SETH	7F5F	ECON1SETH	7F7F	ECON1SETH

Note 1: Bit Set and Bit Clear registers are not implemented for the base SFRs located between 7E80h and 7E9Fh.