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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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PAN1321-SPP

Intel's
BlueMoonUniversal Platform

Wireless Modules

User's Manual

Hardware Description
Revision 3.3

Panasonic
ideas for life

Edition 2011-11-16

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ENW89811xxxF - Intel's BlueMoon™ Universal Platform

Revision History: 2011-11-16, Revision 3.3

Previous Version: 3.2

Page	Subjects (major changes since last revision)
Rev1.0	Initial version
Rev2.0	Due to better range with another ceramic antenna, we have updated module height from 1.8mm to 2.8mm. Changes made in **"Production Package" on Page 29** If you need smaller height, let us discuss your individual case.
Rev3.0	Releasing this document and correct the ordering code to ENW89811xxxF, which is the 85°C version
Rev3.1	Add the **Chapter 9**, Modified **Figure 6 "Package Marking" on Page 29** and **Figure 8 "Top View and Bottom View" on Page 30**
Rev3.2	Fixed all pins for the product life time in **Chapter 1.4**. Added **Table 2 "Firmware Releases as of 2011-11-16" on Page 13** and updated the **Chapter 12**.
Rev3.3	Updated the following:**Chapter 12** Added the following: **Chapter 4.3 "Apple® iPhone Support" on Page 16**, **Chapter 5 "Ordering Information" on Page 17**,

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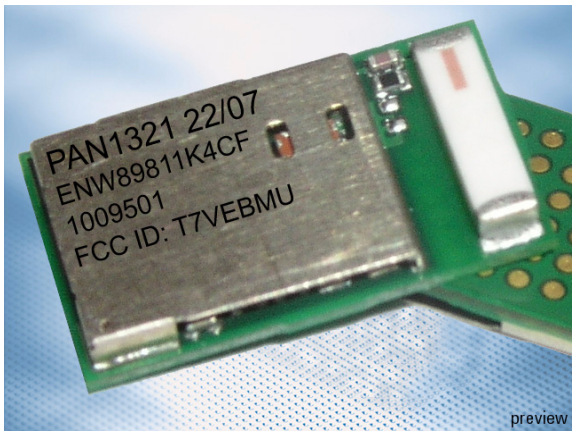

1.1 Features

General

- Complete Bluetooth 2.0 + EDR solution
  - Configurable for BT 1.2
- Ultra low power design in 0.13 µm CMOS
- Temperature range from -40°C to 85°C
- Integrates ARM7TDMI, RAM and patchable ROM
- On-module voltage regulators. External supply 2.9 - 4.1 V
- On-module EEPROM with configuration data
- Reference clock included
- Low power clock from internal oscillator or external low power clock (e.g. 32.768 kHz)
- Dynamic low power mode switching

Interfaces

- AT command interface over UART, configurable from 9600 baud up to 3.25 MBaud
- General purpose I/Os with interrupt capabilities. JTAG for boundary scan and debug

RF

- Transmit power typ. 2.5 dBm (default settings)
- Receiver sensitivity typ. -86 dBm
- Integrated antenna switch, balun and antenna filter
- Integrated LNA with excellent blocking and intermodulation performance
- No external components except antenna
- Digital demodulation for optimum sensitivity and co-/adjacent channel performance

Bluetooth

- Bluetooth V2.0 + EDR compliant
- SPP Device A and B support 1 ACL link with stream or command mode
- SPP Device A and B - Visible while connected
- SPP Device A and B - Visible/connectable when not connected
- SPP Device A and B - Device Discovery capable after receiving OK on data transfer
- Sniff mode is supported with above capabilities
- 5 trusted devices stored in EEPROM
- Testing
- Enable DUT
- Crystal calibration
- H4 with UART HW flow control (RTS/CTS)
- Security modes: Modes 1 and Mode 3
- Master-Slave role switch

1.2 Block Diagram

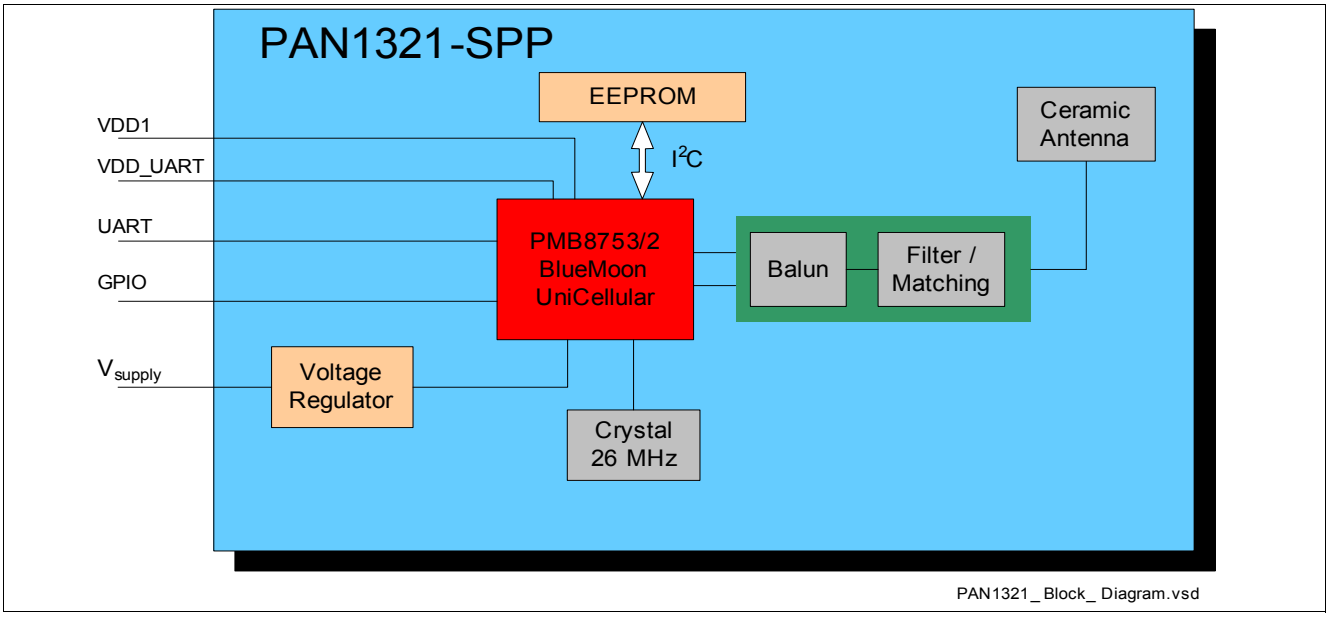

Figure 1 Simplified Block Diagram of PAN1321-SPP

1.3 Pin Configuration LGA

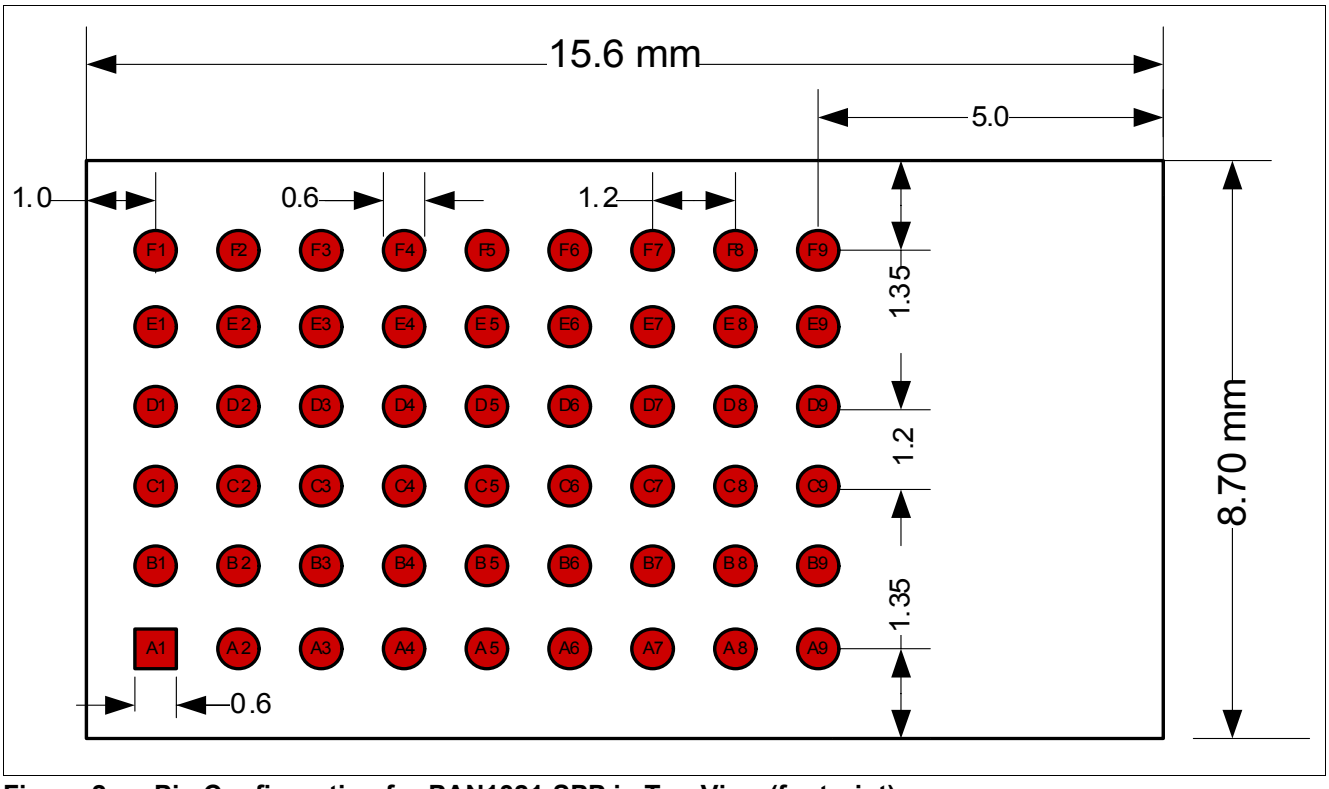

Figure 2 Pin Configuration for PAN1321-SPP in Top View (footprint)

1.4 Pin Description

All mentioned pins are fix for the product lifetime. Pins not listed below shall not be connected.

Table 1 Pin Description

Pin No.	Symbol	Input / Output	Supply Voltage	During Reset	After Reset	Function
A2	P1.6	I/O/OD	Internal1	Z	Z	Port 1.6
A3	RESET#	AI	Internal1	Input	Input	Hardware Reset, active low
A8	P1.5	I/O/OD	Internal1	Input	Input	Port 1.5
B1	P1.7	I/O/OD	Internal1	PD/ Input	PD/ Input	Port 1.7
B2	P1.8	I/O/OD	Internal1	PD	PD	Port 1.8
B3	P1.0 / TMS	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.0 or JTAG interface
B4	P1.4 / RTCK	I/O/OD	Internal2	Z	Z	Port 1.4 or JTAG interface
B5	ONOFF	I		-	-	Connect to VDD1 and refer to chapter 12 item [2].
B9	SLEEPX	I/O	VDDUART	PD	H	Sleep indication signal
C2	P0.9	I/O/OD	Internal2	Z	Z	Port 0.9
C3	JTAG#	I	Internal2	PU	PU	Mode selection Port 1: 0: JTAG 1: Port
C4	TRST#	I	Internal2	PD	PD	JTAG interface
D1	P0.10	I/O/OD	Internal2	Z	Z	Port 0.10
D2	P0.8	I/O/OD	Internal2	PD	PD	Port 0.8
D3	P1.1 / TCK	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.1 or JTAG interface
D4	P0.3	I/O/OD	VDD1	Conf. PD def.	Conf. PD def.	Port 0.3
D5	P0.2	I/O/OD	VDD1	Z	Z	Port 0.2
E1	P0.12 / SDA0	I/O/OD	Internal2	PU	PU	I2C data signal
E2	P0.13 / SCL0	I/O/OD	Internal2	PU	PU	I2C clock signal
E3	P1.3 / TDO	I/O/OD	Internal2	Z	Z	Port 1.3 or JTAG interface
E4	P0.0	I/O/OD	VDD1	PD	PD	Port 0.0 LPM wakeup output
E5	P0.1	I/O/OD	VDD1	PD	PD	Port 0.1
E6	P0.5 / UARTRXD	I/O/OD	VDDUART	Z	Z	Port 0.5 or UART receive data
F2	P1.2 / TDI	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.2 or JTAG interface
F3	P0.11	I/O/OD	Internal2	Z	Z	Port 0.11

Table 1 Pin Description

Pin No.	Symbol	Input / Output	Supply Voltage	During Reset	After Reset	Function
F4	P0.14	I/O	VDDUART	Z	Z	Port 0.14 LPM wakup input
F5	P0.7 / UARTCTS	I/O/OD	VDDUART	Z	Z	Port 0.7 or UART CTS flow control
F7	P0.4 / UARTTXD	I/O/OD	VDDUART	PU	PU	Port 0.4 or UART transmit data
F8	P0.6 / UARTRTS	I/O/OD	VDDUART	PU	PU	Port 0.6 or UART RTS flow control
A4, A5, A6	VSUPPLY	SI		-	-	Power supply
C1	VREG	SO		-	-	Regulated Power supply
F6	VDDUART	SI		-	-	UART interface Power supply
C5	VDD1	SI		-	-	Power supply
A1, A7, A9, C8, C9, D7, D8, E8, E9, F1, F9	VSS			-	-	Ground

1) Fixed pull-up/pull-down if JTAG interface is selected, not affected by any chip reset. If JTAG interface is not selected the port is tristate.

Descriptions of acronyms used in the pin list:

Acronym	Description
I	Input
O	Output
OD	Output with open drain capability
Z	Tristate
PU	Pull-up
PD	Pull-down
A	Analog (e.g. AI means analog input)
S	Supply (e.g. SO means supply output)

1.5 System Integration

PAN1321-SPP is optimized for a low bill of material (BOM) and a small PCB size. **Figure 3** shows a typical application example.

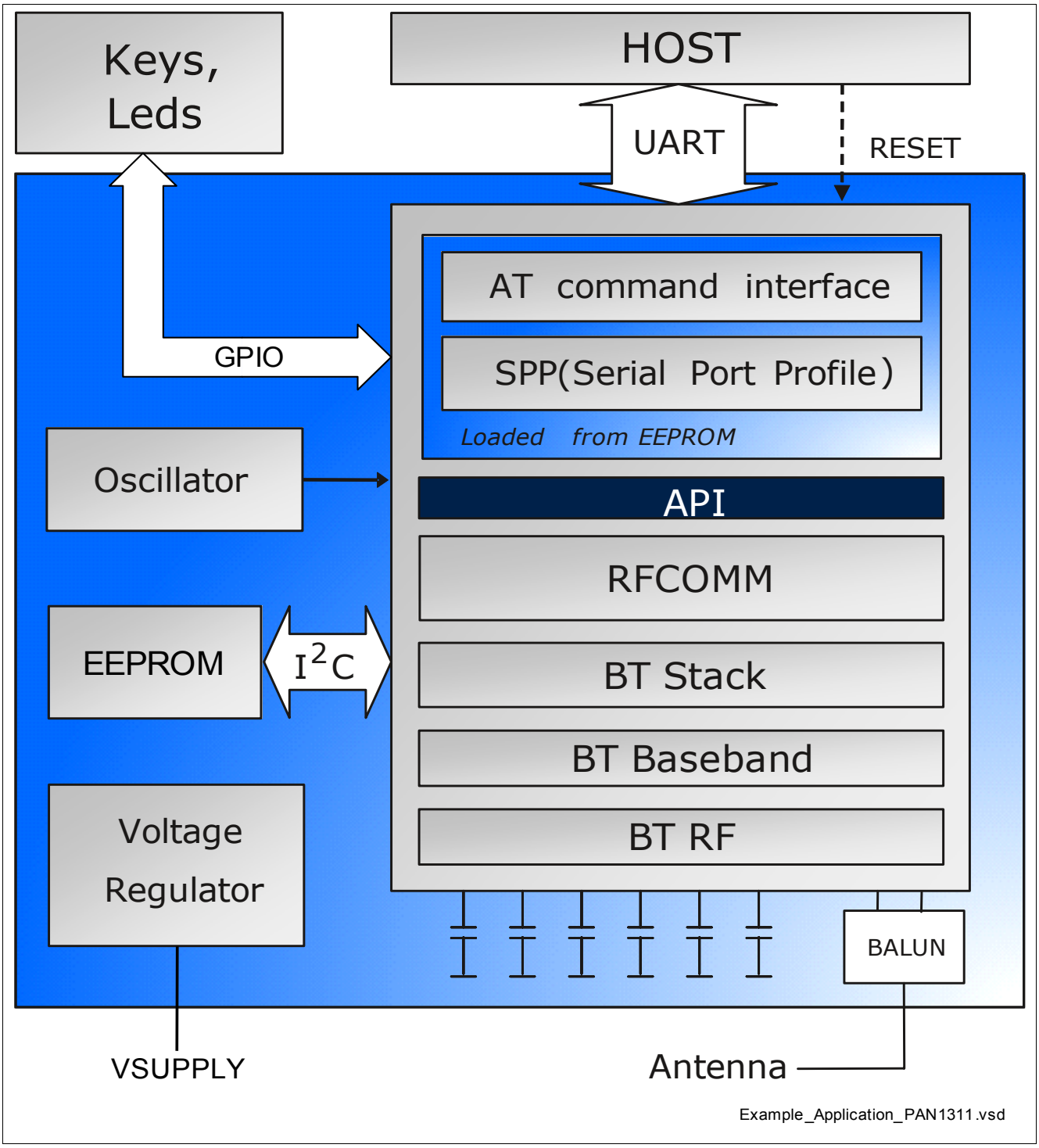

Figure 3 Example of a Bluetooth System using eUniStone

The UART interface is used for communication between the host and PAN1321-SPP. The lines UARTTXD and UARTRXD are used for commands, events and data. The lines UARTRTS and UARTCTS are used for hardware flow control.

Low power mode control of PAN1321-SPP and the host can be implemented in by using the pins P0.14 and P0.0. P0.14 is used by the host to allow PAN1321-SPP to enter low power mode and P0.0 is used by PAN1321-SPP to wake-up the host when attention is required. Additionally, the host could hardware reset PAN1321-SPP using the RESET# pin.

Power is supplied to a single VSUPPLY input from which internal regulators can generate all required voltages. The UART and the GPIO's interfaces have separate supply voltages so that they can comply with host signaling.

1.6 FW version

PAN1321-SPP is available in different firmware (FW) versions. Please check corresponding release documents for latest information in chapter **12** item **[1]**.

The identifier about the software version will be visible on the module, please refer to **Figure 6**, here it is the identifier SW.

There are actual 4 different firmware releases available in **Table 2**

Table 2 Firmware Releases as of 2011-11-16

SW (marking on the module)	FW (firmware version)	Comment
07	1.6	first standard release, free of charge
08	1.8	second standard release, free of charge, should be used for new projects
20	2.0	first iPhone release, special license fee is needed
21	2.1	second iPhone release, special license fee is needed, should be used for new projects

2 Basic Operating Information

2.1 Power Supply

PAN1321-SPP is supplied from a single supply voltage VSUPPLY. This supply voltage must always be present. The PAN1321-SPP chip is supplied from an internally generated 2.5 V supply voltage. This voltage can be accessed from the VREG pin. This voltage may not be used for supplying other components in the host system but can be used for referencing the host interfaces.

The GPIO's and the UART interface are supplied with dedicated, independent, reference levels via the VDD1 and VDDUART pins. All other digital I/O pins are supplied internally by either 2.5 V (Internal2) or 1.5 V (Internal1). **Section 1.4** provides a mapping between pins and supply voltages.

The I/O power domains (VDD1 and VDDUART) are completely separated from the other power domains and can stay present also in low power modes.

2.2 Clocking

PAN1321-SPP contains a crystal from which the internal 26 MHz system clock is generated. Also, the low power mode clock of 32 kHz is generated internally, which means that no external clock is needed.

3 Interfaces

3.1 UART Interface

The UART interface is the main communication interface between the host and PAN1321-SPP.

The interface consists of four UART signals and two wake-up signals as shown in **Figure 4**.

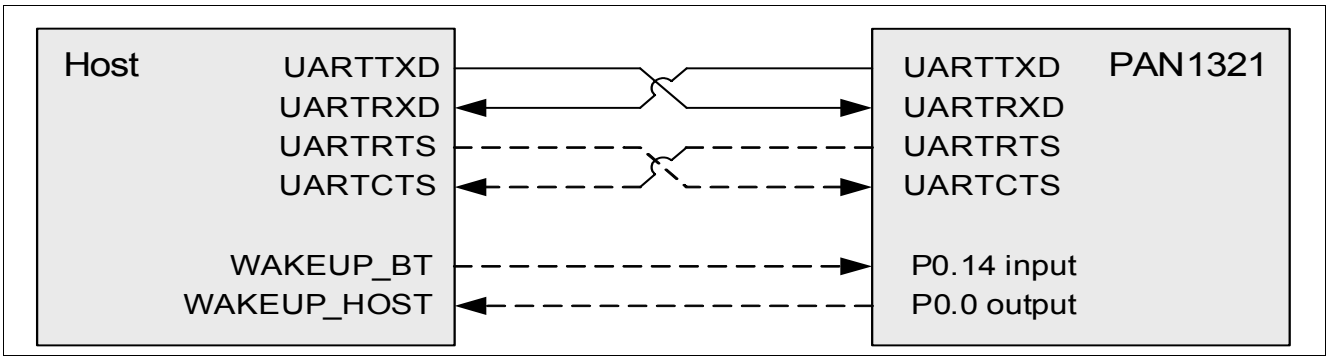

Figure 4 UART Interface

3.1.1 UART

The UART (Universal Asynchronous Receiver and Transmitter) interface is compatible with standard UART H4 (4-wire). The lines UARTTXD and UARTRXD are used for commands, events and data. The lines UARTRTS and UARTCTS are used for hardware flow control. A separate supply voltage, VDDUART, makes it easy to connect the UART interface to any system.

3.1.1.1 Baud Rates

The supported baud rates are listed in **Table 3** together with the small deviation error that results from the internal clock generation. The default baud rate is 115200 Baud.

Table 3 UART Baud Rates

Wanted Baud Rate	Real Baud Rate	Deviation Error (%)
9600	9615	0.16
19200	19230	0.16
38400	38461	0.16
57600	57522	-0.14
115200	115044	-0.14
230400	230088	-0.14
460800	464285	0.76
921600	928571	0.76
1843200	1857142	0.76
3250000	3250000	0

4 General Device Capabilities

This chapter describes features available in the PAN1321 (ENW89811xxxF) core.

Actual feature set and how to access the features can be found in the AT Command document [1]. Release specific performance characteristics, like data speed, is related in the SW Release Notes [1].

4.1 HCI+

The PAN1321 module can be programmed over UART with a specific application for RF test purposes, like TX continuous or TX burst mode. This test application is controlled over the UART through Infineon specific HCI commands. The commands supported by this test application are described in the document “T8753-2-Infineon_Specific_HCI_Commands-7600.pdf”.

4.2 Firmware ROM Patching

In any chip with complex firmware in ROM it is wise to support patching. The risk of project delay is significantly reduced when problems can be solved without hardware changes. Enhancements, adaptations and bug fixes can be handled very late during design-in, even after the PAN1321 has been soldered in the final product.

The well-proven patch concept used in PAN1321 is described below.

4.2.1 Patch Support

PAN1321-SPP contains dedicated hardware that makes it possible to apply patches to the code and data in the firmware ROM. The hardware is capable of replacing up to 32 blocks of 16 bytes each with new content. This area can be filled with any combination of code and data. The firmware patch is stored in EEPROM and automatically loaded after startup. This provides a flexible bugfix solution for the ROM part of the firmware.

4.3 Apple® iPhone Support

The PAN1311i and PAN1321i support Bluetooth Apple iPhone connectivity.

An Apple® authentication IC is required to exchange data with an Apple® Device or access an Apple® Device application. The Bluetooth SPP profile capable of recognizing the Apple® authentication chip, along with the Bluetooth stack is stored and runs on the PAN1311i/1321i.

Customers using the Apple® authentication IC must register as developer, to become an Apple® certified MFI member. License fees may apply, for additional information visit:
http://developer.apple.com/programs/which-program/index.html

Certified MFI developers receive technical specifications describing the iPod® Accessory protocol, the communication protocol used to interact with iPod®, iPhone® and iPad®. Developers also gain access to the ordering information of the hardware connectors and components that are required to manufacture iPod®, iPhone®, and iPad® accessories.

4.3.1 Apple® Authentication Chip

The below **Figure 5** will give a rough overview how the hardware concept looks like, in addition the init commands are shown to establish a link between PAN1311i/1321i and the Apple® Device.

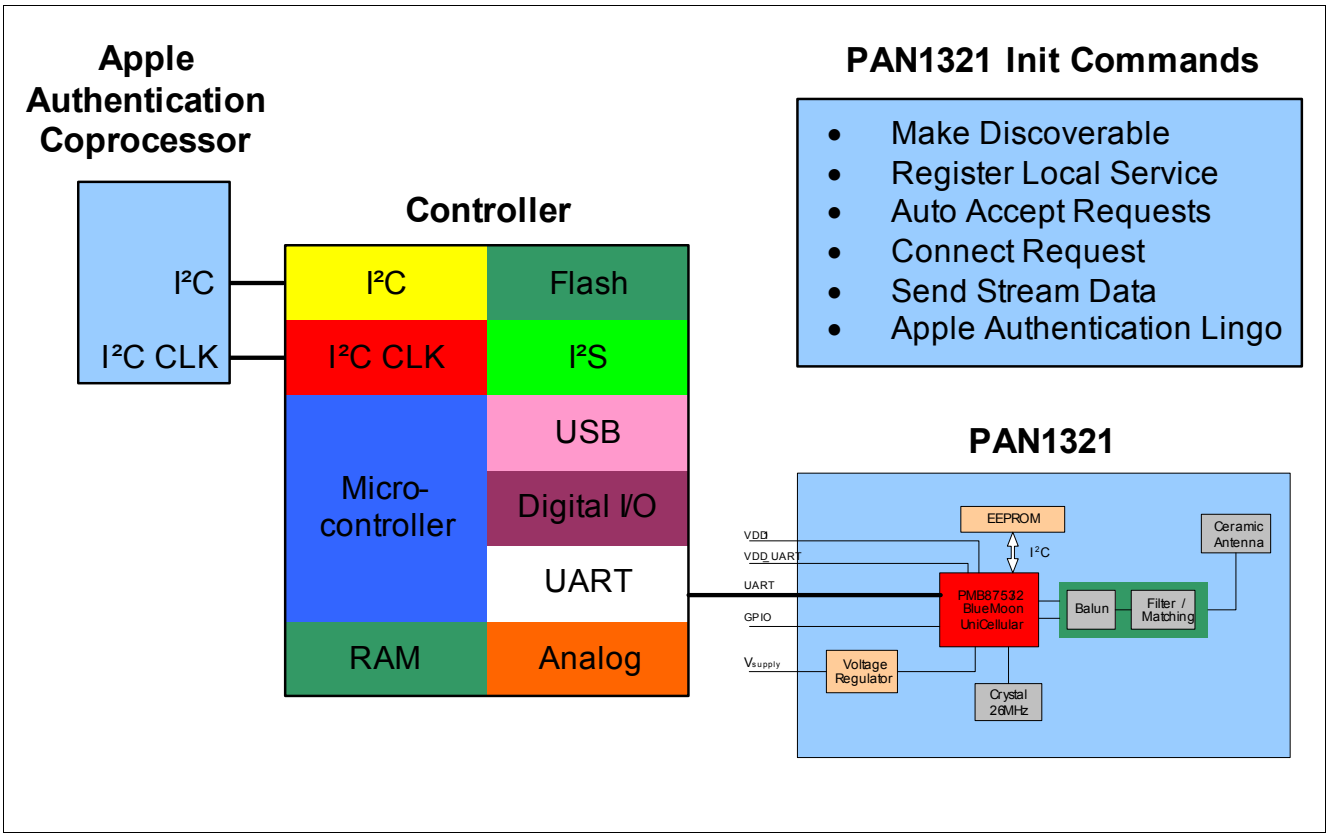

Figure 5 Simplified Block Diagram, when using an Apple Authentication Chip

5 Ordering Information

This chapter shows the different order codes for the PAN1321-SPP. In case, there is no specific software version mentioned in the order, we will always deliver the latest official software release, which is downwards compatible. Please refer also to **Table 2 “Firmware Releases as of 2011-11-16” on Page 13**.

Table 4 Order Code as of 2011-11-16

Order Code	Description	MOQ 1)
ENW89811K4CF	PAN1321-SPP Bluetoth 2.0 Module with integrated Antenna and a standard SPP software.	1500
ENW89811A6KF	PAN1321-SPP Bluetoth 2.0 Module with integrated Antenna and a spezial SPP software, which supports Apples iPhone®	1500

1) Abbreviation for Minimum Order Quantity (MOQ). The standard MOQ for mass production are 1500 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity.

6 Bluetooth Capabilities

6.1 Supported Features

- Bluetooth V2.0 + EDR compliant
- Enhanced Data Rate up to 3 Mbit/s
- Adaptive Frequency Hopping (AFH)
- All packet types
- Authentication, Pairing and Encryption
- SPP Device A and B support 1 ACL link with stream or command mode
- SPP Device A and B - Visible while connected
- SPP Device A and B - Visible/connectable when not connected
- SPP Device A and B - Device Discovery capable after receiving OK on data transfer
- Sniff mode is supported with above capabilities
- 5 trusted devices stored in EEPROM
- Enable DUT
- Crystal calibration
- H4 with UART HW flow control (RTS/CTS)
- Security modes: Modes 1 and Mode 3
- Master-Slave role switch
- Quality of Service
- Channel Quality Driven Data Rate change
- Sniff, Hold
- Role Switch
- RSSI and Power Control
- Power class 2 and 3
- Standard Bluetooth test mode, Active Tester Mode and RF Test Modes

6.2 PAN1321-SPP Specifics and Extensions

6.2.1 During Connection

6.2.1.1 Role Switch

Only one role switch can be performed at a time. If a role switch request is pending, other role switch requests on the same or other links are rejected. If a role switch fails, PAN1321-SPP will automatically try again a maximum of three times. Encryption (if present) is stopped in the old piconet before a role switch is performed and re-enabled when the role switch has succeeded or failed.

6.2.1.2 Dynamic Polling Strategy

In addition to the regular polling scheme, PAN1321-SPP dynamically assigns unused slots to links where data is exchanged. This adapts very well to bursty traffic and improves throughput and latency on the links.

6.2.1.3 Adaptive Frequency Hopping (AFH)

PAN1321-SPP supports adaptive frequency hopping according to the Bluetooth 2.0 + EDR specification. AFH switch and channel classification are supported both as master and slave. Channel classification from the host is also supported.

A number of HCI+ commands and events are available to provide information about AFH operation. The commands Infineon_Enable_AFH_Info_Sending and Infineon_Disable_AFH_Info_Sending turn on and off the Infineon AFH Info events that provide detailed information about channel classification, channel maps, interferers, etc.

If enabled by the Infineon_Enable_Infineon_Events command, the Infineon AFH Extraordinary RSSI event informs the host whenever extraordinary RSSI measurements in unused slots have been started. This is done when the number of known good channels has decreased below a critical limit and periodically after a defined time.

The Infineon_Set_AFH_Measurement_Period command can be used to configure the duration of the AFH measurement period.

6.2.1.4 Channel Quality Driven Data Rate Change (CQDDR)

PAN1321-SPP supports channel quality driven data rate change according to the Bluetooth 2.0 + EDR specification. A device that receives an LMP_preferred_rate message is not required to follow all recommendations. PAN1321-SPP normally at least follows the recommendation whether to use forward error correction (FEC) or not. If possible, recommendations about packet size and modulation scheme will be taken into account. When PAN1321-SPP sends an LMP_preferred_rate to another device the proposal always includes preferences for all parameters.

The HCI+ commands Infineon_Enable_CQDDR_Info_Sending and Infineon_Disable_CQDDR_Info_Sending turn on and off sending of the Infineon CQDDR Info event. This event provides information to the host every time a new CQDDR proposal is sent to a remote device.

6.2.2 RSSI and Output Power Control

6.2.2.1 Received Signal Strength Indication (RSSI)

PAN1321-SPP supports received signal strength measurements and uses LMP signaling to keep the output power of a remote device within the golden receive power range. The range is set with the BD_DATA parameters RSSI_Min and RSSI_Max.

6.2.2.2 Output Power Control

PAN1321-SPP supports power control according to the Bluetooth 2.0+EDR specification.

- The output power can be controlled in up to 4 configurable steps. PAN1321-SPP can work as a class 2 or 3 device, depending on the settings.
- Fine tuning can be used on the power steps.
- A default sub-state power step can be set

The power step configuration is set through BD_DATA parameters.

The Inquiry output power can be programmed with the Write Inquiry Transmit Power Level command introduced in the 2.0 Bluetooth Core specification.

6.2.2.3 Ultra Low Transmit Power

For high security devices the output power can be reduced to a value that reduces the communication range to a few inches. This mode is enabled with the HCI+ command Infineon_TX_Power_Config.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature		-40	–	125	°C	–
VSUPPLY supply voltage		-0.3	–	6.0	V	–
VDDUART supply voltage		-0.9	–	4.0	V	–
VDD1 supply voltage		-0.9	–	4.0	V	–
VREG		-0.3	–	4.0	V	VSUPPLY > 4 V
VREG		-0.3	–	VSUPPLY	V	VSUPPLY < 4 V
ONOFF		-0.3	–	VSUPPLY+0.3	V	
Input voltage range		-0.9	–	4.0	V	–
Output voltage range		-0.9	–	4.0	V	-9
ESD		–	–	1.0	kV	According to MIL-STD883D method 3015.7

Note: Stresses above those listed here are likely to cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.
Maximum ratings are not operating conditions.

7.2 Operating Conditions

Table 6 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operating temperature		-40	–	85	°C	–
Main supply voltage (Vsupply)		2.9	–	4.1	V	–
VDDUART		1.35	–	3.6	V	–
VDD1		1.35	–	3.6	V	–

7.3 DC Characteristics

7.3.1 Pad Driver and Input Stages

For more information, see **Chapter 1.4**.

Table 7 Internal1 (1.5 V) Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.27	V	–
Input high voltage		1.15	–	3.6	V	–
Output low voltage		–	–	0.25	V	IOL = 1 mA
Output high voltage		1.1	–	–	V	IOH = -1 mA
Continuous Load[1)]		–	–	1	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all Internal1 supplied pins shall not exceed 2mA at the same time

Table 8 Internal2 (2.5 V) Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.45	V	–
Input high voltage		1.93	–	2.8	V	P0.10
Input high voltage		1.93	–	3.6	V	Other pins
Output low voltage		–	–	0.25	V	IOL = 5 mA
Output low voltage		–	–	0.15	V	IOL = 2 mA
Output high voltage		2.0	–	–	V	IOH = -5 mA
Output high voltage		2.1	–	–	V	IOH = -2 mA
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all Internal2 supplied pins shall not exceed 35 mA at the same time

Table 9 VDDUART Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.2*VDDUART	V	–
Input high voltage		0.7*VDDUART	–	VDDUART+0.3	V	P0.5/UARTRXD
Input high voltage		0.7*VDDUART	–	3.6	V	Other pins

Table 9 VDDUART Supplied Pins (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output low voltage		–	–	0.25	V	IOL = 5 mA VDDUART = 2.5 V
Output low voltage		–	–	0.15	V	IOL = 2 mA VDDUART = 2.5 V
Output high voltage		VDDUART -0.25	–	–	V	IOH = -5 mA VDDUART = 2.5 V
Output high voltage		VDDUART -0.15	–	–	V	IOH = -2 mA VDDUART = 2.5 V
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all VDDUART supplied pins shall not exceed 35 mA at the same time

Table 10 VDD1 Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.2*VDD1	V	–
Input high voltage		0.7*VDD1	–	3.6	V	–
Output low voltage		–	–	0.25	V	IOL = 5 mA VDD1 = 2.5 V
Output low voltage		–	–	0.15	V	IOL = 2 mA VDD1 = 2.5 V
Output high voltage		VDD1 -0.25	–	–	V	IOH = -5 mA VDD1 = 2.5 V
Output high voltage		VDD1 -0.15	–	–	V	IOH = -2 mA VDD1 = 2.5 V
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all VDD1 supplied pins shall not exceed 35 mA at the same time

Table 11 ONOFF PIN

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		–	–	0.7	V	–
Input high voltage		1.7	–	VSUPPLY	V	–
Input current		-1	0.01	1	µA	ONOFF = 0 V

7.3.2 Pull-ups and Pull-downs

Table 12 Pull-up and Pull-down Currents

Pin	Pull Up Current			Pull Down Current			Unit	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
P0.12 P0.13	260	740	1300	N/A	N/A	N/A	µA	Pull-up current measured with pin voltage = 0 V Pull-down current measured with pin voltage = supply voltage Min measured at 125°C with supply = 1.35 V Typ. measured at 27°C with supply = 2.5V Max measured at -40°C with supply = 3.63 V
P0.0 P0.1 P0.2 P0.3	22	130	350	23	150	380	µA	
P0.4 P0.5 P0.6 P0.7 P0.10 P0.8 P0.9 P0.11 P0.14 P0.15	4.2	24	68	3.0	20	55	µA	
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7 P1.8	1.1	6.0	17	0.75	5.0	14	µA	

7.3.3 Protection Circuits

All pins have an inverse protection diode against VSS.
P0.10 has an inverse diode against Internal2.
P0.5/UARTRXD has an inverse diode against VDDUART.
All other pins have no diode against their supply.

7.3.4 System Power Consumption

Table 13 Max. Load at the Different Supply Voltages

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Vsupply		–	–	100	mA	Peak current

Note: I/O currents are not included since they depend mainly on external loads.

7.4 AC Characteristics

7.5 RF Part

7.5.1 Characteristics RF Part

The characteristics involve the spread of values to be within the specific temperature range. Typical characteristics are the median of the production.

All values refers to Infineon reference design. All values will be updated after verification/Characterisation.

7.5.1.1 Bluetooth Related Specifications

Table 14 BDR - Transmitter Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output power (high gain)		0.5	2.5	4.5	dBm	Default settings
Output power (highest gain)		–	4.5	–	dBm	Maximum settings
Power control step size		4	6	8	dB	–
Frequency range fL		2400	2401.3	–	MHz	–
Frequency range fH		–	2480.7	2483.5	MHz	–
20 dB bandwidth		–	0.930	1	MHz	–
2nd adjacent channel power		–	-40	-20	dBm	–
3rd adjacent channel power		–	-60	-40	dBm	–
>3rd adjacent channel power		–	-64	-40	dBm	Max. 2 of 3 exceptions @ 52 MHz offset might be used
Average modulation deviation for 00001111 sequence		140	156	175	kHz	–
Minimum modulation deviation for 01010101 sequence		115	145	–	kHz	–
Ratio Deviation 01010101 / Deviation 00001111		0.8	1	–		–
Initial carrier frequency tolerance |foffset|		–	–	75	kHz	–