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Product Specification

Applicant / Manufacturer Hardware	Panasonic Industrial Devices Europe GmbH Zeppelinstrasse 19 21337 Lüneburg Germany
Applicant / Manufacturer Software	Not applicable
Software Version	Not applicable
Contents	Approval for Mass Production
Customer	
Bluetooth QDL ID	Qualified Design Listing (QDL) ID: B019784 As Controller Sub-System Listing for PAN13xx Series.

By purchase of any products described in this document the customer accepts the document's validity and declares their agreement and understanding of its contents and recommendations. Panasonic reserves the right to make changes as required without notification.

TABLE OF CONTENTS

1 SCOPE OF THIS DOCUMENT

This product specification describes Panasonic's HCI, Class 1.5 , TI based, Bluetooth®[1] modules, series number 13xx.

For detailed family overview that includes part numbers see Chapter 29, Ordering Information.

Non-antenna versions will be refered to as PAN131x, versions with antenna will be refered to as PAN132x in this document.

For information and features on Bluetooth Low Energy 4.0 refer to Chapter 20, for information on ANT refer to Chapter 22.

1.1 NEW PAN13X5B, PAN13X6B

The PAN13x5B and PAN13x6B Series are based on Texas Instruments' NEW CC2560B and CC2564B controller respectively. The NEW PAN13x5B/13x6B Series Modules support assisted mode for the HFP1.6 (WBS) profile or the A2DP profile. The PAN13x6B also supports 10 LE connections (instead of 6 before).

Compatibility:

PAN1315(A/B) and PAN1316(B) are 100% footprint compatible

PAN1325(A/B) and PAN1326(B) are 100% footprint compatible

NOTE: In the following chapters PAN13x5, PAN13x6 naming also considers the A and B version.

As an updated initialization script resident on the application microcontroller is required for modules based on the CC2560B and CC2564B, compatibility between the basic, A and B version is dependent on the Bluetooth stack.

BT-Stack solutions provided by software development partners are available for most processors, including linux based host systems.

For detailed family overview that includes part numbers see Chapter 29 Ordering Information.

Contact your stack provider or local Panasonic sales company for currently available Bluetooth Profiles.

[1] Bluetooth is a registered trademark of the Bluetooth Special Interest Group.

2 KEY FEATURES

- Bluetooth specification v2.1 + EDR (**E**nhanced **D**ata **R**ate)
- Surface mount type 6.5(9.5 w. Ant.) x 9.0 x 1.8 mm^3
- Up to 10 dBm Tx power with transmit power control
- High sensitivity (-93 dBm typ.)
- Texas Instrument's CC256X BlueLink 7.0 inside
- Fast Connection Setup
- Extended SCO Link
- Supports convenient direct connection to battery (2.2-4.8 V), or connect to DC/DC (1.7-1.98 V) for improved power efficiency
- Internal crystal oscillator (26MHz)
- Fully shielded for immunity
- Full Bluetooth data rate up to 2,178kbps asymmetric
- Support for Bluetooth power saving modes (Sniff, Hold)
- Support for very low-power modes (deep sleep and power down)
- Optional support for ultra-low-power mode. Standby with Battery-Backup
- PCM Interface Master / Slave supporting 13 or 16 bit linear, 8 bit µ-law or A-law Codecs and CVSD transcoders on up to 3 SCO channels
- Full 8- to 128-bit encryption
- UART, I^2C and PCM Interface
- IO operating voltage = 1.8 V nominal
- Bluetooth profiles such as SPP, A2DP and others are available. Refer to Panasonic's RF module website for a listing of the most current releases.
- Manufactured in conformance with RoHS

3 APPLICATIONS FOR THE MODULE

All Embedded Wireless Applications

- Smart Phones
- Industrial Control
- Medical
- Scanners
- Wireless Sensors
- Low Power
- Cable Replacement
- Automotive
- Access Points
- Consumer Electronics
- Monitoring and Control
- Access Points

4 DESCRIPTION FOR THE MODULE

The PAN1315 and PAN1315A are short-range, Class 1 or 2, HCI modules for implementing Bluetooth functionality into various electronic devices. A block diagram can be found in Chapter 7.

Communication between the module and the host controller is carried out via UART.

New designs can be completed quickly by mating the PAN13xx series modules with Texas Instruments' MSP430BT5190 that contains Mindtree's EtherMind Bluetooth Protocol Stack and serial port profile, additional computing power can be achieved by choosing TI's Stellaris ARM7 controller that includes StoneStreet One's A2DP profile. Other BT profiles are available on custom development basis.

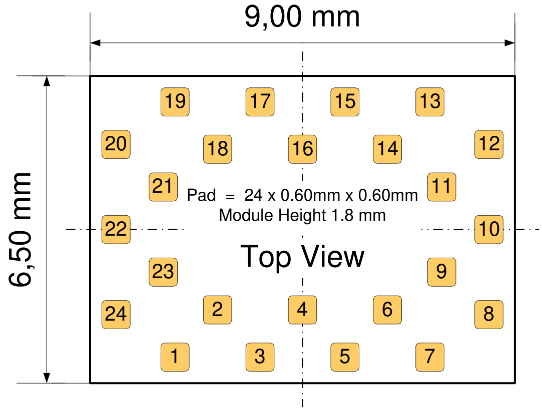
Additional controllers are also supported by the PAN13xx series by using a TI/Panasonic software development partner to port the Bluetooth stack and profiles. Mindtree's Software Development Kit (SDK) is available on TI's website -- www.ti.com/connectivity.com

Contact your local sales office for further details on additional options and services, by visiting www.panasonic.com/rfmodules or write an e-mail to wireless@eu.panasonic.com.

5 DETAILED DESCRIPTION

5.1 TERMINAL LAYOUT

5.1.1 5.1.1. Terminal Layout PAN131x without antenna



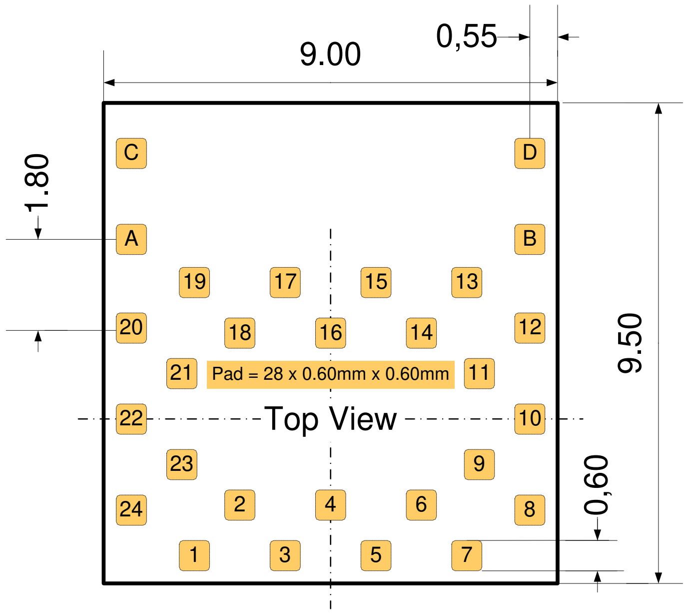
No	Pin Name	Pull at Reset	Def. Dir. [2]	I/O Type [3]	Description of Options (Common)
1	GND				Connect to Ground
2	TX_DBG	PU	O	2 mA	Logger output
3	HCI_CTS	PU	I	8 mA	HCI UART clear-to-send.
4	HCI_RTS	PU	O	8 mA	HCI UART request-to-send.
5	HCI_RX	PU	I	8 mA	HCI UART data receive
6	HCI_TX	PU	O	8 mA	HCI UART data transmit
7	AUD_FSYNC	PD	IO	4 mA	PCM frame synch. (NC if not used) Fail safe[4]
8	SLOW_CLK_IN		I		32.768-kHz clock in Fail safe
9	NC		IO		Not connected
10	MLDO_OUT		O		Main LDO output (1.8 V nom.)
11	CL1.5_LDO_IN		I		PA LDO input
12	GND				Connect to Ground
13	RF		IO		Bluetooth RF IO
14	GND				Connect to Ground
15	MLDO_IN		I		Main LDO input
16	nSHUTD	PD	I		Shutdown input (active low).
17	AUD_OUT	PD	O	4 mA	PCM data output. (NC if not used) Fail safe
18	AUD_IN	PD	I	4 mA	PCM data input. (NC if not used) Fail safe
19	AUD_CLK	PD	IO	HY, 4 mA	PCM clock. (NC if not used) Fail safe
20	GND				Connect to Ground
21	NC				EEPROM I²C SDA (Internal)
22	VDD_IO		PI		I/O power supply 1.8 V Nom
23	NC				EEPROM I²C SCL (Internal)
24	NC		IO		Not connected

[2] I = input; O = output; IO = bidirectional; P = power; PU = pulled up; PD = pulled down

[3] I/O Type: Digital I/O cells. HY = input hysteresis, current = typ. output current

[4] No signals are allowed on the IO pins if no VDD_IO (Pin 22) power supplied, except pin 7, 8, 17-19.

5.1.2 5.1.2. Terminal Layout PAN132x with antenna



No	Pin Name	Pull at Reset	Def. Dir. [5]	I/O Type [6]	Description of Options (Common)
A	GND				Connect to Ground
B	GND				Connect to Ground
C	GND				Connect to Ground
D	GND				Connect to Ground

No 1-24 see above in Chapter 5.1.1. Except PIN 13 is not connected. For RF conducted measurements, either use the PAN1323ETU or de-solder the antenna and solder an antenna connector to the hot pin.

[5] I = input; O = output; IO = bidirectional; P = power; PU = pulled up; PD = pulled down

[6] I/O Type: Digital I/O cells. HY = input hysteresis, current = typ. output current

5.2 PIN DESCRIPTION

Pin Name	No	ESD [7] (V)	Pull at Reset	Def. Dir. [8]	I/O Type [9]	Description of Options
Bluetooth IO SIGNALS						
HCI_RX	5	750	PU	I	8 mA	HCI UART data receive
HCI_TX	6	750	PU	O	8 mA	HCI UART data transmit
HCI_RTS	4	750	PU	O	8 mA	HCI UART request-to-send.
HCI_CTS	3	750	PU	I	8 mA	HCI UART clear-to-send.
AUD_FYSNC	7	500	PD	IO	4 mA	PCM frame synch (NC if not used) Fail safe
AUD_CLK	19	500	PD	IO	HY, 4 mS	PCM clock (NC if not used) Fail safe
AUD_IN	18	500	PD	I	4 mA	PCM data input (NC if not used) Fail safe
AUD_OUT	17	500	PD	O	4 mA	PCM data output (NC if not used) Fail safe
TX_DBG	2	1000	PU	O	2 mA	Logger output OPTION: nTX_DBG – logger out (low = 1)
CLOCK SIGNALS						
SLOW_CLK_IN	8	1000		I		32.768-kHz clock in Fail safe
Bluetooth ANALOG SIGNALS						
RF	13	1000		IO		Bluetooth RF IO (not connected with antenna)
nSHUTD	16	1000	PD	I		Shutdown input (active low).
Bluetooth POWER AND GND SIGNALS						
VDD_IO	22	1000		PI		I/O power supply 1.8 V Nom
MLDO_IN	15	1000		I		Main LDO input Connect directly to battery or to a pre-regulated 1.8-V supply
MLDO_OUT	10	1000		O		Main LDO output (1.8 V nom.) Can not be used as 1.8V supply due to internal connection to the RF part.
CL1.5_LDO_IN	11	1000		I		PA LDO input Connect directly to battery or to a pre-regulated 1.8-V supply
GND	1			P		Connect to Ground
GND	12			P		Connect to Ground
GND	14			P		Connect to Ground
GND	20			P		Connect to Ground
EEPROM IO SIGNALS (EEPROM is optional in PAN13x product line)						
NC	23	1000	PU/PD	I	HY, 4mA	EEPROM I²C SCL (Internal)
NC	21	1000	PU/PD	IO	HY, 4mA	EEPROM I²C IRQ (Internal)

Remark:

HCI_CTS is an input signal to the CC256X device:

- When HCI_CTS is low, then CC256X is allowed to send data to Host device.
- When HCI_CTS is high, then CC256X is not allowed to send data to Host device.

[7] ESD: Human Body Model (HBM). JEDEC 22-A114

[8] I = input; O = output; IO = bidirectional; P = power; PU = pulled up; PD = pulled down

[9] I/O Type: Digital I/O cells. HY = input hysteresis, current = typ output current

5.3 DEVICE POWER SUPPLY

The PAN13XX Bluetooth radio solution is intended to work in devices with a limited power budget such as cellular phones, headsets, hand-held PC's and other battery-operated devices. One of the main differentiators of the PAN13XX is its power management – its ability to draw as little current as possible.

The PAN13XX device requires two kinds of power sources:

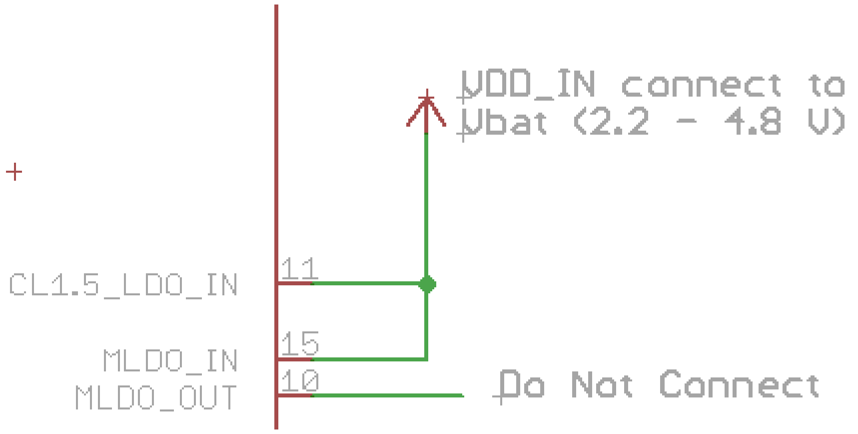
- Main power supply for the Bluetooth - VDD_IN = V_{BAT}
- Power source for the 1.8 V I/O ring - VDD_IO

The PAN13XX includes several on-chip voltage regulators for increased noise immunity. The PAN13XX can be connected either directly to the battery or to an external 1.8-V DC to DC converter.

There are three ways to supply power:

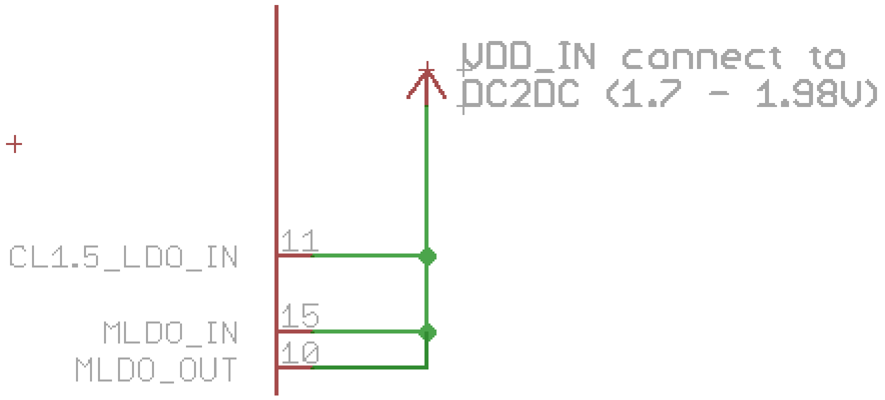
- Full-V_{BAT} system:

Maximum RF output power, but not optimum system power:



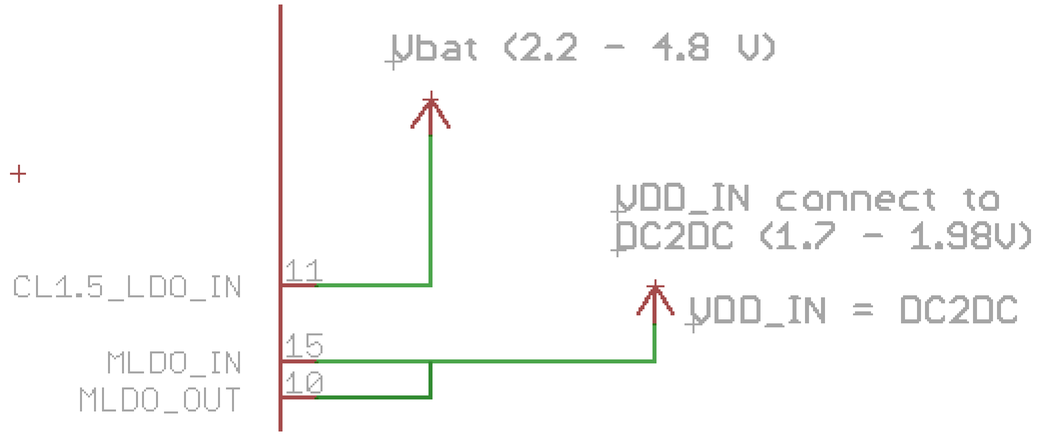
- Full-DC2DC system:

Lower RF output power, but optimum system power:



- Mixed DC2DC-V_{BAT} system:

Maximum RF output power and optimum system power, but requires routing of V_{BAT}:



5.4 CLOCK INPUTS

The slow clock is always supplied from an external source. It is connected to the SLOW_CLK_IN pin number 8 and can be a digital signal with peak to peak of 0-1.8 V.

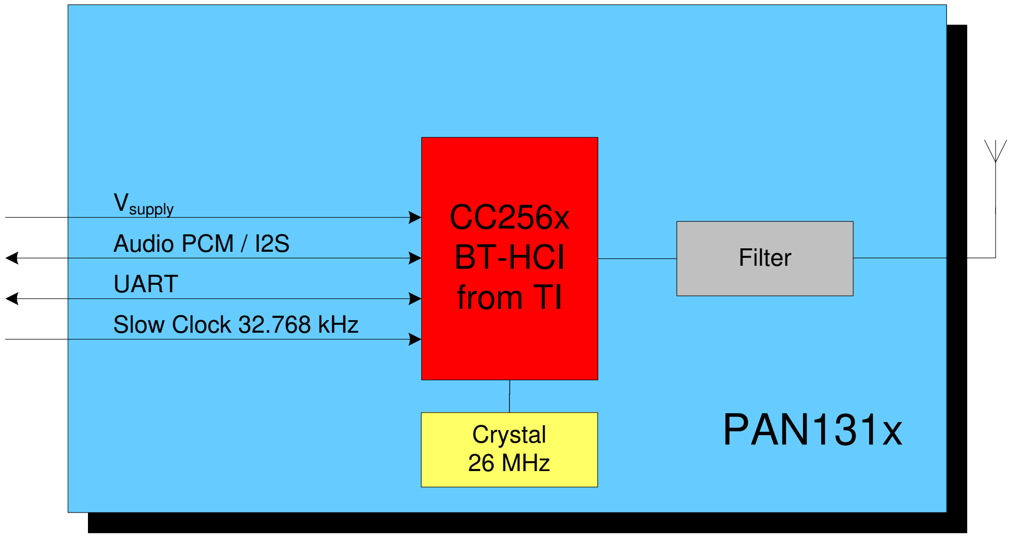
The slow clock's frequency accuracy must be 32.768 kHz ±250 ppm for Bluetooth usage (according to the Bluetooth specification).

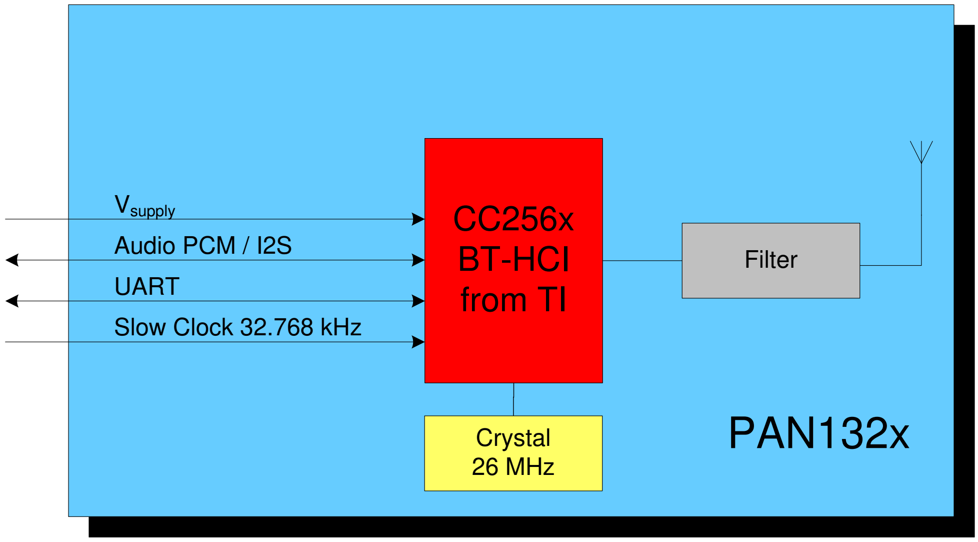
The Slow Clock 32.768 kHz is mandatory to start the internal controller, otherwise the module does not start up.

6 BLUETOOTH FEATURES

- Support of Bluetooth2.1+EDR (Lisbon Release) up to HCI level.
- Very fast AFH algorithm for both ACL and eSCO.
- Supports typically 4 dBm Class 2 TX power w/o external PA, improving Bluetooth link robustness. Adjusting the host settings, the TX power can be increased to 10 dBm. However it is important, that the national regulations and Bluetooth specification are met.
- Digital Radio Processor (DRP) single-ended 50 ohm.
- Internal temperature detection and compensation ensures minimal variation in the RF performance over temperature.
- Flexible PCM and I2S digital audio/voice interfaces: Full flexibility of data-format (Linear, a-Law, µ-Law), data-width, data order, sampling and slot positioning, master/slave modes, high clock rates up to 15 MHz for slave mode (or 4.096 MHz for Master Mode). Lost packet concealment for improved audio.
- Proprietary low-power scan method for page and inquiry scans, achieves page and inquiry scans at 1/3rd normal power.

7 BLOCK DIAGRAM





Note: The Slow Clock 32.768 kHz is mandatory, otherwise the module does not start up, refer to Chapter 5.4 for additional information.

Note: The IO are 1.8V driven and might need external level shifter and LDO. The MLDO_OUT PIN can not be used as reference due to RF internal connection.

The total capacity will not exceed 2.8uF and the total inductance will not exceed 0nH. There are no voltage multiplying or voltage boosting circuits.

8 TEST CONDITIONS

Measurements shall be made under room temperature and humidity unless otherwise specified.

9 GENERAL DEVICE REQUIREMENTS AND OPERATION

Temperature	25	±	10°C
Humidity	40	to	85%RH
SW-Patch	V2.30		
Supply Voltage	3.3V		

All specifications are over temperature and process, unless indicated otherwise.

9.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).

Note

All parameters are measured as follows unless stated otherwise:

VDD_IN [10] = 3.3 V, VDD_IO = 1.8 V.

No	See [11]		Value	Unit
Ratings Over Operating Free-Air Temperature Range				
1	VDD_IN	Supply voltage range	–0.5 to 5.5	V [12]
2	VDDIO_1.8V		–0.5 to 2.145	V
3	Input voltage to RF (Pin 13)		–0.5 to 2.1	V

[10] VDD_IN is supplied to MLDO_IN (Pin 15) and CL1.5_LDO_IN (Pin 11), other options are described in Chapter 5.3.

[11] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[12] Maximum allowed depends on accumulated time at that voltage: VDD_IN is defined in Reference schematics. When DC2DC supply is used, maximum voltage into MLDO_OUT and LDO_IN = 2.145 V.

No	See [11]	Value	Unit
4	Operating ambient temperature range	–40 to 85[13]	°C
5	Storage temperature range	–40 to 125	°C
6	Bluetooth RF inputs (Pin 13)	10	dBm
7	ESD: Human Body Model (HBM). JEDEC 22-A114	500	V

9.2 RECOMMENDED OPERATING CONDITIONS

No	Rating	Condition	Symbol	Min	Max	Unit
1	Power supply voltage [14]		VDD_IN	1.7	4.8	V
2	IO power supply voltage		VDD_IO	1.62	1.92	V
3	High-level input voltage	Default	V_{IH}	0.65 x VDD_IO	VDD_IO	V
4	Low-level input voltage	Default	V_{IL}	0	0.35 x VDD_IO	V
5	IO Input rise/fall times, 10% to 90% [15]		Tr/Tf	1	10	ns
6	Maximum ripple on VDD_IN (Sine wave) for 1.8 V (DC2DC) mode	0 to 0.1 MHz			60	mVp-p
		0.1 to 0.5 MHz			50	
		0.5 to 2.5 MHz			30	
		2.5 to 3.0 MHz			15	
		> 3.0 MHz			5	
7	Voltage dips on VDD_IN (V_{BAT}) (duration = 577 µs to 2.31 ms, period = 4.6 ms)				400	mV
8	Maximum ambient operating temperature [16]				85	°C
9	Minimum ambient operating temperature [17]				-40	□C

[13] Older generation parts, which are not recommended for new designs, will support a temperature range -20 to 70. See chapter 28, ordering information, for details.

[14] Excluding 1.98 < VDD_IN < 2.2 V range – not allowed.

[15] Asynchronous mode.

[16] The device can be reliably operated for 7 years at $T_{ambient}$ of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).
Older generation parts, which are not recommended for new designs, will support a temperature range -20 to 70. See chapter 28, ordering information, for details.

[17] The device can be reliably operated for 7 years at $T_{ambient}$ of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).
Older generation parts, which are not recommended for new designs, will support a temperature range -20 to 70. See chapter 28, ordering information, for details.

9.3 CURRENT CONSUMPTION

No	Characteristics	Min 25°C	Typ 25°C	Max 25°C	Min -40°C	Typ -40°C	Max -40°C	Min +85°C	Typ +85°C	Max +85°C	Unit
1	Current consumption in shutdown mode [18]		1	3						7	µA
2	Current consumption in deep sleep mode [19]		40	105						700	µA
3	Total IO current consumption for active mode			1			1			1	mA
4	Current consumption during transmit DH5 full throughput		40								mA

[18] Vbat + Vio

[19] Vbat + Vio + Vsd (shutdown)

9.4 GENERAL ELECTRICAL CHARACTERISTICS

No	Rating			Condition	Min	Max	Value
1	High-level output voltage, V_{OH}			at 2/4/8 mA	0.8 x VDD_IO	VDD_IO	V
				at 0.1 mA	VDD_IO – 0.2	VDD_IO	V
2	Low-level output voltage, V_{OL}			at 2/4/8 mA	0	0.2 x VDD_IO	V
				at 0.1 mA	0	0.2	V
3	IO input impedance			Resistance	1		MΩ
				Capacitance		5	pF
4	Output rise/fall times,10% to 90% (Digital pins)			C_L = 20 pF		10	Ns
5	IO pull currents	TX_DBG, PCM bus	PU	typ = 6.5	3.5	9.7	µA
			PD	typ = 27	9.5	55	
		All others	PU	typ = 100	100	300	µA
			PD	typ = 100	100	360	

9.5 NSHUTD REQUIREMENTS

No	Parameter	Symbol	Min	Max	Unit
1	Operation mode level [20]	V_{IH}	1.42	1.98	V
2	Shutdown mode level	V_{IL}	0	0.4	V
3	Minimum time for nSHUT_DOWN low to reset the device		5		ms
4	Rise/fall times	Tr/Tf		20	µs

9.6 EXTERNAL DIGITAL SLOW CLOCK REQUIREMENTS

No	Characteristics	Condition	Symbol	Min	Typ	Max	Unit
1	Input slow clock frequency				32768		Hz
2	Input slow clock accuracy (Initial + temp + aging)	Bluetooth				±250	Ppm
3	Input transition time Tr/Tf – 10% to 90%		Tr/Tf			100	Ns
4	Frequency input duty cycle			15%	50%	85%	
5	Phase noise	at 1 kHz				-125	dBc/Hz
6	Jitter	Integrated over 300 to 15000 Hz				1	Hz
7	Slow clock input voltage limits	Square wave, DC coupled	V_{IH}	0.65 x VDD_IO		VDD_IO	V peak
			V_{IL}	0		0.35 x VDD_IO	
8	Input impedance			1			MΩ
9	Input capacitance					5	pF

[20] Internal pull down retains shut down mode when no external signal is applied to this pin.

10 HOST CONTROLLER INTERFACE

The CC256X incorporates one UART module dedicated to the host controller interface (HCI) transport layer. The HCI interface transports commands, events, ACL, and synchronous data between the Bluetooth device and its host using HCI data packets.

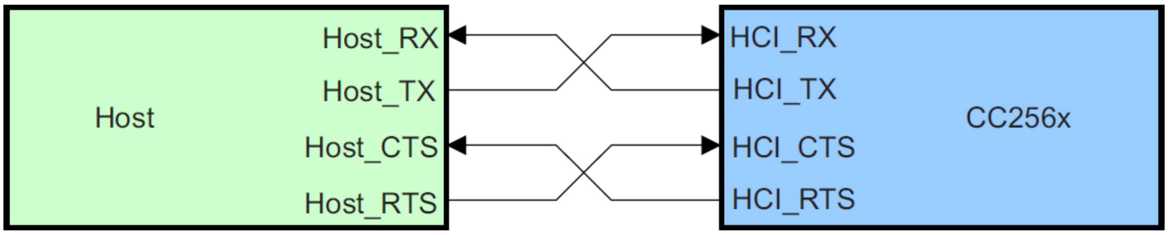
The UART module supports H4 (4-wires) protocol with maximum baud rate of 4 Mbps for all fast clock frequencies.

After power up the baud rate is set for 115.2 kbps, irrespective of fast clock frequency. The baud rate can thereafter be changed with a vendor specific command. The CC256X responds with a Command Complete Event (still at 115.2 kbps), after which the baud rate change takes place. HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTS/RTS hardware flow control

The interface includes four signals: TXD, RXD, CTS, and RTS. Flow control between the host and the CC256X is byte-wise by hardware.

Flow control is obtained by the following:



When the UART RX buffer of the CC256X passes the “flow control” threshold, it will set the UART_RTS signal high to stop transmission from the host.

When the UART_CTS signal is set high, the CC256X will stop its transmission on the interface. In case HCI_CTS is set high in the middle of transmitting a byte, the CC256X will finish transmitting the byte and stop the transmission.

11 AUDIO/VOICE CODEC INTERFACE

The codec interface is a fully-dedicated programmable serial port that provides the logic to interface to several kinds of PCM or I2S codec's. PAN13XX supports all voice coding schemes required by Bluetooth specification – Log PCM (A-Law or µ-Law) and Linear (CVSD). In addition, module also supports transparent scheme:

- Two voice channels
- Master / slave modes
- µ-Law, A-Law, Linear, Transparent coding schemes
- Long and short frames
- Different data sizes, order, and positions.
- High rate PCM interface for EDR
- Enlarged interface options to support a wider variety of codecs
- PCM bus sharing

11.1 PCM HARDWARE INTERFACE

The PCM interface is one implementation of the codec interface. It contains the following four lines:

- Clock—configurable direction (input or output)
- Frame Sync—configurable direction (input or output)
- Data In—Input
- Data Out—Output/3-state

The Bluetooth device can be either the master of the interface where it generates the clock and the frame-sync signals, or slave where it receives these two signals. The PCM interface is fully configured by a vendor specific command.

For slave mode, clock input frequencies of up to 16 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits. For master mode, the CC256X can generate any clock frequency between 64 kHz and 6 MHz.

When the I2S bus is used in an application, Panasonic recommends adding a low pass filter (series resistor and capacitor to GND) to the bus for better noise suppression. Connecting the host µController/DSP directly with the module's I2S interface is not recommended.

The suggested low pass filter component values are:

470pf
120 ohms

11.2 DATA FORMAT

The data format is fully configurable:

- The data length can be from 8 to 320 bits, in 1-bit increments, when working with two channels, or up to 640 bits when using 1 channel. The Data length can be set independently for each channel.

• The data position within a frame is also configurable in with 1 clock (bit) resolution and can be set independently (relative to the edge of the Frame Sync signal) for each channel.

• The Data_In and Data_Out bit order can be configured independently. For example; Data_In can start with the MSB while Data_Out starts with LSB. Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample sizes up to 24 bits.

• It is not necessary for the data in and data out size to be the same length.

• The Data_Out line is configured to 'high-Z' output between data words. Data_Out can also be set for permanent high-Z, irrespective of data out. This allows the CC256X to be a bus slave in a multi-slave PCM environment. At powerup, Data Out is configured as high-Z.

11.3 FRAME IDLE PERIOD

The codec interface has the capability for frame idle periods, where the PCM clock can "take a break" and become '0' at the end of the PCM frame, after all data has been transferred.

The CC256X supports frame idle periods both as master and slave of the PCM bus.

When CC256X is the master of the interface, the frame idle period is configurable. There are two configurable parameters:

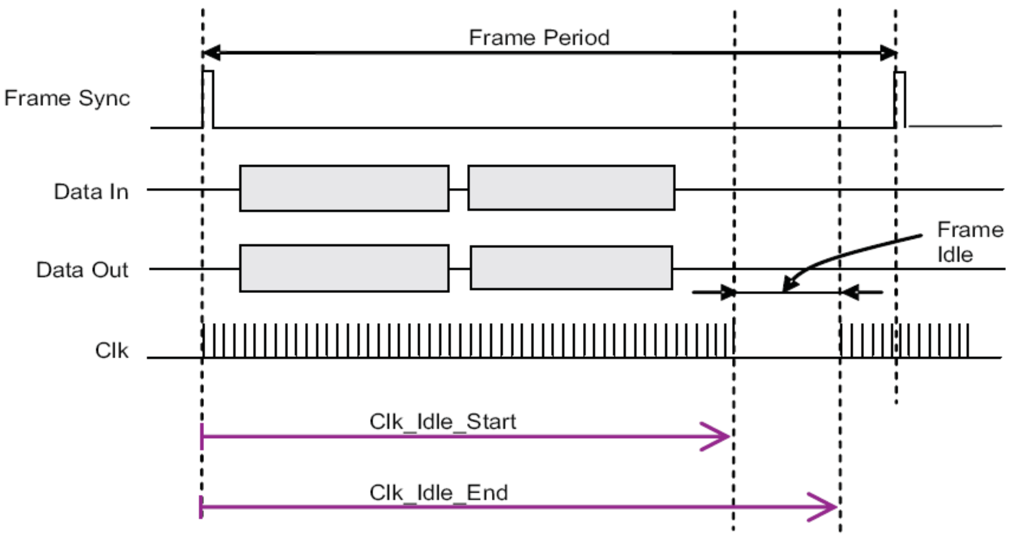
• Clk_Idle_Start – Indicates the number of PCM clock cycles from the beginning of the frame until the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock will become '0'.

• Clk_Idle_End – Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

For example, for PCM clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90.

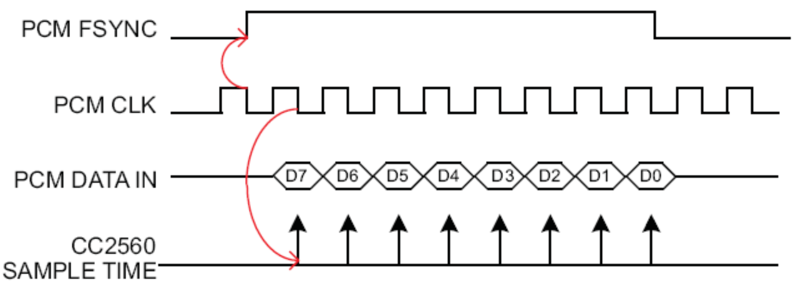
Between each two frame syncs there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame, and lasts 90 – 60 = 30 clock cycles. This means that the idle period ends 100 – 90 = 10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.



11.4 CLOCK-EDGE OPERATION

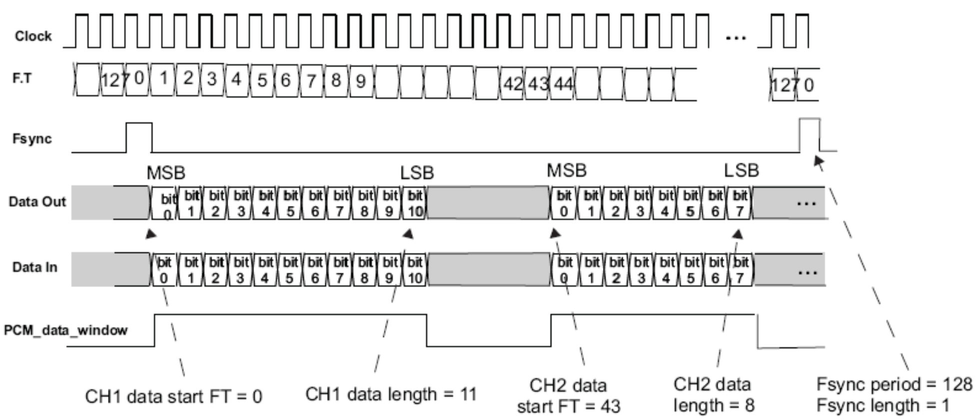
The codec interface of the CC256X can work on the rising or the falling edge of the clock. It also has the ability to sample the frame sync and the data at inversed polarity.

This is the operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame sync signal is updated (by the codec) on the falling clock edge and therefore shall be sampled (by the CC256X) on the next rising clock. The data from the codec is sampled (by the CC256X) on the clock falling edge.



11.5 TWO-CHANNEL PCM BUS EXAMPLE

In below figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus frame. (FT stands for Frame Timer)



11.6 AUDIO ENCODING

The CC256X codec interface can use one of four audio-coding patterns:

- A-Law (8-bit)
- µ-Law (8-bit)
- Linear (8- or 16-bit)

11.7 IMPROVED ALGORITHM FOR LOST PACKETS

The CC256X features an improved algorithm for improving voice quality when received voice data packets are lost. There are two options:

• Repeat the last sample – possible only for sample sizes up to 24 bits. For sample sizes >24 bits, the last byte is repeated.

• Repeat a configurable sample of 8 to 24 bits (depends on the real sample size), in order to simulate silence (or anything else) in the PCM bus. The configured sample will be written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

11.8 BLUETOOTH/PCM CLOCK MISMATCH HANDLING

In Bluetooth RX, the CC256X receives RF voice packets and writes these to the codec I/F. If the CC256X receives data faster than the codec I/F output allows, an overflow will occur. In this case, the Bluetooth has two possible behaviour modes: 'allow overflow' and 'don't allow overflow'.

• If overflow is allowed, the Bluetooth will continue receiving data and will overwrite any data not yet sent to the codec.

• If overflow is not allowed, RF voice packets received when buffer is full will be discarded.

11.9 BLUETOOTH INTER-IC SOUND (I2S)

The CC256X can be configured as an Inter-IC Sound (I2S) serial interface to an I2S codec device. In this mode, the CC256X audio codec interface is configured as a bi-directional, full-duplex interface, with two time slots per frame: Time slot 0 is used for the left channel audio data and time slot 1 for the right channel audio data. Each time slot is configurable up to 40 serial clock cycles in length and the frame is configurable up to 80 serial clock cycles in length.

Do not connect the the microcontroller/DSP directly to the module's PCM interface, a simple RC low pass filter is recommended to improve noise suppression.

11.10 CURRENT CONSUMPTION FOR DIFFERENT BLUETOOTH SCENARIOS

The following table gives average current consumption for different Bluetooth scenarios.

Conditions: VDD_IN = 3.6 V, 25°C, 26-MHz fast clock, nominal unit, 4 dBm output power.

Mode Description	Master/Slave	Average Current	Unit
Idle current (ARM off)	Master/Slave	2.5	mA
SCO link HV3	Master/Slave	12	mA
eSCO link EV3 64 kbps, no retransmission	Master/Slave	11.5	mA
eSCO link 2-EV3 64 kbps, no retransmission	Master/Slave	8.3	mA
GFSK full throughput: TX = DH1, RX = DH5	Master/Slave	38.5	mA
EDR full throughput: TX = 2-DH1, RX = 2-DH5	Master/Slave	39.2	mA
EDR full throughput: TX = 3-DH1, RX = 3-DH5	Master/Slave	39.2	mA
Sniff, 1 attempt, 1.28 s	Master/Slave	76/100	µA
Page or Inquiry Scan 1.28 s, 11.25 ms	Master/Slave	300	µA
Page (1.28 s) and Inquiry (2.56 s) scans, 11.25 ms	Master/Slave	430	µA
Low power scan, 1.28-s interval, quiet environment	Master/Slave	135	µA

12 BLUETOOTH RF PERFORMANCE

No	Characteristics	Typ	BT Spec Max	BT Spec Min
			Class1	Class1
1	Average Power Hopping DH5 [dBm] [22, 23]	7.2	20	4
2	Average Power: Ch0 [dBm] [22, 23]	7.5	20	4
3	Peak Power: Ch0 [dBm] [22, 23]	7.7	23	
4	Average Power: Ch39 [dBm] [22, 23]	7.0	20	4
5	Peak Power: Ch39 [dBm] [22, 23]	7.2	23	
6	Average Power: Ch78 [dBm] [22, 23]	6.7	20	4
7	Peak Power: Ch78 [dBm] [22, 23]	7.0	23	
8	Max. Frequency Tolerance: Ch0 [kHz]	-2.6	75	-75
9	Max. Frequency Tolerance: Ch39 [kHz]	-2.2	75	-75
10	Max. Frequency Tolerance: Ch78 [kHz]	-2.1	75	-75
11	Max. Drift: Ch0_DH1 [kHz]	3.6	25	-25
12	Max. Drift: Ch0_DH3 [kHz]	3.7	40	-40
13	Max. Drift: Ch0_DH5 [kHz]	4.0	40	-40
14	Max. Drift Rate: Ch0_DH1 [kHz]	-2.6	20	-20
15	Max. Drift Rate: Ch0_DH3 [kHz]	-3.2	20	-20
16	Max. Drift Rate: Ch0_DH5 [kHz]	-3.3	20	-20
17	Max. Drift: Ch39_DH1 [kHz]	4.0	25	-25
18	Max. Drift: Ch39_DH3 [kHz]	4.3	40	-40
19	Max. Drift: Ch39_DH5 [kHz]	4.3	40	-40
20	Max. Drift Rate: Ch39_DH1 [kHz]	-3.1	20	-20
21	Max. Drift Rate: Ch39_DH3 [kHz]	-3.6	20	-20

No	Characteristics	Typ	BT Spec Max	BT Spec Min
			Class1	Class1
22	Max. Drift Rate: Ch39_DH5 [kHz]	-3.7	20	-20
23	Max. Drift: Ch78_DH1 [kHz]	4.1	25	-25
24	Max. Drift: Ch78_DH3 [kHz]	4.5	40	-40
25	Max. Drift: Ch78_DH5 [kHz]	4.4	40	-40
26	Max. Drift Rate: Ch78_DH1 [kHz]	-3.4	20	-20
27	Max. Drift Rate: Ch78_DH3 [kHz]	-3.9	20	-20
28	Max. Drift Rate: Ch78_DH5 [kHz]	-4.1	20	-20
29	Delta F1 Avg: Ch0 [kHz]	159.5	175	140
30	Delta F2 Max.: Ch0 [%]	100.0		99.9
31	Delta F2 Avg/Delta F1 Avg: Ch0	0.9		0.8
32	Delta F1 Avg: Ch39 [kHz]	159.8	175	140
33	Delta F2 Max.: Ch39 [%]	100.0		99.9
34	Delta F2 Avg/Delta F1 Avg: Ch39	0.9		0.8
35	Delta F1 Avg: Ch78 [kHz]	159.1	175	140
36	Delta F2 Max.: Ch78 [%]	100.0		99.9
37	Delta F2 Avg/Delta F1 Avg: Ch78	0.9		0.8
45	Sensitivity	-93.0		-81
46	f(H)-f(L): Ch0 [kHz]	918.4	1000	
47	f(H)-f(L): Ch39 [kHz]	918.3	1000	
48	f(H)-f(L): Ch78 [kHz]	918.2	1000	
49	ACPower -3: Ch3 [dBm]	-51.5	-40	
50	ACPower -2: Ch3 [dBm]	-50.4	-40	
51	ACPower -1: Ch3 [dBm]	-18.5		
52	ACPower Center: Ch3 [dBm]	8.1	20	4
53	ACPower +1: Ch3 [dBm]	-19.2		
54	ACPower +2: Ch3 [dBm]	-50.7	-40	
55	ACPower +3: Ch3 [dBm]	-53.3	-40	
56	ACPower -3: Ch39 [dBm]	-51.6	-40	
57	ACPower -2: Ch39 [dBm]	-50.7	-40	
58	ACPower -1: Ch39 [dBm]	-19.0		
59	ACPower Center: Ch39 [dBm]	7.7	20	4
60	ACPower +1: Ch39 [dBm]	-19.7		
61	ACPower +2: Ch39 [dBm]	-50.9	-40	
62	ACPower +3: Ch39 [dBm]	-53.2	-40	
63	ACPower -3: Ch75 [dBm]	-51.7	-40	
64	ACPower -2: Ch75 [dBm]	-50.7	-40	
65	ACPower -1: Ch75 [dBm]	-19.2		
66	ACPower Center: Ch75 [dBm]	7.5	20	4
67	ACPower +1: Ch75 [dBm]	-20.0		
68	ACPower +2: Ch75 [dBm]	-51.0	-40	
69	ACPower +3: Ch75 [dBm]	-53.4	-40	
70	omega i 2-DH5: Ch0 [kHz]	-4.7	75	-75
71	omega o + omega i 2-DH5: Ch0 [kHz]	-6.0	75	-75
72	omega o 2-DH5: Ch0 [kHz]	-1.5	10	-10
73	DEVM RMS 2-DH5: Ch0 [%]	0.0	0.2	

No	Characteristics	Typ	BT Spec Max	BT Spec Min
			Class1	Class1
74	DEVM Peak 2-DH5: Ch0 [%]	0.1	0.35	
75	DEVM 99% 2-DH5: Ch0 [%]	100.0		99
76	omega i 3-DH5: Ch0 [kHz]	-3.7	75	-75
77	omega o + omega i 3-DH5: Ch0 [kHz]	-5.8	75	-75
78	omega o 3-DH5: Ch0 [kHz]	-2.6	10	-10
79	DEVM RMS 3-DH5: Ch0 [%]	0.0	0.13	
80	DEVM Peak 3-DH5: Ch0 [%]	0.1	0.25	
81	DEVM 99% 3-DH5: Ch0 [%]	100.0		99
82	omega i 2-DH5: Ch39 [kHz]	-4.8	75	-75
83	omega o + omega i 2-DH5: Ch39 [kHz]	-6.1	75	-75
84	omega o 2-DH5: Ch39 [kHz]	-1.4	10	-10
85	DEVM RMS 2-DH5: Ch39 [%]	0.0	0.2	
86	DEVM Peak 2-DH5: Ch39 [%]	0.1	0.35	
87	DEVM 99% 2-DH5: Ch39 [%]	100.0		99
88	omega i 3-DH5: Ch39 [kHz]	-3.8	75	-75
89	omega o + omega i 3-DH5: Ch39 [kHz]	-5.9	75	-75
90	omega o 3-DH5: Ch39 [kHz]	-2.6	10	-10
91	DEVM RMS 3-DH5: Ch39 [%]	0.0	0.13	
92	DEVM Peak 3-DH5: Ch39 [%]	0.1	0.25	
93	DEVM 99% 3-DH5: Ch39 [%]	100.0		99
94	omega i 2-DH5: Ch78 [kHz]	-4.9	75	-75
95	omega o + omega i 2-DH5: Ch78 [kHz]	-6.2	75	-75
96	omega o 2-DH5: Ch78 [kHz]	-1.4	10	-10
97	DEVM RMS 2-DH5: Ch78 [%]	0.0	0.2	
98	DEVM Peak 2-DH5: Ch78 [%]	0.1	0.35	
99	DEVM 99% 2-DH5: Ch78 [%]	100.0		99
100	omega i 3-DH5: Ch78 [kHz]	-3.8	75	-75
101	omega o + omega i 3-DH5: Ch78 [kHz]	-6.0	75	-75
102	omega o 3-DH5: Ch78 [kHz]	-2.7	10	-10
103	DEVM RMS 3-DH5: Ch78 [%]	0.0	0.13	
104	DEVM Peak 3-DH5: Ch78 [%]	0.1	0.25	
105	DEVM 99% 3-DH5: Ch78 [%]	100.0		99

No	Characteristics	Condition	Min	Typ	Max	BT Spec	Unit
1	Operation frequency range		2402		2480		MHz
2	Channel spacing			1			MHz
3	Input impedance			50			Ω
4	Sensitivity, Dirty Tx on	GFSK, BER = 0.1%		-93.0		-70	dBm
		Pi/4-DQPSK, BER = 0.01%		-92.5		-70	
		8DPSK, BER = 0.01%		-85.5		-70	