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Product Specification

Applicant / Manufacturer Hardware	Panasonic Industrial Devices Europe GmbH Zeppelinstrasse 19 21337 Lüneburg Germany
Applicant / Manufacturer Software	Dialog Semiconductors

By purchase of any of products described in this document the customer accepts the document's validity and declares their agreement and understanding of its contents and recommendations. Panasonic reserves the right to make changes as required without notification.

TABLE OF CONTENTS

1 KEY FEATURES

- Pre-programmed BT/MAC Address
- Includes 16MHz and 32.768kHz crystal Crystal calibrated up to 1ppm
- Single-mode Bluetooth Smart System-on-Chip
- Programmable ARM CORTEX M0 CPU
- Autonomous BTLE Stand Alone Operation
- Bluetooth v4.1 (LE) embedded GATT profile – Low Energy Single Mode
- Small 9.0 x 9.5 x 1.8 mm SMD package with antenna
- Temperature Range from -40°C to +85°C
- Peak Power consumption 4.9mA Rx and Tx
- Less than a few µA in low power modes
- Link budget 93dBm (Rx Sensitivity -93, Tx 0 dBm)
- Integrated shielding to resist EMI
- No external components needed

2 BLUETOOTH LOW ENERGY

Bluetooth Low Energy (BLE), also called Bluetooth Smart, is a part of Bluetooth Ver. 4.0, BT v4.0 covers both BLE as well as Classic Bluetooth v2.1 and v3.0.

Bluetooth Low Energy (BLE) is not backwards compatible with previous Classic Bluetooth standards (v2.1+EDR or v3.0). Dual mode Bluetooth v4.0 is targeted to gateway products and backwards compatible, but is not practical for low power devices.

Bluetooth® 4.1 is an evolutionary update to the Bluetooth Core Specification. It rolls up adopted Bluetooth Core Specification Addenda (CSA1, 2, 3 & 4) while adding new features and benefits. Bluetooth 4.1 improves usability for consumers, empowers innovation for product developers and extends the technology's foundation as an essential link for the Internet of Things.

For more more details please see the BLUETOOTH® 4.1 QUICK REFERENCE GUIDE from Bluetooth SIG [1]

3 DESCRIPTION FOR THE MODULE

The PAN1740 is a short-range BLE single mode module for implementing Bluetooth functionality into various electronic devices.

PAN1740 is fully compliant with the Bluetooth V4.1 standard.

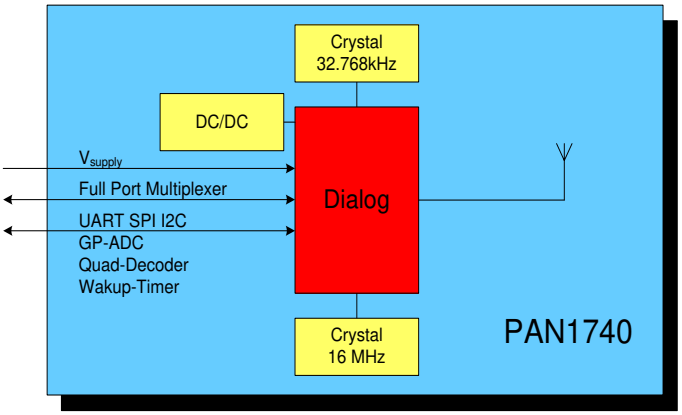
It includes dedicated hardware for the Link Layer implementation of Bluetooth®Smart and interface controllers for enhanced connectivity capabilities.

Please contact your local sales office for further details on additional options and services:

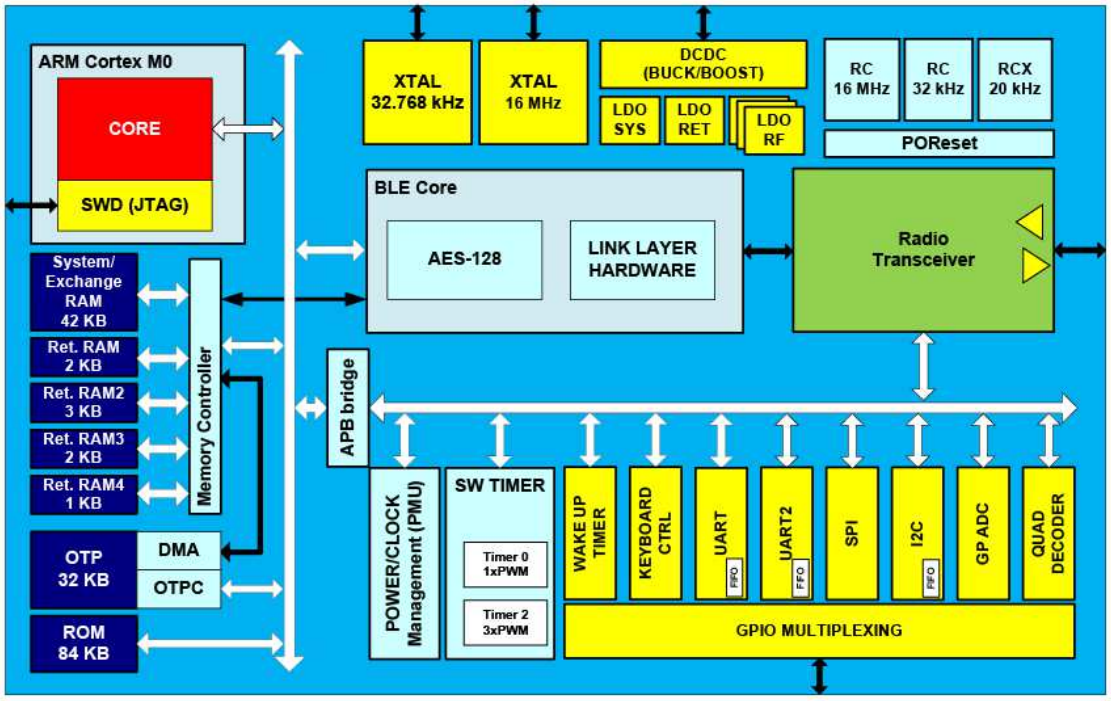
www.panasonic.com/rfmodules for the US, http://pideu.panasonic.de/products/wireless-modules.html for EU or write an e-mail to wireless@eu.panasonic.com.

4 BLOCK DIAGRAM

4.1 PAN1740



4.2 BLUETOOTH IC



5 SYSTEM OVERVIEW

The PAN1740 contains the following internal blocks:

5.1 ARM CORTEX M0 CPU

The Cortex-M0 processor is a 32-bit Reduced Instruction Set Computing (RISC) processor with a von Neumann architecture (single bus interface). It uses an instruction set called Thumb, which was first supported in the ARM7TDMI processor; however, several newer instructions from the ARMv6 architecture and a few instructions from the Thumb-2 technology are also included. Thumb-2 technology extended the previous Thumb instruction set to allow all operations to be carried out in one CPU state. The instruction set in Thumb-2 includes both 16-bit and 32-bit instructions; most instructions generated by the C compiler use the 16-bit instructions, and the 32-bit instructions are used when the 16-bit version cannot carry out the required operations. This results in high code density and avoids the overhead of switching between two instruction sets.

In total, the Cortex-M0 processor supports 56 base instructions, although some instructions can have more than one form. While the instruction set is small, the Cortex-M0 processor is highly capable because the Thumb instruction set is highly optimized.

5.2 BLUETOOTH SMART

5.2.1 BLE Core

The BLE (Bluetooth Low Energy) core is a qualified Bluetooth v4.1 baseband controller compatible with Bluetooth Smart specification and it is in charge of packet encoding-decoding and frame scheduling.

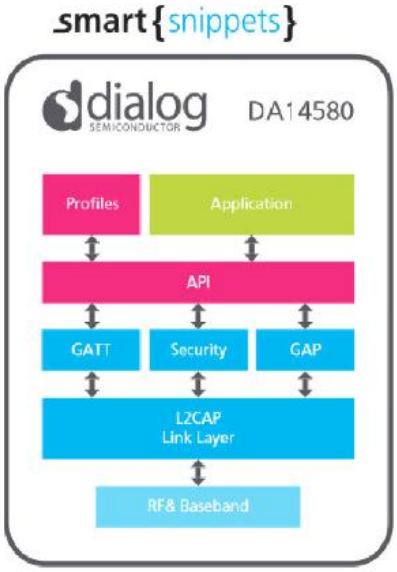
- Bluetooth Smart Specifications compliant according to the Specification of the Bluetooth System, v4.1, Bluetooth SIG.
- All device classes are supported -- Broadcast, Central, Observer, Peripheral)
- All packet types (Advertising / Data / Control)
- Encryption (AES / CCM)
- Bit stream processing (CRC, Whitening)
- FDMA / TDMA / events formatting and synchronization
- Frequency Hopping calculation
- Operating clock with internal 16 MHz
- Low power modes with internal 32.678 kHz
- Supports power down of the baseband during the protocol's idle periods.
- Advanced High performance Bus (AHB) Slave interface for register file access.
- AHB Slave interface for Exchange Memory access of CPU via BLE core.
- AHB Master interface for direct access of BLE core to Exchange Memory space

5.2.2 Smart Snippets

The PAN1740 is available together with Dialog's SmartSnippets™ Bluetooth Software platform which includes a qualified Bluetooth Smart single-mode stack on chip.

Numerous Bluetooth Smart profiles for consumer wellness, sport, fitness, security and proximity applications are supplied as standard, while additional customer profiles can be developed and added as needed.

The SmartSnippetsTM software development environment is based on Keil™ 's uVision mature tools and contains example application code for both embedded and hosted modes.



5.2.3 Memory

The following memories are part of the PAN1740's internal blocks:

ROM. This is a 84 kB ROM containing the Bluetooth Smart protocol stack as well as the boot code sequence.

OTP. This is a 32 kB One-Time Programmable memory array, used to store the application code as well as Bluetooth Smart profiles. It also contains the system configuration and calibration data.

System SRAM. This is a 42 kB system SRAM (Sys-RAM) which is primarily used for mirroring the program code from the OTP when the system wakes/powers up. It also serves as Data RAM for intermediate variables and various data that the protocol requires. Optionally, it can be used as extra memory space for the BLE TX and RX data structures.

Retention RAMs. These are 4 special low leakage SRAM cells (2 kB + 2 kB + 3 kB + 1 kB) used to store various data of the Bluetooth Smart protocol as well as the system's global variables and processor stack when the system goes into Deep Sleep mode. Storage of this data ensures secure and quick configuration of the BLE Core after the system wakes up. Every cell can be powered on or off according to the application needs for retention area when in Deep Sleep mode.

5.2.4 Functional Modes

The PAN1740 is optimized for embedded applications such as health monitoring, sports measuring, human interaction devices, etc. Customers are able to develop and test their own applications. Upon completion of development, the application code can be programmed into the OTP. In general, the system has three functional modes of operation:

A. Development Mode: During this phase application code is developed using the ARM Cortex M0 SW environment. The compiled code is then downloaded into the System RAM or any Retention RAMs by means of SWD (JTAG) or any serial interface (e.g. UART). Address 0x00 is remapped to the physical memory that contains the code and the CPU is configured to reset and execute code from the remapped device. This mode enables application development, debugging and on-the-fly testing.

B. Normal Mode: After the application is completed and verified, the code can be burned into the OTP. When the system boots/wakes up, the DMA of the OTP controller will automatically copy the program code from the OTP into the system RAM. Next, a SW reset will remap address 0x00 to the System RAM and code execution is started. Hence, in this mode, the system is autonomous, contains the required SW in OTP and is ready for integration into the final product.

C. Calibration Mode: Programming the Bluetooth device address is completed in Calibration Mode.

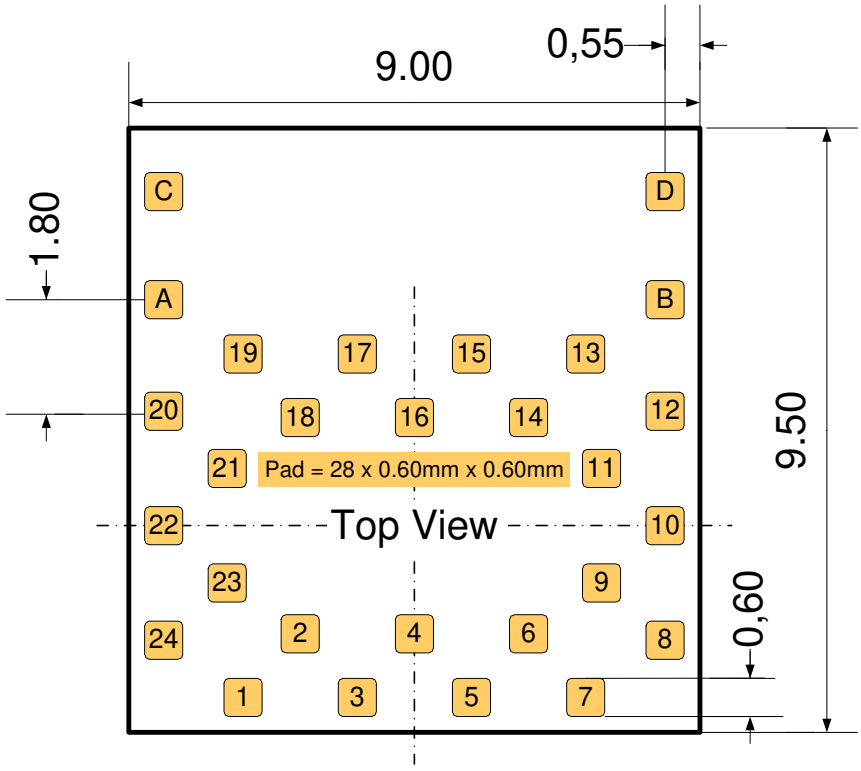
5.2.5 Power Modes

There are four different power modes in the PAN1740:

- Active Mode: System is active and operates at full speed.
- Sleep Mode: No power gating has been programmed, the ARM CPU is idle, waiting for an interrupt. PD_SYS is on. PD_PER and PED_RAD depending on the programmed enabled value.
- Extended Sleep Mode: All power domains are off except for the PD_AON, the programmed PD_RRx and the PD_SR. Since the SysRAM retains its data, no OTP mirroring is required upon waking up the system.
- Deep Sleep Mode: All power domains are off except for the PD_AON and the programmed PD_RRx. This mode dissipates the minimum leakage power. However, since the SysRAM has not retained its data, an OTP mirror action is required upon waking up the system.

6 TERMINAL LAYOUT

Top view, Application PCB



7 TERMINAL DESCRIPTION

PIN			Description
1	GND		
2	RST	I	INPUT. Reset signal (active high).
3	P0.7	IO	General purpose I/O port bit or alternate function nodes.
4	P0.6	IO	General purpose I/O port bit or alternate function nodes.
5	P0.5	IO	General purpose I/O port bit or alternate function nodes. UART RX*
6	P0.4	IO	General purpose I/O port bit or alternate function nodes. UART TX*
7	GND		
8	VCC	AI	Power supply
9	P0.3	IO	General purpose I/O port bit or alternate function nodes. UART CTS*
10	P0.2	IO	General purpose I/O port bit or alternate function nodes. UART RTS*
11	P0.1	IO	General purpose I/O port bit or alternate function nodes.
12	P0.0	IO	General purpose I/O port bit or alternate function nodes.
13	n.c.		
14	VPP	AI	INPUT. This pin is used while OTP programming and testing. **
15	GND		
16	P1_4/SWCLK	IO	INPUT JTAG clock signal
17	GND		

18	P1_5/SW_DIO	IO	INPUT/OUTPUT. JTAG Data input/output.
19	GND		
20	GND		
21	P1.3	IO	General purpose I/O port bit or alternate function nodes.
22	P1.2	IO	General purpose I/O port bit or alternate function nodes.
23	P1.1	IO	General purpose I/O port bit or alternate function nodes.
24	P1.0	IO	General purpose I/O port bit or alternate function nodes.
A	GND		
B	GND		
C	GND		
D	GND		

For more detailed description of the alternate function nodes please refer to the Dialog Datasheet.

*Dependent on the software configuration the UART can be set also to any other IO.

** Supply voltage on pin VPP during OTP programming is 6.8V+/-0.25V

8 INTERFACES

8.1 UART

The UART is compliant to the industry-standard 16550 and is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back. There is no DMA support on the UART block since its contains internal FIFOs. Both UARTs support hardware flow control signals (RTS, CTS, DTR, DSR).

Features

- 16 bytes Transmit and receive FIFOs.
- Hardware flow control support (CTS/RTS)
- Shadow registers to reduce software overhead and also include a software programmable reset
- Transmitter Holding Register Empty (THRE) interrupt mode
- IrDA 1.0 SIR mode supporting low power mode.
- Functionality based on the 16550 industry standard:
- Programmable character properties, such as number of data bits per character (5-8), optional
- parity bit (with odd or even select) and number of stop bits (1, 1.5 or 2)
- Line break generation and detection
- Prioritized interrupt identification
- Programmable serial data baud rate as calculated by the following: baud rate = (serial clock frequency)/(divisor).

8.2 SPI+

This interface supports a subset of the Serial Peripheral Interface SPI™. The serial interface can transmit and receive 8, 16 or 32 bits in master/slave mode and transmit 9 bits in master mode. The SPI+ interface has enhanced functionality with bidirectional 2x16-bit word FIFOs.

SPI™ is a trademark of Motorola, Inc.

Features

- Slave and Master mode
- 8 bit, 9 bit, 16 bit or 32 bit operation
- Clock speeds up to 16 MHz. Programmable output frequencies of SPI source clock divided by 1, 2, 4, 8
- SPI mode 0, 1, 2, 3 support. (clock edge and phase)
- Programmable SPI_DO idle level
- Maskable Interrupt generation
- Bus load reduction by unidirectional writes-only and reads-only modes.
- Built-in RX/TX FIFOs for continuous SPI bursts.

8.3 I^2C

The I^2C is a programmable control bus that provides support for the communications link between Integrated Circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters.

Features

- Two-wire I^2C serial interface consists of a serial data line (SDA) and a serial clock (SCL)
- Two speeds are supported:
- Standard mode (0 to 100 Kb/s)
- Fast mode (<= 400 Kb/s)
- Clock synchronization
- 32 deep transmit/receive FIFOs
- Master transmit, Master receive operation
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- Bulk transmit mode
- Default slave address of 0x055
- Interrupt or polled-mode operation
- Handles Bit and Byte waiting at both bus speeds
- Programmable SDA hold time

8.4 GENERAL PURPOSE (GP) ADC

The PAN1740 is equipped with a high-speed ultra low power 10-bit general purpose Analog-to-Digital Converter (GPADC). It can operate in unipolar (single ended) mode as well as in bipolar (differential) mode. The ADC has its own voltage regulator (LDO) of 1.2 V, which represents the full scale reference voltage.

Features

- 10-bit dynamic ADC with 65 ns conversion time
- Maximum sampling rate 3.3 Msample/s
- Ultra low power (5 µA typical supply current at 100 ksample/s)
- Single-ended as well as differential input with two input scales
- Four single-ended or two differential external input channels
- Battery monitoring function
- Chopper function
- Offset and zero scale adjust
- Common-mode input level adjust

8.5 QUADRATURE DECODERS

This block decodes the pulse trains from a rotary encoder to provide the step and the direction of the movement of an external device. Three axes (X, Y, Z) are supported.

The integrated quadrature decoder can automatically decode the signals for the X, Y and Z axes of a HID input device, reporting step count and direction: the channels are expected to provide a pulse train with 90 degrees phase difference; depending on whether the reference channel is leading or lagging, the directioncan be determined.

This block can be used for waking up the chip as soon as there is any kind of movement from the external device connected to it.

Features

- Three 16-bit signed counters that provide the step count and direction on each of the axes (X, Y and Z)
- Programmable system clock sampling at maximum 16 MHz.
- APB interface for control and programming
- Programmable source from P0, P1 ports
- Digital filter on the channel inputs to avoid spikes

8.6 KEYBOARD CONTROLLER

The keyboard controller can be used for debouncing the incoming GPIO signals when implementing a keyboard scanning engine. It generates an interrupt to the CPU (KEYBR_IRQ). In parallel, five extra interrupt lines can be triggered by a state change on 32 selectable GPIOs (GPIOx_IRQ).

Features

- Monitors any of the 12 available GPIOs
- Generates a keyboard interrupt on key press or key release
- Implements debouncing time from 0 up to 63 ms
- Supports five separate interrupt generation lines from GPIO toggling

8.7 INPUT/OUTPUT PORTS

The PAN1740 has software-configurable I/O pin assignment, organized into ports Port 0, Port1.

Features

- Port 0: 8 pins, Port 1: 6 pins (including SW_CLK and SWDIO)
- Fully programmable pin assignment
- Selectable Push-pull or open drain per pin
- Selectable 25KOhm pull-up, pull-down resistors per pin
- Pull-up voltage VBAT3V (BUCK mode)
- Fixed assignment for analog pin ADC[3:0]
- Pins retain their last state when system enters the Extended or Deep Sleep mode.

8.8 TIMERS

For any software related description please refer to the according Dialog document.

8.9 RESET

The PAN1740 comprises an RST pad which is active high. It contains an RC filter for spikes suppression with 400 kΩ and 2.8 pF for the resistor and the capacitor respectively. It also contains a 25 kΩ pulldown resistor. This pad should be connected to ground if not needed by the application. The typical latency of the RST pad is in the range of 2 µs.

9 SPECIFICATIONS

Table 3: Absolute maximum ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{PIN(LIM)}$(default)	limiting voltage on a pin	Voltage between GND and VBAT3V	-0.1		VBAT3V+ 0.2	V
T_{STG}	storage temperature		-50		150	°C
$t_{R(SUP)}$	supply rise time	Power supply rise time			100	ms
$V_{BAT(LIM)}$(VBAT3V) *Note1	limiting battery supply voltage	Supply voltage on VBAT3V in a buck-converter application, pin VBAT1V is connected to ground	1.8/2.2 *Note1		3.45	V
$V_{ESD(HBM)}$(WLCSP34)	electrostatic discharge voltage (Human Body Model)				2000	V
$V_{ESD(HBM)}$(QFN48)	electrostatic discharge voltage (Human Body Model)				4000	V
$V_{ESD(MM)}$(WLCSP34)	electrostatic discharge voltage (Machine Model)				175	V
$V_{ESD(CDM)}$(WLCSP34)	electrostatic discharge voltage (Charged Device Model)				500	V

Note1: The BUCK mode of the DCDC can operate correctly with voltages in the range of 2.2V upto 3.3V. If the voltage drops below that, then the OTP might not be readable any more. However, if no OTP is used, then the system is able to further operate up to 1.8V.

Table 4: Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}(VBAT3V)	battery supply voltage	Supply voltage on VBAT3V in a buck-converter application, pin VBAT1V is connected to ground	2.35		3.3	V
V_{PIN}(default)	voltage on a pin	Voltage between GND and VBAT3V	0		3.3	V
T_A	ambient temperature		-40		85	°C
VPP	programming voltage	Supply voltage on pin VPP during OTP programming	6.55	6.8	7.05	V

Table 5: DC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{BAT}(DP_SLP)_ BUCK_1kB	battery supply current	Typical buck-application in deep-sleep with 1kB retention RAM active. VBAT3V = 3V, running from RC32K oscillator at lowest frequency		0.4		µA
IBAT(DP_SLP)_ BUCK_2kB	battery supply current	Typical buck-application in deep-sleep with 2kB retention RAM active. VBAT3V = 3V (Note 3)		0.45		µA
IBAT(DP_SLP)_ BUCK_8kB	battery supply current	Typical buck-application in deep-sleep with 8kB retention RAM active. VBAT3V = 3V		0.6		µA
IBAT(EXT_SLP) _BUCK_43KB	battery supply current	Typical buck-application in extended-sleep mode with 42kB (SysRAM) and 1kB (RetRAM) retained		1.2		µA
IBAT(EXT_SLP) _BUCK_50kB	battery supply current	Typical buck-application in extended-sleep mode with 42kB (SysRAM) and 8kB (RetRAM) retained		1.4		µA
IBAT(ACT_RX)_ BUCK	battery supply current	Typical application with buck converter and receiver active, VBAT3V = 3.0V		5.1		mA

IBAT(ACT_TX)_ BUCK	battery supply current	Typical application with buck converter and transmitter active, VBAT3V = 3.0V		4.8		mA
PBAT(DP_SLP) _BUCK_1kB	battery power consump- tion	Typical boost-applica- tion in deep-sleep with 1kB retention RAM active, running from RC32K oscillator		1.2		µW
PBAT(ACT_RX) _BUCK	battery power consump- tion	Typical application with buck converter, receive mode		15.5		mW
PBAT(ACT_TX) _BUCK	battery power consump- tion	Typical application with buck converter, transmit mode		14.3		mW

Table 8: 16 MHz Crystal Oscillator: Timing characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$t_{STA(XTAL)}$(16M)	crystal oscillator startup time		0.5	2	3	ms

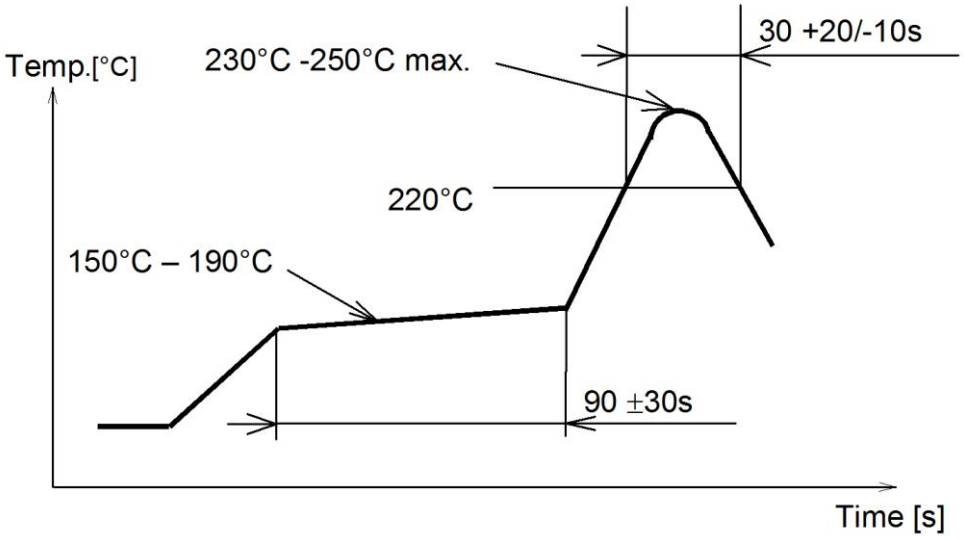
Table 10: 32 kHz Crystal Oscillator: Timing characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$t_{STA(XTAL)}$(32k)	crystal oscillator startup time	Typical application, time until 1000 clocks are detected		0.4		s

Table 12: DC-DC converter: DC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_O(BUCK)	output voltage	default settings		1.41		V
η_{CONV_MAX}(BUCK)	maximum conversion efficiency			86		%
$\Delta V_O/\Delta V_I$(BUCK)	line regulation	2.35V < VBAT3V < 3.3V	-2	0.7	2	%/V
$\Delta V_O/\Delta I_L$(BUCK)	load regulation	VBAT3V = 2.5V	-0.2	-0.02	0.2	%/mA
V_{RPL}(BUCK)	ripple voltage	buck mode; RMS ripple voltage		5		mV

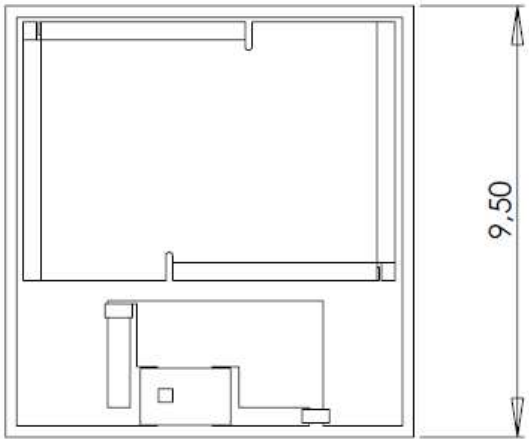
10 SOLDERING TEMPERATURE-TIME PROFILE (FOR REFLOW SOLDERING)

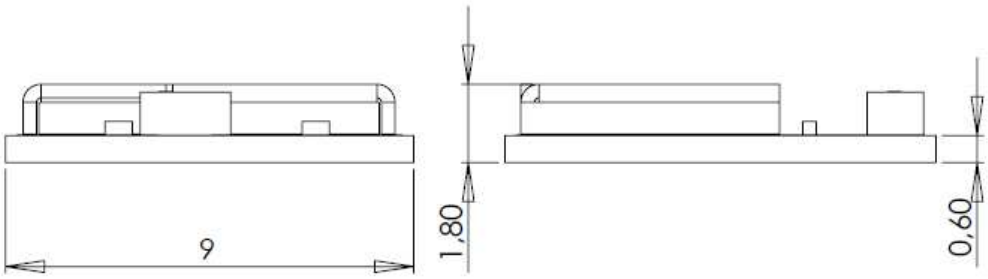


Reflow permissible cycle: 2
Opposite side reflow is prohibited due to module weight.

11 MODULE DIMENSION

No.	Item	Dimension	Tolerance	Remark
1	Width	9.50	± 0.30	
2	Lenght	9.00	± 0.30	
3	Height	1.80	± 0.20	With case

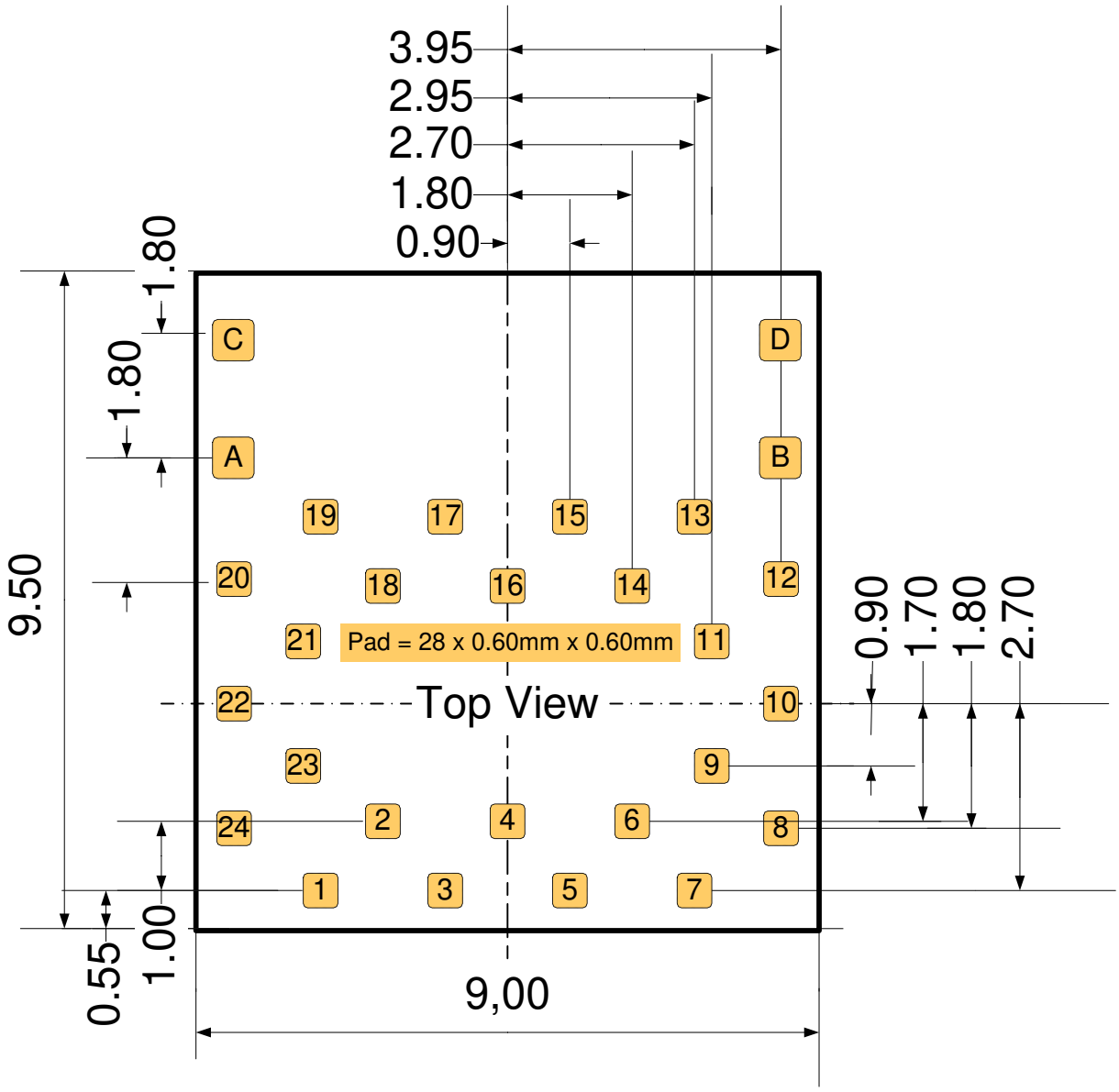




12 FOOTPRINT OF THE MODULE

All dimensions are in millimeters.
The outer dimensions have a tolerance of ± 0.2mm.

The layout is symetric to center. The inner pins (2,4,6,9,11,14,16,18,21,23) are shifted to the center by 1mm.



13 CASE MARKING

14 MARKING

P	A	N	1	7	4	0			H	W	/	S	W		
E	N	W	8	9	8	4	6	A	1	K	F				
Y	Y	W	W	D	L	L									
F	C	C	I	D	:		T	7	V	1	7	4	0		

15 MARKING DEFINITION

PAN1740 (Model Name), HW/SW (Hardware/Software version)

ENW89846A1KF (Part Number, refer to chapter 28 Ordering Information)

Lot code (YearYear, WeekWeek, Day, LotLot)

FCC ID

ES (Engineering Sample marking)

16 MECHANICAL REQUIREMENTS

No.	Item	Limit	Condition
1	Solderability	More than 75% of the soldering area shall be coated by solder	Reflow soldering with recommendable temperature profile
2	Resistance to soldering heat	It shall be satisfied electrical requirements and not be mechanical damage	

17 RELIABILITY TESTS

The measurement should be done after being exposed to room temperature and humidity for 1 hour.

No.	Item	Limit	Condition
1	Vibration test	Electrical parameter should be in specification	a) Freq.:10~50Hz,Amplitude:1.5mm a) 20min. / cycle,1hrs. each of XYZ axis b) Freq.:30~100Hz, 6G b) 20min. / cycle,1hrs. each of XYZ axis
2	Shock test	the same as above	Dropped onto hard wood from height of 50cm for 3 times
3	Heat cycle test	the same as above	-40°C for 30min. and +85°C for 30min.; each temperature 300 cycles
4	Moisture test	the same as above	+60°C, 90% RH, 300h
5	Low temp. test	the same as above	-40°C, 300h
6	High temp. test	the same as above	+85°C, 300h

18 CAUTIONS

Failure to follow the guidelines set forth in this document may result in degrading of the product's functions and damage to the product.

19 DESIGN NOTES

(1) Follow the conditions written in this specification, especially the control signals of this module.
(2) The supply voltage has to be free of AC ripple voltage (for example from a battery or a low noise regulator output). For noisy supply voltages, provide a decoupling circuit (for example a ferrite in series connection and a bypass capacitor to ground of at least 47uF directly at the module).
(3) This product should not be mechanically stressed when installed.
(4) Keep this product away from heat. Heat is the major cause of decreasing the life of these products.
(5) Avoid assembly and use of the target equipment in conditions where the products' temperature may exceed the maximum tolerance.
(6) The supply voltage should not be exceedingly high or reversed. It should not carry noise and/or spikes.
(7) Keep this product away from other high frequency circuits.

20 INSTALLATION NOTES

(1) Reflow soldering is possible twice based on the conditions in chapter 15.
Set up the temperature at the soldering portion of this product according to this reflow profile.
(2) Carefully position the products so that their heat will not burn into printed circuit boards or affect the other components that are susceptible to heat.
(3) Carefully locate these products so that their temperatures will not increase due to the effects of heat generated by neighboring components.
(4) If a vinyl-covered wire comes into contact with the products, then the cover will melt and generate toxic gas, damaging the insulation. Never allow contact between the cover and these products to occur.
(5) This product should not be mechanically stressed or vibrated when reflowed.
(6) If you want to repair your board by hand soldering, please keep the conditions of this chapter.
(7) Do not wash this product.
(8) Refer to the recommended pattern when designing a board.
(9) Pressing on parts of the metal cover or fastening objects to the metal will cause damage to the unit.
(10) For more details on LGA (Land Grid Arrey) soldering processes refer to the application note.

21 USAGE CONDITIONS NOTES

(1) Take measures to protect the unit against static electricity.
If pulses or other transient loads (a large load applied in a short time) are applied to the products, check and evaluate their operation befor assembly on the final products.
(2) Do not use dropped products.
(3) Do not touch, damage or soil the pins.
(4) Follow the recommended condition ratings about the power supply applied to this product.
(5) Electrode peeling strength: Do not add pressure of more than 4.9N when soldered on PCB.
(6) Pressing on parts of the metal cover or fastening objects to the metal cover will cause damage.
(7) These products are intended for general purpose and standard use in general electronic equipment, such as home appliances, office equipment, information and communication equipment.

22 STORAGE NOTES

(1) The module should not be stressed mechanically during storage.
(2) Do not store these products in the following conditions or the performance characteristics of the product, such as RF performance will be adversely affected:
- Storage in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX
- Storage in direct sunlight
- Storage in an environment where the temperature may be outside the range of 5°C to 35°C range, or where the humidity may be outside the 45 to 85% range.
- Storage of the products for more than one year after the date of delivery Storage period: Please check the adhesive strength of the embossed tape and soldering after 6 months of storage.

(3) Keep this product away from water, poisonous gas and corrosive gas.
(4) This product should not be stressed or shocked when transported.
(5) Follow the specification when stacking packed crates (max. 10).

23 SAFETY CAUTIONS

These specifications are intended to preserve the quality assurance of products and individual components.

Before use, check and evaluate the operation when mounted on your products. Abide by these specifications, without deviation when using the products. These products may short-circuit. If electrical shocks, smoke, fire, and/or accidents involving human life are anticipated when a short circuit occurs, then provide the following failsafe functions, as a minimum.

(1) Ensure the safety of the whole system by installing a protection circuit and a protection device.
(2) Ensure the safety of the whole system by installing a redundant circuit or another system to prevent a dual fault causing an unsafe status.

24 OTHER CAUTIONS

(1) This specification sheet is copyrighted. Reproduction of this data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices.
(2) Do not use the products for other purposes than those listed.
(3) Be sure to provide an appropriate fail-safe function on your product to prevent an additional damage that may be caused by the abnormal function or the failure of the product.
(4) This product has been manufactured without any ozone chemical controlled under the Montreal Protocol.
(5) These products are not intended for other uses, other than under the special conditions shown below. Before using these products under such special conditions, check their performance and reliability under the said special conditions carefully to determine whether or not they can be used in such a manner.
- In liquid, such as water, salt water, oil, alkali, or organic solvent, or in places where liquid may splash.

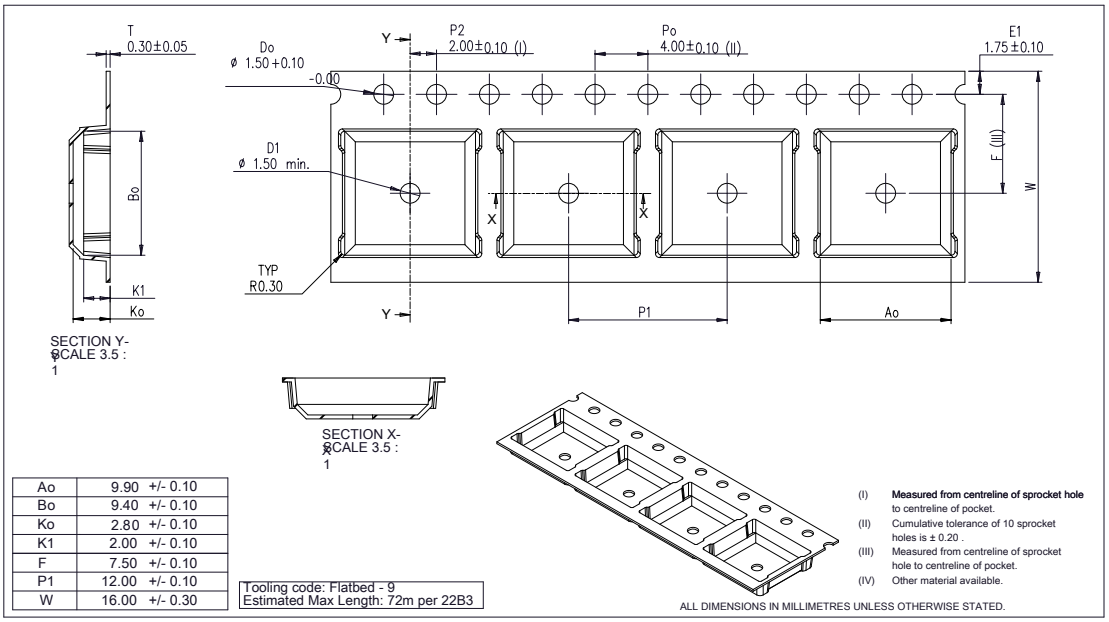
- In direct sunlight, outdoors, or in a dusty environment
- In an environment where condensation occurs.
- In an environment with a high concentration of harmful gas (e.g. salty air, HCl, Cl2, SO2, H2S, NH3, and NOX)

(6) If an abnormal voltage is applied due to a problem occurring in other components or circuits, replace these products with new products because they may not be able to provide normal performance even if their electronic characteristics and appearances appear satisfactory.

(7) When you have any question or uncertainty, contact Panasonic.

25 PACKAGING

Tape Dimension



Ao	9.90 +/- 0.10
Bo	9.40 +/- 0.10
Ko	2.80 +/- 0.10
K1	2.00 +/- 0.10
F	7.50 +/- 0.10
P1	12.00 +/- 0.10
W	16.00 +/- 0.30

Tooling code: Flatbed - 9
Estimated Max Length: 72m per 22B3

Packing in Tape