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Specification for Production

Applicant / Manufacturer Hardware	Panasonic Industrial Devices Europe GmbH Zeppelinstrasse 19 21337 Lüneburg Germany
Applicant / Manufacturer Software	Please refer to chapter 32 / 32.1 Information regarding Software Versions
Software Version	Please refer to chapter 32 / 32.1 Information regarding Software Versions

By purchase of any of products described in this document the customer accepts the document's validity and declares their agreement and understanding of its contents and recommendations. Panasonic reserves the right to make changes as required without notification.

TABLE OF CONTENTS

1. SCOPE OF THIS DOCUMENT

This product specification applies to Panasonic's WLAN IEEE 802.11 b/g/n 2x2 MIMO and Bluetooth®[1] 4.0 High Speed / Low Energy - Radio Module with series number PAN9055 / PAN9045 (88W8797 from Marvell®).

2. HISTORY FOR THIS DOCUMENT

Revision	Date	Modification / Remarks
0.1	July 2014	1st preliminary version

3. DATA SHEET STATUS

This data sheet contains the PRELIMINARY specification. Supplementary data will be published at a later date.

Panasonic reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Please consult the most recently issued data sheet before initiating or completing a design.

4. RELATED DOCUMENTS

For an update, please search in the suitable homepage.

[1] PAN9055 and PAN9045 Design-Guide
TBP

[2] Semiconductor Datasheet
88W8797 from Marvell®

[3] Application Note Land Grid Array
http://www.pideu.panasonic.de/pdf/184ext.pdf

[4] REACH and RoHS Certificate
http://www.pideu.panasonic.de/pdf/182ext2.jpg

[1] Bluetooth is a registered trademark of the Bluetooth Special Interest Group.

5. KEY FEATURES

- Surface Mount Type 26.0 x 13.5 x 2.4 mm³
- Wireless Local Area Network (WLAN) and Bluetooth technology
- Operating in the 2.4GHz ISM band
- WLAN 2x2 MIMO operation
- Supports IEEE 802.11
  - IEEE 802.11b/g payload data rates
  - IEEE 802.11n high throughput data rates
  - IEEE 802.11i security standards AES-CCMP, WEP, TKIP, AES-CMAC and WAPI
  - IEEE 802.11e Quality of Service (QoS)
- Supports Bluetooth 4.0 + HS
  - Bluetooth Classic with BT Class 2 or Class 1.5 support
  - Bluetooth High Speed (BT 3.0)
  - Bluetooth Low Energy (BLE)
- Coexistence with cellular and other 2.4GHz on-chip radios
- WLAN Tx power up to +18 dBm (IEEE 802.11b CCK) and +14 dBm (IEEE 802.11g ODFM)
- WLAN High Rx sensitivity
  - -98dBm (IEEE 802.11b DSSS 1Mbps)
  - -76dBm (IEEE 802.11g OFDM 54Mbps)
  - -74dBm (IEEE 802.11n MCS7 HT20 65Mbps)
  - -71dBm (IEEE 802.11n MCS7 HT40 135Mbps)
- Marvell® 88W8797 WLAN / Bluetooth System-on-Chip (SoC) solution inside
- High performance low power CPU core
- Four powerful independent DMA channels
- Power Management Unit with internal Sleep Clock (for Power Save Mode)
- Internal crystal oscillator (38.4MHz)
- USB 2.0, SDIO 3.0 and HS-UART interface
- Integrated shielding to resist EMI
- Manufactured in conformance with RoHS

6. APPLICATIONS FOR THE MODULE

All Embedded Wireless Applications

- Platform
- Consumer Electronic
- Portable Application
- Health & Fitness
- Smart Energy
- Game Console, Imaging
- Home AV Entertainment, TV, Set-top Boxes, Media Servers
- Handsets, AV Device, Tablet, eBook
- Home Gateways, Medical devices
- Thermostat, Control panels

7. WIRELESS LOCAL AREA NETWORK (WLAN)

Wireless Local Area Network (WLAN) is indicating a local radio network meant as a part of the standard IEEE 802.11 family. The IEEE 802.11 is an international standard describing the wireless network. The standard defines the lower layers of the OSI model for wireless communication with the Physical Layer (PHY) and the Data Link Layer (DLL) with its two sub-layers Logical Link Control (LLC) and Media Access Control (MAC). It makes it possible to use any protocol over a IEEE 802.11 wireless network as used at an Ethernet network. Basically WLAN networks using two operating modes for connecting station computers (STA) equipped with a wireless network adapter. The first one is the infrastructure mode where the wireless clients are connected via one or more access points (AP) to a wired network. In this case the network is configured with the same Service Set Identifier (SSID) network name in order to communicate. The second one is the Ad-hoc mode where wireless clients are connected without any access point to the internet.

WLAN devices typically have a higher transmit power to cover a radio range about 100m. Furthermore WLAN is commonly used to transmit high throughput data using upon other the Orthogonal Frequency Division Multiplexing (OFDM) modulation technique. The Carrier Sense Multiple Access with Collosion Avoidance (CSMA/CA) mechanism enables the parallel access of more than one device to the media of a IEEE 802.11 network. By implementation of security mechanisms like Adavanced Encryption Standard (AES) with Counter Mode CBC-MAC Protocol (CCMP) or Cipher-Based Message Authentication Code (CMAC) and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) the network is supporting the security standard IEEE 802.11i. Video, voice and multimedia applications are supported by the IEEE 802.11e Quality of Service amendment.

8. BLUETOOTH 4.0

Bluetooth Low Energy (BLE) is a part of Bluetooth Version 4.0, which covers both BLE as well as BT Classic 2.1 and 3.0. If both are implemented in one device it is called dual mode. Dual mode chips implement the low energy specification, providing connectivity to battery applications. Dual mode combines low energy with the power of classic Bluetooth and are likely to become a de facto feature in almost all new Bluetooth enabled cellular phones, computers or portable communication nodes.

Bluetooth Low Energy (BLE) is not backwards compatible with previous Bluetooth classic standards (2.1+EDR or 3.0). Dual mode Bluetooth 4.0 is backwards compatible but is not practical for low power devices but targeted to gateway products.

9. DESCRIPTION FOR THE MODULE

The ENWF9101x1yF is a 2.4GHz ISM band wireless radio module for implementing WLAN and Bluetooth functionality into various electronic devices. A block diagram can be found in chapter 17.

The ENWF9101x1yF is a cost-effective, low-power operation, system-on-chip (SoC) solution for WLAN and Bluetooth applications. It enables wireless network adapters and cards to be built with low total bill-of-material costs. The ENWF9101x1yF combines an excellent IEEE 802.11 and BT4.0 wireless radio, baseband processor, medium access controller, encryption unit, CPU, boot ROM with patching capability, internal SRAM, in-system programmable flash memory and many other powerful supporting features and peripherals. The low-power operation supporting deep sleep and standby modes by using the on-board power management unit. The ENWF9101x1yF is suitable for wireless network systems based on WLAN IEEE 802.11 b/g/n and Bluetooth BT4.0 (2.4GHz) where small form factor, highly integration, high throughput data rates and low RF expertise are required.

Panasonic offers the software package supporting various Fedora Core Kernel versions. It includes the WLAN/BT SoC Firmware binary that powers the WLAN/BT SoC for client (STA), micro access point (uAP), Ad-hoc mode (Wi-Fi direct), Bluetooth Classic, High Speed and Low Energy (BLE) applications. In addition it includes the HOST Driver-Firmware Interface (API) which represents the interface between the host driver and SoC firmware.

For WLAN the Driver-Firmware Interface handles all 802.11 MAC management tasks by converting standard 802.3 frames to the SoC firmware to transmit over the wireless link as 802.11 frames and processes the received 802.11 frames and converts them into 802.3 frames before forwarding them to the host driver. The HOST driver is seperated in three modules. The Standard Ethernet driver, the 802.11 Extensions and the Hardware Interface Driver. The 802.11 Extensions module extends the Standard Ethernet driver in order to view and control the state of the WLAN adapter. For Bluetooth the Driver-Firmware Interface handles the BT Baseband, Link Manager Protocol (LMP) and HCI functionality in cooperation with the CPU.

The Hardware Interface Driver controls the hardware interface on the HOST side. Furtheron the software package from Marvell® consists of various applications, demonstrations and utilities.

Refer to [1] PAN9055 and PAN9045 Design-Guide and chapter 32. Ordering Information.

Please contact your local sales office for further details on additional options and services:

www.panasonic.com/rfmodules for the US,

http://industrial.panasonic.com/eu/i/29606/wireless_modules/wireless_modules.html for EU

or write an e-mail to wireless@eu.panasonic.com.

10. DIFFERENCE PAN9055 TO PAN9045

The PAN9045 is the non antenna version with two bottom pads where the PAN9055 is the version with two antennas.

11. DETAILED DESCRIPTION

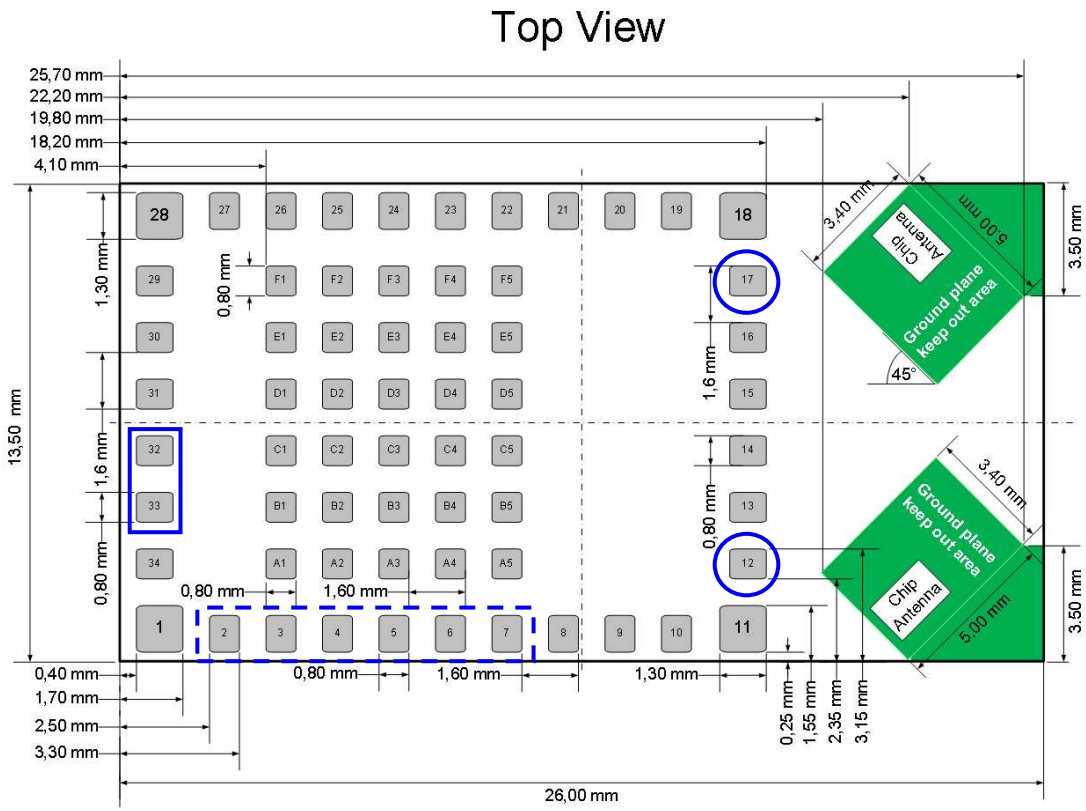
11.1. PAN9055 / PAN9045 TERMINAL LAYOUT

The USB pins are marked with a blue rectangular box.

The SDIO pins are marked with a blue dashed rectangular box.

The two PAN9045 antenna pins are marked with blue circles.

Top View, Application PCB



11.2. PAN9055 / PAN9045 COMMON TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description
1	GND	Ground Pin	Connect to Ground
2..7	…	…	… for SDIO specific terminals see chapter 11.3
8	RESETn	Input Signal	Reset, active-low
9	PDn	Input Signal	Power down, active-low
10	S_CSN / CON2	Output / Input	S_CSN: Chip Select for external SPI EEPROM, chip select from the SoC CON2: Firmware Boot option
11	GND	Ground Pin	Connect to Ground
12	NC	NC	… for PAN9045 see chapter 11.4
13	GND	Ground Pin	Connect to Ground
14	GND	Ground Pin	Connect to Ground
15	GND	Ground Pin	Connect to Ground
16	GND	Ground Pin	Connect to Ground
17	NC	NC	… for PAN9045 see chapter 11.4
18	GND	Ground Pin	Connect to Ground
19	3.3V RF	Power	3.0V – 3.6V power supply connection
20	3.3V RF	Power	3.0V – 3.6V power supply connection
21	CON0	Digital I/O	CON0: Firmware Boot option see chapter
22	CON1	Digital I/O	CON1: Firmware Boot option see chapter
23	UART_SOUT	Output Signal	Serial data output to modem, data set, or peripheral device
24	UART_SIN	Input Signal	Serial data input from modem, data set, or peripheral device
25	UART_RTS	Output Signal	Request-to-Send output to modem, data set, or peripheral device (active low)
26	UART_CTS	Input Signal	Clear-to-Send input from modem, data set, or peripheral device (active low)
27	GPIO4	Digital I/O	Port 4 – GPIO[4]
28	GND	Ground Pin	Connect to Ground
29	3.3V	Power	3.0V – 3.6V power supply connection
30	3.3V	Power	3.0V – 3.6V power supply connection
31	3.3V USB	Power	3.0V – 3.6V power supply connection
32	USB_DMNS	D-	USB Bus Data Minus
33	USB_DPLS	D+	USB Bus Data Plus
34	SD_VIO	Power	1.8V or 3.3V Digital I/O SDIO Power Supply
A1	TMS / BT_FREQ	Input Signal	TMS: JTAG controller select BT_FREQ: Information BT using channel which overlaps WLAN channel or not
A2	TDO / BT_REQ	Output / Input	TDO: JTAG test data output / BT_REQ: BT device request access to medium
A3	S_WB	Input Signal	Serial Read/Write Control Signal input, SPI EEPROM serial data to the SoC
A4	S_CLK	Output Signal	Serial Clock Signal output, SPI EEPROM serial clock from the SoC
A5	S_DAT	Output Signal	Serial Data output, SPI EEPROM serial data from the SoC
B1	TCK / BT_GRANTn	Input / Output	TCK: JTAG test clock BT_GRANTn: Indicate permission to transmit, low BT can transmit
B2	TDI / BT_STATE	Input Signal	TDI: JTAG test data input BT_STATE: Information BT_REQ priority (1- or 2-bit) and direction BT RX/TX
B3	GND	Ground Pin	Connect to Ground
B4	GND	Ground Pin	Connect to Ground
B5	GND	Ground Pin	Connect to Ground
C1	CHIP_WAKEUP	Digital I/O	Port 18 – optional GPIO[18] or Host-to-Chip wake-up
C2	I2S2_LRCLK	Output / Input	I^2S Audio Left/Right Clock, Master mode as output, Slave mode as input
C3	GND	Ground Pin	Connect to Ground
C4	GND	Ground Pin	Connect to Ground
C5	GND	Ground Pin	Connect to Ground
D1	I2S2_DOUT	Output Signal	I^2S Audio output data (for playback)
D2	I2S2_DIN	Input Signal	I^2S Audio input data (for recording)
D3	PCM_SYNC	Input / Output	PCM Sync Pulse Signal, output if PCM Master, input if PCM Slave
D4	GND	Ground Pin	Connect to Ground
D5	GND	Ground Pin	Connect to Ground
E1	I2S2_BCLK	Input / Output	I^2S Audio Bit Clock, Master mode as output, Slave mode as input
E2	LED1	Digital Output	Port 17 – LED output with typ. 10mA drive capability
E3	PCM_CLK	Input / Output	PCM Clock Signal, output if PCM Master, input if PCM Slave
E4	GND	Ground Pin	Connect to Ground
E5	PCM_DOUT	Output Signal	PCM Data Output Signal
F1	HOST_WAKEUP	Digital I/O	Port 16 – optional GPIO[16] or Chip-to-Host wake-up
F2	LED0	Digital Output	Port 1 – LED output with typ. 10mA drive capability
F3	PCM_DIN	Input Signal	PCM Data Input Signal
F4	PCM_MCLK	Output Signal	PCM Clock Signal, optional clock used for some codec derived from PCM_CLK
F5	GND	Ground Pin	Connect to Ground

11.3. PAN9055 / PAN9045 SDIO SPECIFIC TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description		
			4-bit mode	1-bit mode	SPI mode
2	SD_CMD	Digital I/O	-	Command Line	Data Input
3	SD_DAT[0]	Digital I/O	Data Line bit [0]	Data Line	Data Output
4	SD_DAT[1]	Digital I/O	Data Line bit [1]	Interrupt	Interrupt
5	SD_DAT[2]	Digital I/O	Data Line bit [2] or … Read Wait (optional)		Reserved
6	SD_DAT[3]	Digital I/O	Data Line bit [3]	Not used	Chip Select, active low
7	SD_CLK	Digital I/O	Clock	Clock	Clock

11.4. PAN9045 RF-TERMINAL PIN-CONFIGURATIONS

No	Pin Name	Pin Type	Description
12	RF_B	RF Port B	50Ω bottom pad
17	RF_A	RF Port A	50Ω bottom pad

12. GENERAL FEATURES

- Embedded WLAN / BT SoC with following features:
  - Integrated CPU with maximum clock speed of 256 MHz
  - Single-chip integration of IEEE 802.11 2x2 MIMO and BT4.0 wireless radio, baseband, MAC, CPU, memory and HOST interface
  - SRAM for Tx frame queues and Rx data buffer
  - Boot ROM and ROM patching capability
  - Independent Four-Channel Direct Memory Access (DMA)
  - Low power operation supporting deep sleep and stand-by modes
  - Optional power management with internal sleep clock crystal unit for near zero deep sleep

13. HOST INTERFACES

13.1. USB 2.0 INTERFACE

- Compliant with the Universal Serial Bus Specification, Revision 2.0
- Allows HOST controller using USB cable bus and USB 2.0 device interface
- High/full speed operation with (480/12 Mbps)
- Suspend / host resume / device resume (remote wake-up)
- Supports Link Power Management (LPM), corresponding host resume or device resume (remote wakeup) to exit from L1 sleep state
- USB 2.0 device interface with integrated level shifter for 3.3V signal level

13.2. SDIO 3.0 INTERFACE

- Supports SDIO 3.0 Standard
- SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification
- Supports SPI, 1-bit SDIO and 4-bit SDIO transfer modes at the full clock range of 0 to 100MHz
- Special interrupt register for information exchange
- Allows card to interrupt host
- SoC acts as a device on a SDIO bus

13.3. HIGH-SPEED UART INTERFACE

- Supports high-speed Universal Asynchronous Receiver / Transmitter (UART) interface
- Compliant with the industry standard 16550 specification
- High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data
- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit, receive and two for flow control
- Interrupt triggers for low-power, high throughput operation

14. PERIPHERAL BUS INTERFACE

- Embedded SoC with following features:
  - Clocked Serial Unit (CSU)
    - 2-Wire Serial Interface (TWSI)
    - 1-Wire Serial Interface
    - SPI Serial (EEPROM) Interface
  - General-Purpose I/O (GPIO) Interface
    - User-defined GPIOs, I/O configured to either input or output
    - GPIOs independently controlled
    - Two GPIOs with LED output functionality
      - LED Pulse Stretching to observe short duration of status events
      - Two software controlled blink rates to indicate events
  - One-Time Programmable Memory (OTP)
    - Storing calibration data and hardware information of the device
    - Programmed during production process of device
    - Device performs calibration when it is powered up

15. AUDIO INTERFACE FEATURES

15.1. AUDIO CODEC INTERFACE

- Class D Audio Amplifier
- I^2S (Inter-IC Sound) interface for audio data connection to ADC and DAC
- Master and slave mode for I^2S, MSB and LSB audio interfaces
- Tri-state I^2S interface capability

15.2. PCM INTERFACE

- Master or slave mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- Short frame and long frame synchronization
- Tri-state PCM interface capability

16. WLAN FEATURES

16.1. IEEE 802.11 / STANDARDS

- 802.11 data rates 1 and 2 Mbps (DSSS)
- 802.11b data rates 5.5 and 11 Mbps (CCK)
- 802.11g data rates 6, 9, 12, 18, 24, 36, 48 and 54 Mbps (OFDM)
- 802.11b/g performance enhancements
- 802.11n compliant with maximum data rates up to 145 Mbps (20 MHz channel) and 300 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11i enhanced security (WEP, WPA, WPA2)
- 802.11k radio resource measurement
- 802.11n block acknowledgement extensions
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi Direct connectivity

16.2. WLAN MAC

- Ad-Hoc and Infrastructure Modes
- RTS/CTS for operation und DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- WLAN SoC with Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- 20/40 MHz channel coexistence
- Reduced Inter-Frame Spacing (RIFS) receive
- Management Information Base (MIB) counter
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgement with 802.11n extensions
- Beamforming
  - Supports beamforming to 802.11n MIMO and SISO devices
  - 802.11n explicit beamformer, supports NDP and Stagger sounding
  - 802.11n explicit beamformee, supports immediate feedback generation using un-compress and compress steering matrix or delayed feedback of all feedback types
- TIM frame transition
- Multiple-BSSID and Multiple-Station operation
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Marvell® Mobile Hotspot technology (MMH)

16.3. WLAN BASEBAND

- 802.11n 2x2 MIMO (WLAN SoC with MIMO RF radio)
- Backward compatibility with legacy 802.11b/g technology
- WLAN / Bluetooth LNA sharing
- PHY data rates up to 300 Mbps (802.11n – MCS15)
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel and 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- Modulation and Coding Scheme MCS 0 ~ 15 and MCS 32 (duplicate 6 Mbps)
- Radio resource measurement
- Optional 802.11n MIMO features:
  - 20/40 MHz coexistence
  - 1 spatial stream Space-Time-Block-Coding (STBC) reception and transmission
  - Short Guard Interval
  - RIFS on receive path
  - Implicit beamforming
  - Explicit beamformer and beamformee support
  - Greenfield Tx/Rx
- Power save features

16.4. WLAN RADIO

- 20 and 40 MHz channel bandwidth
- Shared WLAN / Bluetooth receive input scheme for 2.4 GHz band
- Embedded WLAN SoC with following features:
  - Direct conversion radio (no SAW filter)
  - Closed/Open loop power control (0.5 dB step increments)
  - Optimized Tx gain distribution for linearity and noise performance
  - Fine channel step with AFC (adaptive frequency control)

16.5. WLAN RF PATH

- Shared WLAN / Bluetooth receive input scheme for 2.4 GHz band
- Two RF pathes with following features:
  - Two separate Front-End-Modules (FEM) for each RF path
  - 1st FEM with integrated 2.4GHz Tx/Rx switch, Power Amplifier (PA) and Low Noise Amplifier (LNA) path
  - 2nd FEM with integrated 2.4GHz Tx/Rx/BT switch, Power Amplifier (PA), Low Noise Amplifier (LNA) and RF Bypass path
  - Gain selectable LNAs with optimized noise figure and power consumption
  - Power Amplifiers with power control

16.6. WLAN ENCRYPTION

- Embedded WLAN SoC with following features:
  - WEP 64-bit and 128-bit encryption with hardware TKIP processing (WPA)
  - AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
  - Enhanced AES engine performance
  - AES-Chipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
  - WLAN Authentication and Privacy Infrastructure (WAPI)

17. BLUETOOTH FEATURES

17.1. GENERAL

- Supports Bluetooth 4.0 + High Speed
- Shared Tx/Rx path for Bluetooth
- Digital Audio Interface including PCM interface for voice applications and I^2S for digital stereo applications
- BDR/EDR, BLE and WLAN coexistence
- WLAN/Bluetooth Coexistence (BCA) protocol support

17.2. BLUETOOTH CLASSIC

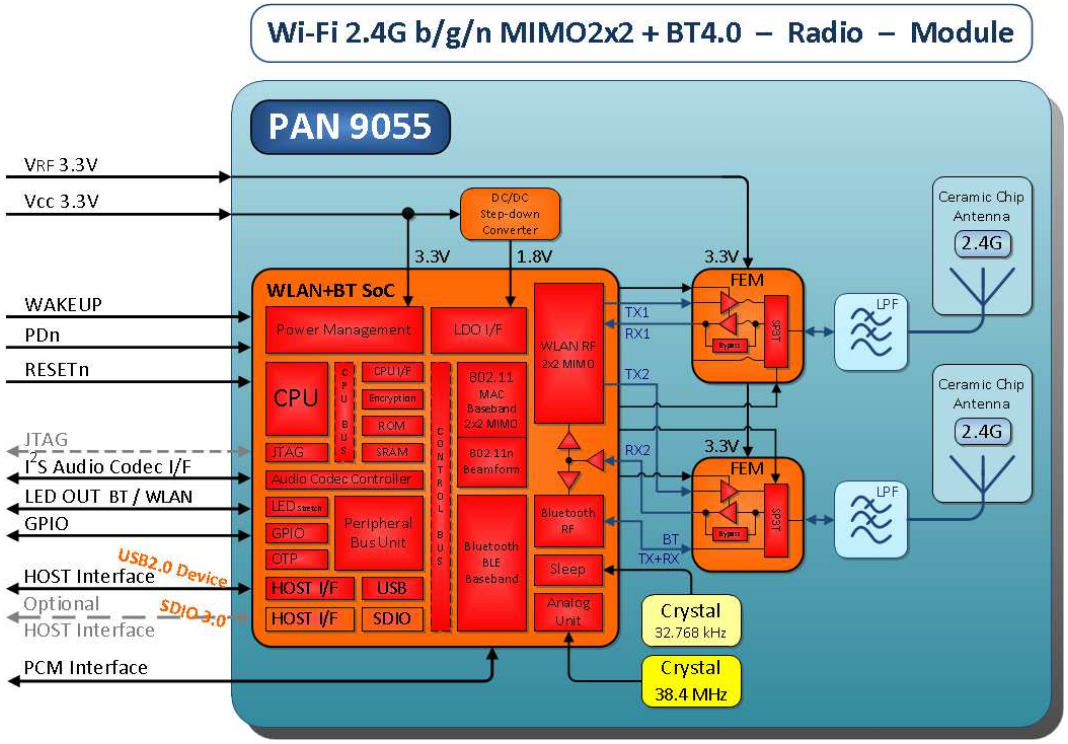
- Bluetooth Classic with BT Class 2 or Class 1.5 support
- Bluetooth High Speed (BT 3.0)
- Baseband and radio Basic Data Rate (BDR) and Enhanced Data Rate (EDR) packet types with 1Mbps (GFSK), 2Mbps (π/4-DQPSK) and 3Mbps (8DPSK)
- Fully functional Bluetooth baseband with Adaptive Frequency Hopping (AFH), forward error correction, header error control, access code correlation, CRC, encryption bit stream generation and whitening
- Adaptive Frequency Hopping (AFH) including Packet Loss Rate (PLR) and RSSI
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard UART and SDIO HCI transport layer
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanism (i.e. hold, sniff modes and sniff-sub rating)
- Enhanced low power scan mode
- Enhanced Power Control (EPC)
- Channel Quality Driven (CQD) data rate
- SBC off load for A2DP streaming
- Wideband Speech (WBS) support (1 WBS link)

17.3. BLUETOOTH LOW ENERGY (BLE)

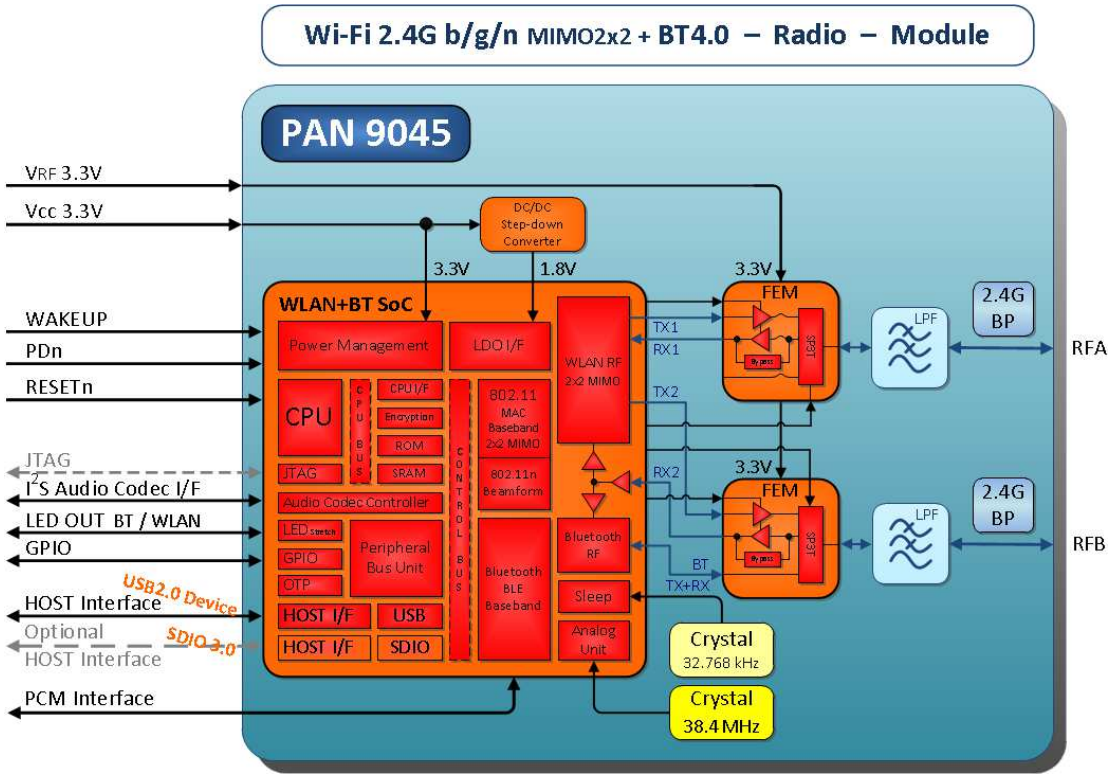
- Advertiser, Scanner, Initiator, Master and Slave roles support (connects up to 16 links)
- Shared RF with BDR/EDR
- Encryption AES support
- Hardware support for intelligent Adaptive Frequency Hopping (AFH)

18. PAN9055 / PAN9045 BLOCK DIAGRAM

18.1. PAN9055 VARIANT



18.2. PAN9045 VARIANT



19. KEY PARTS LIST

Part Name	Material
P.W.Board	Glass cloth epoxide resin with gold plating
Casing	Material: C7521 or ZSNC S1S8 8/8, thickness 0.30mm
IC part name	88W8797 (Marvell®, www.marvell.com)

20. TEST CONDITIONS

Measurements shall be made under operating free-air temperature range unless otherwise specified.

Temperature	25 ± 10°C
Humidity	40 to 85%RH
Supply Voltage	3.3V

21. GENERAL REQUIREMENTS AND OPERATION

All specifications are over temperature and process, unless indicated otherwise.

21.1. ABSOLUTE MAXIMUM RATINGS

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the module will result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{STOR}	Storage temperature		-40		+125	°C
V_{ESD}	ESD robustness	All pads, according to human-body model, JEDEC STD 22, method A114			1000	V
		According to charged-device model, JEDEC STD 22, method C101			500	V
P_{RF}	RF input level				+20	dBm
V_{DDMAX}	Maximum voltage	Maximum power supply voltage from any pin with respect to V_{SS} (GND)	-0.3		3.9	V
V_{IO}	Voltage on any digital pin	GPIOs, PDn, RESETn, Coex I/F	-0.3		V_{DDMAX}	V
V_{USBMAX}	USB Maximum voltage	Maximum power supply voltage from any pin with respect to V_{SS} (GND)	-0.3		3.9	V
V_{IO_SDMAX}	3V3 SDIO Maximum voltage	Maximum power supply voltage from any pin with respect to V_{SS} (GND)	-0.3		3.9	V
	1V8 SDIO Maximum voltage		-0.3		2.1	V

21.2. RECOMMENDED OPERATING CONDITIONS

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the module will result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_A	Ambient operating temperature range	Commercial Grade (refer to chapter 32.)	0		+70	°C
		Extended Grade (refer to chapter 32.)	-30		+85	°C
V_{DD}	3V3 Supply voltage [2]	Voltage on pins 19 / 20 (3.3V RF), 29 / 30 (3.3V) I/O supply voltage VIO internally connected to V_{DD}	3.0	3.3	3.6	V
V_{USB}	3V3 USB Supply voltage [2]	Voltage on pin 31 (3.3V USB) Supply voltage V_{USB} connected to 3.3V USB	3.0	3.3	3.6	V
V_{IO_SD}	3V3 SDIO Supply voltage [2]	Voltage on pin 34 (SD_VIO) Supply voltage V_{IO_SD} connected to SD_VIO	3.0	3.3	3.6	V
	1V8 SDIO Supply voltage [2]	Voltage on pin 34 (SD_VIO) Supply voltage V_{IO_SD} connected to SD_VIO	1.6	1.8	2.0	V

[2] The supply current must be limited to max. 1A

21.3. DIGITAL PIN CHARACTERISTICS

21.3.1. VIO with V_{DD} 3.3V Operation for GPIO's

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage [3]	3.3V Operation ($V_{IO} = V_{DD}$)	$0.7V_{DD}$		$V_{DD}+0.3$	V
V_{IL}	Low level input voltage [3]	3.3V Operation ($V_{IO} = V_{DD}$)	-0.3		$0.3V_{DD}$	V
V_{HYS}	Input hysteresis voltage [3]	3.3V Operation ($V_{IO} = V_{DD}$)	200			mV
V_{OH}	High level output voltage [3]	3.3V Operation ($V_{IO} = V_{DD}$)	$V_{DD} - 0.4$			V
V_{OL}	Low level output voltage [3]	3.3V Operation ($V_{IO} = V_{DD}$)			0.4	V

21.3.2. SD_VIO 1.8V Operation for SDIO I/F

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage [3]	1.8V Operation (V_{IO_SD} = 1.8V)	$0.7V_{IO\_SD}$		$V_{IO\_SD}+0.3$	V
V_{IL}	Low level input voltage [3]	1.8V Operation (V_{IO_SD} = 1.8V)	-0.3		$0.3V_{IO\_SD}$	V
V_{HYS}	Input hysteresis voltage [3]	1.8V Operation (V_{IO_SD} = 1.8V)	150			mV
V_{OH}	High level output voltage [3]	1.8V Operation (V_{IO_SD} = 1.8V)	V_{IO_SD} – 0.4			V
V_{OL}	Low level output voltage [3]	1.8V Operation (V_{IO_SD} = 1.8V)			0.4	V

21.3.1. SD_VIO 3.3V Operation for SDIO I/F

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage [3]	3.3V Operation (V_{IO_SD} = 3.3V)	$0.7V_{IO\_SD}$		$V_{IO\_SD}+0.3$	V
V_{IL}	Low level input voltage [3]	3.3V Operation (V_{IO_SD} = 3.3V)	-0.3		$0.3V_{IO\_SD}$	V
V_{HYS}	Input hysteresis voltage [3]	3.3V Operation (V_{IO_SD} = 3.3V)	200			mV
V_{OH}	High level output voltage [3]	3.3V Operation (V_{IO_SD} = 3.3V)	V_{IO_SD} – 0.4			V
V_{OL}	Low level output voltage [3]	3.3V Operation (V_{IO_SD} = 3.3V)			0.4	V

[3] The capacitive load should not be larger than 50 pF for all I/O's when using the default driver strength settings. Generally, large capacitance loads increase the overall current consumption.

21.4. ELECTRICAL CHARACERISTICS

The current consumption depends on the user scenario and the setup and timing in the power modes. Assume V_{DD} = 3.3V, T_{amb} = 25°C if nothing else stated

21.4.1. Current consumption WLAN and Bluetooth with USB I/F

Symbol	Parameter Current Consumption	Mode	Condition	Min.	Typ.	Max.	Units
$I_{TX\ WLAN}$	Active Transmit [4]	WLAN [5]	P_{TX} = +18 dBm for 802.11b @ 11 Mbps		TBD		mA
			P_{TX} = +14 dBm for 802.11g @ 54 Mbps				mA
			P_{TX} = +13 dBm 802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			P_{TX} = +13 dBm 802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			P_{TX} = +13 dBm 802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			P_{TX} = +13 dBm 802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
$I_{RX\ WLAN}$	Active Receive [6]		802.11b @ 11 Mbps				mA
			802.11g @ 54 Mbps				mA
			802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
$I_{IEEE-PS}$	IEEE Power Save [7]		DTIM = 1 with beacon interval 100ms				µA
$I_{TX\ BT}$	Peak BT	BT (BDR) (EDR)	$P_{TX\ BT}$ = +4 dBm / USB Active				mA
			$P_{TX\ BT}$ = +4 dBm / USB Suspend [8]				mA
$I_{RX\ BT}$			USB Active				mA
			USB Suspend				mA
$I_{SCAN\ BT}$	Page / Inquiry Scan		1.28s @ normal mode				mA
$I_{SNIFF\ BT}$	ACL Sniff		1.28s				mA
$I_{A2DP\ BT}$	A2DP		BDR / EDR @ 330 Kbps (3M baud rate)				mA
$I_{TX\ BLE}$	Peak BLE	BLE	$P_{TX\ BLE}$ = +4 dBm				mA
$I_{RX\ BLE}$							mA
I_{PDn}	Power Down [9]	WLAN and BT	Grounding of PDn pin				µA
$I_{DeepSleep}$	Deep Sleep [10]		Low-power state used in sleep state				µA

[4] Peak values for specified output power level and data rate with UDP traffic between the AP and Device (STA).

[5] Using WLAN Client mode. Bluetooth is in Deep Sleep during this mode.

[6] Peak values for specified data rate with UDP traffic between the AP and DUT.

[7] In IEEE Power Save the device automatically wakes up on beacons. This is dependent on the DTIM value of the AP it is connected to. If it is a DTIM value of 1 along with a beacon interval of 100ms, the device wakes up every 100ms.

[8] USB Suspend Mode is valid only for the USB Host interface. The low-power device automatically enters a suspend state after 3ms of no bus activity.

[9] Power Down state can be achieved by grounding the PDn pin. All internal clocks are shut down, the registers and memory are not maintained. Upon exiting power down mode, a rest is automatically performed and a firmware re-download is required.

[10] It is a low-power mode used in the deep sleep state of power save mode. In this case the external reference clock and many WLAN SoC specific blocks are switched-off. Only an internal slow sleep clock is used to maintain register and memory states.

21.4.2. Current consumption WLAN and Bluetooth with SDIO I/F

Symbol	Parameter Current Consumption	Mode	Condition	Min.	Typ.	Max.	Units
$I_{TX\ WLAN}$	Active Transmit	WLAN	P_{TX} = +18 dBm for 802.11b @ 11 Mbps		TBD		mA
			P_{TX} = +14 dBm for 802.11g @ 54 Mbps				mA
			P_{TX} = +13 dBm 802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			P_{TX} = +13 dBm 802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			P_{TX} = +13 dBm 802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			P_{TX} = +13 dBm 802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
$I_{RX\ WLAN}$	Active Receive		802.11b @ 11 Mbps				mA
			802.11g @ 54 Mbps				mA
			802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
$I_{IEEE-PS}$	IEEE Power Save		DTIM = 1 with beacon interval 100ms				µA
$I_{TX\ BT}$	Peak BT	BT (BDR) (EDR)	$P_{TX\ BT}$ = +4 dBm / USB Active				mA
			$P_{TX\ BT}$ = +4 dBm / USB Suspend				mA
$I_{RX\ BT}$			USB Active				mA
			USB Suspend				mA
$I_{SCAN\ BT}$	Page / Inquiry Scan		1.28s @ normal mode				mA
$I_{SNIFF\ BT}$	ACL Sniff		1.28s				mA
$I_{A2DP\ BT}$	A2DP		BDR / EDR @ 330 Kbps (3M baud rate)				mA
$I_{TX\ BLE}$	Peak BLE	BLE	$P_{TX\ BLE}$ = +4 dBm				mA
$I_{RX\ BLE}$							mA
I_{PDn}	Power Down	WLAN and BT	Grounding of PDn pin				µA
$I_{DeepSleep}$	Deep Sleep		Low-power state used in sleep state				µA

21.5. INTERNAL OPERATING FREQUENCIES

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SYSCLK}	CPU clock speed	Refers to clock speed of WLAN SoC's CPU			256	MHz
	System / Encryption clock speed	Refers to clock speed of WLAN SoC's System and Encryption Unit			171	MHz
f_{REFCLK}	Crystal fundamental frequency	Frequency tolerance < ±10 ppm over operating temperature and process		38.4		MHz
$f_{SLEEPCLK}$	Sleep Clock frequency [11]	CMOS input clock signal type, ±250 ppm over temperature, aging and process		32.768		kHz

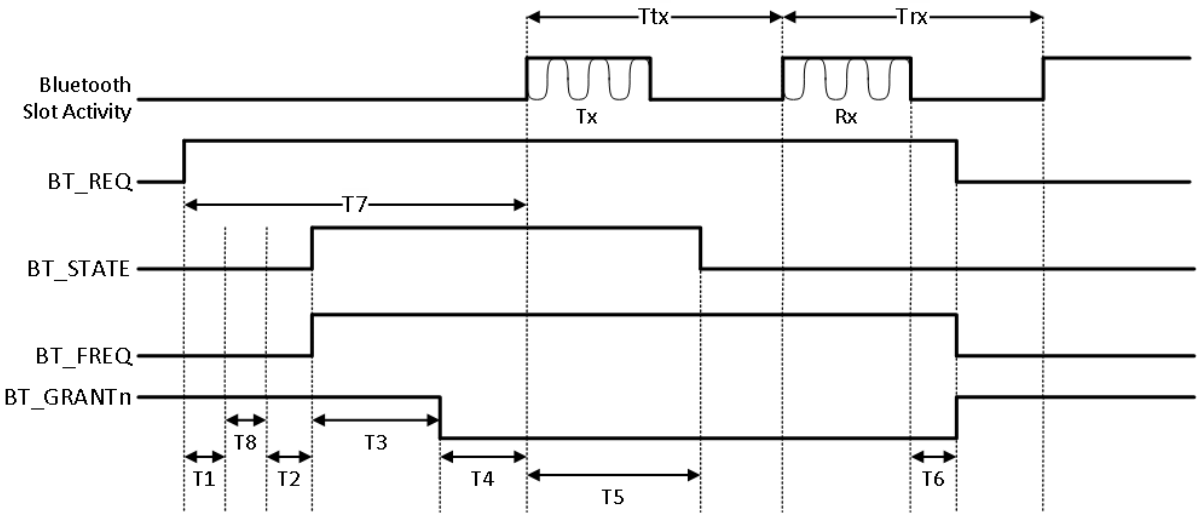
[11] Need to use module internal sleep clock crystal unit (optional) when low power operation mode near zero deep sleep is necessary. The internal sleep clock is not necessary for normal power modes.

21.6. COEXISTENCE INTERFACE SPECIFICATION

The Coexistence Interface pins are powered from the VIO voltage supply internally connected to V_{DD} = 3.3V. See Chapter 21.3 Digital Pin Characteristics for DC specification.

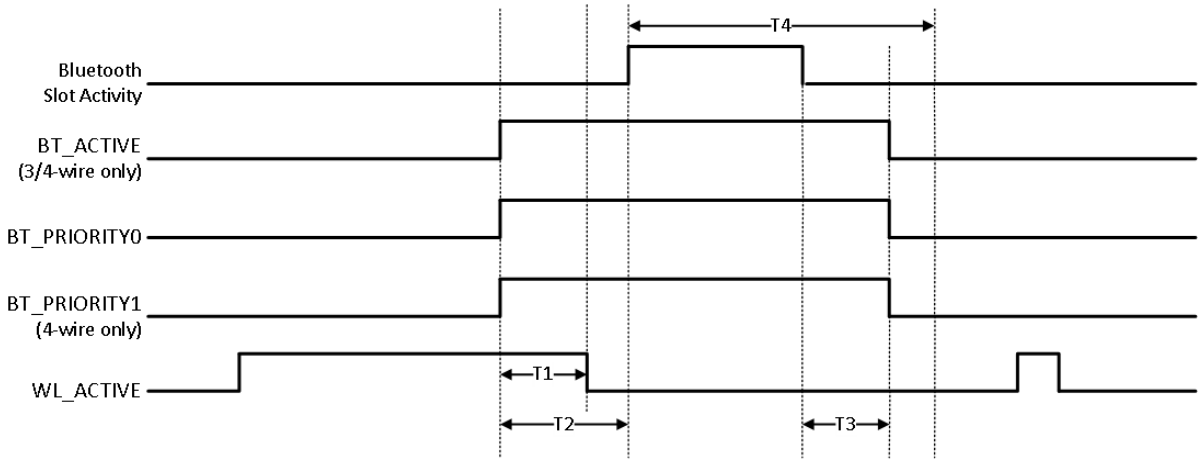
21.6.1. Marvell® 3/4-Wire Timing Data

Symbol	Parameter	Min.	Typ.	Max.	Units
T1	Priority[0] info is valid in BT_STATE on and after T1 from BT_REQ rise.	0	1	100	µs
T2	TxRx Info is valid in BT_STATE on and after T2. The BT_STATE must hold until there is any change of direction in the next slots.	2	19	100	µs
T3	Time from TxRx Info valid to BCA grant decision (T3 = T7 – T4 – T2 – T8 – T1).	2	40	594	µs
T4	BT_GRANTn needs to be valid T4 time before the upcoming slot. BT_GRANTn indicates Tx grant, and may also indicate Rx grant. Once a slot is granted, the subsequent slots are also granted unless there is a change in direction from Rx to Tx. Rx to Tx change always re-arbitrates.	2	80	594	µs
T5	TxRx Info for the next slot is valid on and after T5 to the start of the next slot. If direction remains the same for the next slot, then BT_STATE must not change during the current slot. If the direction changes for the next slot, the BT_STATE must change only after the last bit of Bluetooth data is transferred; otherwise the transfer may be disrupted.	5	40	600	µs
T6	The BT_REQ signal de-asserts T6 time after last bit of Bluetooth data is transferred.	0	15	25	µs
T7	Time from BT_REQ rise to first Bluetooth slot boundary. Bluetooth slot boundary is marked by first bit of Bluetooth data.	8	150	600	µs
T8	Optional Priority[1] information is valid in BT_STAT on and after T8. This time parameter only exists if BCA is configured for 2-bit priority on same BT_STATE pin. Otherwise, the start of T2 would come after T1.	2	10	100	µs
Ttx	Slot time (fixed fpr Bluetooth)		625		µs
Trx	Slot time (fixed fpr Bluetooth)		625		µs



21.6.2. WL_ACTIVE 2/3/4-Wire Timing Data

Symbol	Parameter	Min.	Typ.	Max.	Units
T1	• If WLAN can be stopped, WL_ACTIVE will de-asser prior to Bluetooth slot start (T1 < T2) • If the Bluetooth device samples WL_ACTIVE before starting priority transfer, WL_ACTIVE needs to de-assert earlier than the sampling time.	0		499	µs
T2	Time from BT_PRIORITY rise to start of Bluetooth activity.	20	50	499	µs
T3	Time from end of Bluetooth activity to BT_PRIORITY fall.	0	0	499	µs
T4	Slot time (fixed fpr Bluetooth)		625		µs



21.7. HOST INTERFACE SPECIFICATION

21.7.1. USB 2.0 Host Interface

The USB 2.0 Host Interface pins are powered from the 3.3V_USB voltage supply with 3.3V. It supports the high / full speed operation (480 / 12 Mbps) depending on the USB bus termination. The default mode is high speed operation.

21.7.1.1. Common Electrical Characteristics

Symbol	*Parameter*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Input Levels for Low / Full Speed						
V_{IH}	Input high voltage (driven)		2.0			V
V_{IHZ}	Input high voltage (floating)		2.7		3.6	V
V_{IL}	Input low voltage				0.8	V
V_{DI}	Differential input sensitivity		0.2			V
V_{CM}	Differential common mode range		0.8		2.5	V
Input Levels for High Speed						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)		525		625	mV
---	High-speed differential input signaling levels	Specified by eye pattern templates; see Section 7.1.7.2 in the USB 2.0 specification				
V_{HSCM}	High-speed data signaling common mode voltage range		-50		500	mV
Output Levels for Low / Full Speed						
V_{OL}	Output low voltage		0.0		0.3	V
V_{OH}	Output high voltage (driven)		2.8		3.6	V
V_{OSE1}	Output SE1 voltage		0.8			V
V_{CRS}	Output signal crossover voltage		1.3		2.0	V
Output Levels for High Speed						
V_{HSOI}	High-speed idle level		-10		10	mV
V_{HSOH}	High-speed data signaling high		360		440	mV
V_{HSOL}	High-speed data signaling low		-10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700		1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		-900		-500	mV