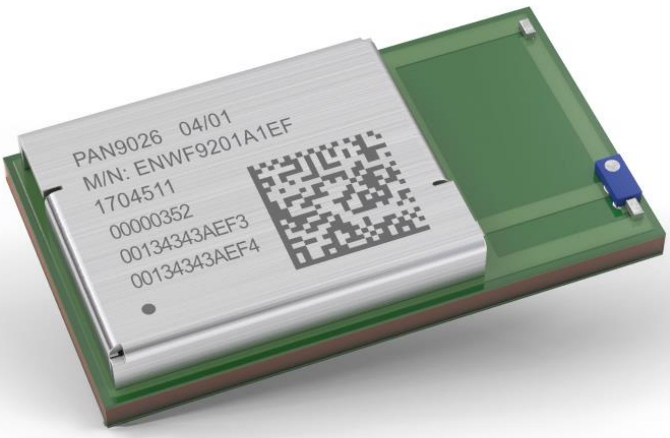
Panasonic

PAN9026

Wi-Fi Dual Band 2.4/5 GHz and Bluetooth Module

Product Specification

Rev. 1.0



Wireless Modules

Overview

The PAN9026 is a 2.4/5 GHz ISM band Wi-Fi and Bluetooth radio module, which includes a wireless radio for easy integration of Wi-Fi and Bluetooth connectivity into various electronic devices.

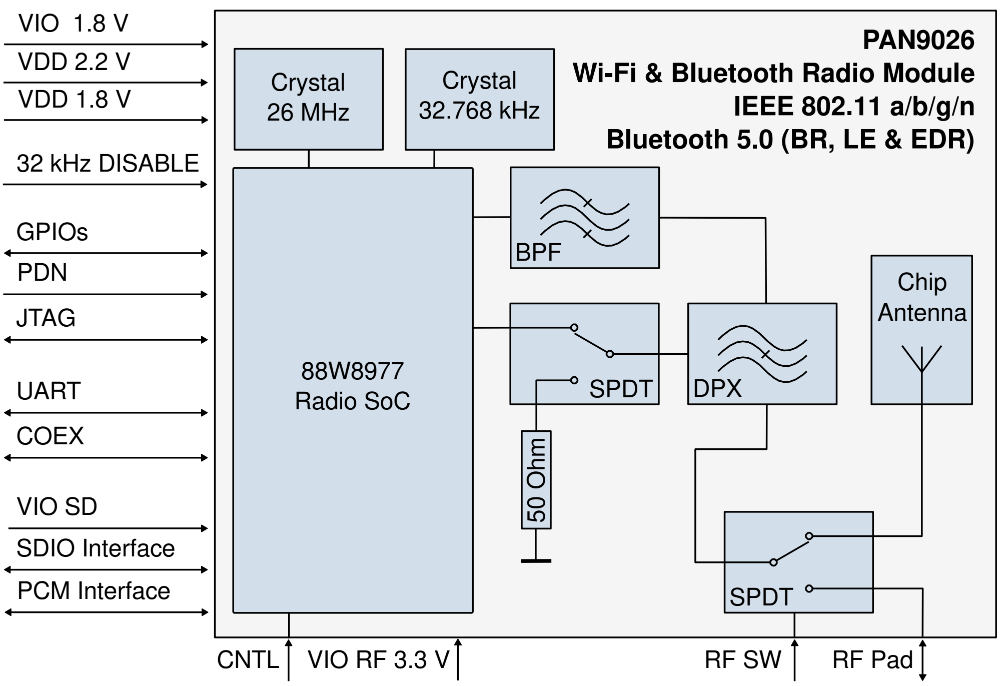
Features

- Dual band 2.4/5 GHz 802.11 a/b/g/n Wi-Fi/BT combo module
- Supports 802.11i security standards through AES, CCMP, and more security mechanisms
- 802.11e Quality of Service is supported for multimedia applications
- IEEE 802.11n-compliant, 1x1 spatial stream with data rates up to MCS7 150 Mbps
- Bluetooth 5.0 (includes LE)
- Dual simultaneous and independent WLAN and Bluetooth operation
- Dynamic Rapid Channel Switching (DRCS) for simultaneous operation in 2.4 GHz and 5 GHz bands
- Indoor location and navigation with IEEE 802.11mc
- Power management with sleep clock
- Coexistence interface for arbitration of co-located WLAN, Bluetooth, or Mobile Wireless System (e.g. LTE)
- Generic interfaces include SDIO 3.0 and high-speed UART for host processor connection
- Software Linux driver

Characteristics

- Surface Mount Type (SMT)
  17.5 mm x 10.0 mm x 2.6 mm
- Marvell® 88W8977 WLAN 2.4/5 GHz and Bluetooth single-chip solution inside
- TX Power +16 dBm @ 802.11b
- RX Sensitivity -98 dBm @ 802.11b DSSS 1 Mbps
- IEEE 802.11n 20 MHz and 40 MHz channel bandwidth
- Long and Short Guard Interval support
- Power supply 3.3 V, 2.2 V, 1.8 V
- Current consumption Wi-Fi typical 400 mA @ TX and 70 mA @ RX
- SDIO 1-bit or 4-bit
- Wide temperature range of -30 to +85 °C

Block Diagram



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If Engineering Samples are delivered to the customer, these samples have the status "Engineering Samples". This means that the design of this product is not yet concluded. Engineering Samples may be partially or fully functional, and they may differ from the published Product Specification.

Engineering Samples are not qualified and they are not to be used for reliability testing or series production.

Disclaimer

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Table of Contents

1 About This Document

1.1 Purpose and Audience

This Product Specification provides details on the functional, operational, and electrical characteristics of the Panasonic PAN9026 modules. It is intended for hardware design, application, and Original Equipment Manufacturers (OEM) engineers. The product is referred to as “the PAN9026” or “the module” within this document.

1.2 Revision History

Revision	Date	Modifications/Remarks
0.1	13.04.2017	First preliminary version
1.0	20.12.2017	Change to Bluetooth 5.0: ⇨ Features, 2.1 Block Diagram, 2.9 Bluetooth, 7.1 Ordering Information Change PM: ⇨ 2.3.1 Power Configuration Example with 3.3 V Host Operation Include values: ⇨ 4.3.2 Current Consumption, 4.4.3.2 Transmitter Section RF Characteristics Remove section: ⇨ 4.3.7.2 TDM Interface Additional models: ⇨ 7.1 Ordering Information Add section: ⇨ 7.2 Acronyms and Abbreviations

1.3 Use of Symbols

Symbol	Description
	**Note** Indicates important information for the proper use of the product. Non-observance can lead to errors.
	**Attention** Indicates important notes that, if not observed, can put the product’s functionality at risk.
⇨ [chapter number] [chapter title]	**Cross reference** Indicates cross references within the document. **Example:** Description of the symbols used in this document ⇨ 1.3 Use of Symbols.

1.4 Related Documents

Please refer to the Panasonic website for related documents ⇨ 7.3.2 Product Information.

2 Overview

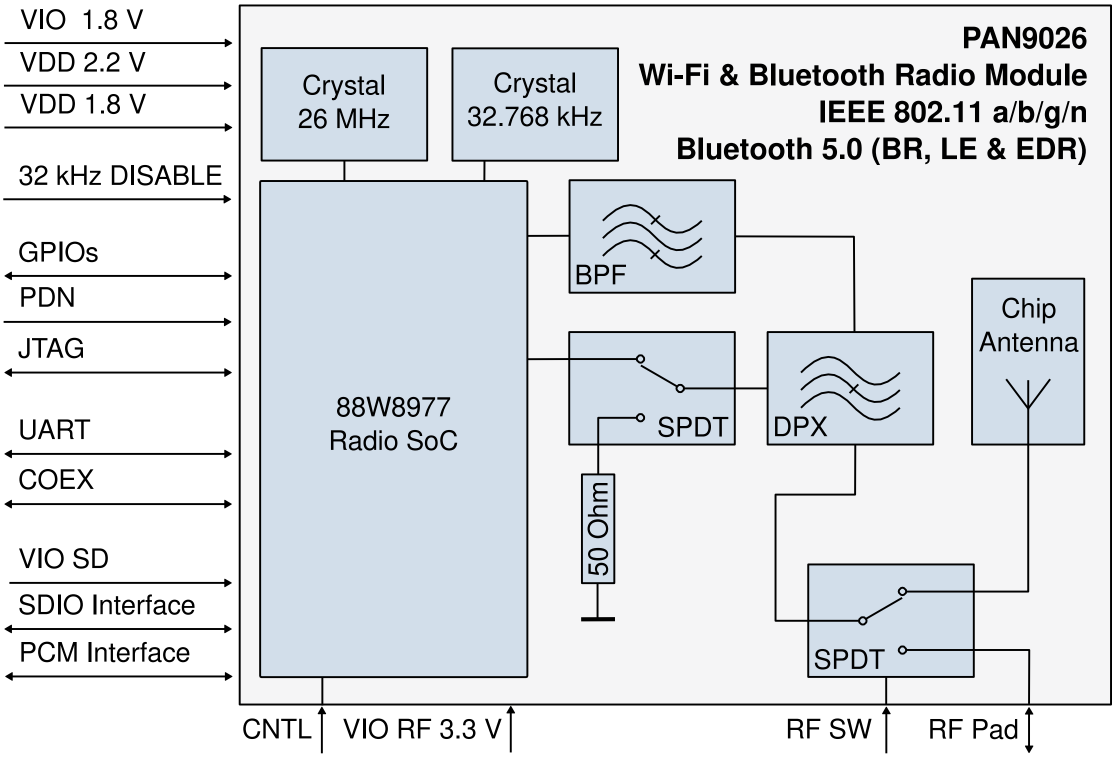
The PAN9026 is a dual band 2.4/5 GHz 802.11 a/b/g/n Wi-Fi radio module with integrated Bluetooth BR/EDR/LE, specifically designed for highly integrated and cost-effective applications. The simultaneous and independent operation of the two standards enables high data rates (802.11n) and low-power operation (Bluetooth Low Energy). Integrated power management, a fast dual-core CPU, 802.11i security standard support, and high-speed data interfaces deliver the performance for the speed, reliability, and quality requirements of next generation products. TX power calibration data and Wi-Fi/Bluetooth system parameters are pre-stored on the one-time-programmable memory of the PAN9026 during production at Panasonic. This simplifies passing the certification process for PAN9026 customers. Furthermore, the module reduces design, test, and calibration effort resulting in reduced time-to-market compared to discrete solutions.

Integrating Wi-Fi and Bluetooth wireless connectivity allows applications such as Smart Energy and home gateways to manage multiple devices and appliances. The combination of Wi-Fi and Bluetooth provides the highest flexibility for connectivity.

Please refer to the Panasonic website for related documents ⇨ 7.3.2 Product Information.

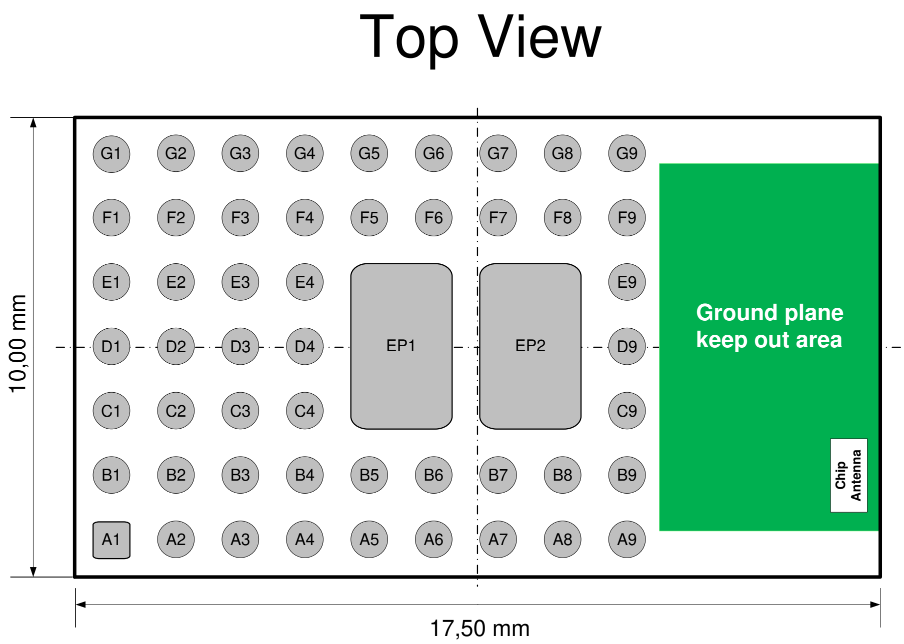
Further information on the variants and versions ⇨ 7.1 Ordering Information.

2.1 Block Diagram



2.2 Pin Configuration

Pin Assignment



Pin Functions

No	Pin Name	Pin Type	Description
A1 [1]	PCM_DOUT	Output signal	PCM data output signal
	IO5	Digital I/O	General Purpose IO – GPIO[5]
A2	32KHZ_IN	NC	Do not connect
A3	PDN	Input signal	Power down, active-low
A4	VDD1V8	Power	1.7 V-1.9 V (typ. 1.8 V) power supply connection
A5	VDD1V8	Power	1.7 V-1.9 V (typ. 1.8 V) power supply connection
A6	VDD2V2	Power	2.1 V- 2.3 V (typ. 2.2 V) power supply connection
A7	RF_SW1	Input signal	RF Switch Pin 1 – logical voltage level to activate on-board antenna or RF Pad ⇨ RF-Switch Pins Function
A8	GND	Ground pin	Connect to ground
A9	RF_OUT	RF port	50 Ω bottom pad to be activated by RF_SW1/RF_SW2 control voltage ⇨ RF-Switch Pins Function
B1 [1]	PCM_CLK	Input/output	PCM clock signal, output if PCM master, input if PCM slave
	IO6	Digital I/O	General Purpose IO – GPIO[6]

[1] Multi-purpose pins: After the firmware download, the pins (GPIO, Serial Interface, RF control) are programmed in functional mode with dedicated functionality.

No	Pin Name	Pin Type	Description
B2 [1]	PCM_DIN	Input signal	PCM data input signal
	IO4	Digital I/O	General Purpose IO – GPIO[4]
B3 [1]	PCM_SYNC [2]	Input/output	PCM Sync Pulse signal, output if PCM master, input if PCM slave
	IO7 [3]	Digital I/O	General Purpose IO – GPIO[7]
B4	32KHZ_EN	Input Signal	If using VIO 3.3V disable the internal 32.768 kHz crystal oscillator (100 Ω to GND) to use the SoC reference clock with lower accuracy
B5	VDD2V2	Power	2.1 V-2.3 V (typ. 2.2 V) power supply connection
B6	VDD2V2	Power	2.1 V-2.3 V (typ. 2.2 V) power supply connection
B7	RF_SW2	Input signal	RF Switch Pin 2 – logical voltage level to activate on-board antenna or RF Pad ⇨ RF-Switch Pins Function
B8	GND	Ground pin	Connect to ground
B9	GND	Ground pin	Connect to ground
C1	IO2	Digital I/O	General Purpose IO – GPIO[2]
	DVSC[0]	Output signal	Digital voltage scaling control for PMIC (VOUT 2.2V) ⇨ Power Configuration Example with 3.3 V Host Operation
C2	IO3	Digital I/O	General Purpose IO – GPIO[3]
	DVSC[1]	Output signal	Digital voltage scaling control for PMIC (VOUT 1.05V) - not used
C3	IO1	Digital I/O	General Purpose IO – GPIO[1]
C4	COEX_SIN	Input signal	Serial data input from MWS modem or peripheral device
C9	GND	Ground pin	Connect to ground
D1	IO15	Digital I/O	General Purpose IO – GPIO[15]
D2	IO14	Digital I/O	General Purpose IO – GPIO[14]
D3	DNC_E3	NC	Do not connect
D4	COEX_SOUT	Output signal	Serial data output to MWS modem or peripheral device
D9	GND	Ground pin	Connect to ground
E1	SD_CLK	Digital I/O	For SDIO specific terminals ⇨ SDIO Pins Function
E2	SD_CMD	Digital I/O	For SDIO specific terminals ⇨ SDIO Pins Function
E3	IO0	Digital I/O	General Purpose IO – GPIO[0]
E4	DNC_E4	NC	Do not connect
E9	GND	Ground pin	Connect to ground
F1	SD_DAT0	Digital I/O	For SDIO specific terminals ⇨ SDIO Pins Function

[2] PCM Mode: After enabling the mode by host command, the pin is used as PCM Audio Interface.

[3] GPIO Mode: After enabling the mode by host command, the pin is used as Multi-Purpose Interface.

No	Pin Name	Pin Type	Description
F2	SD_DAT1	Digital I/O	For SDIO specific terminals ⇨ SDIO Pins Function
F3 [1]	UART_SOUT [4]	Output Signal	Serial data output to peripheral device
	IO8 [3]	Digital I/O	General Purpose IO – GPIO[8]
	BT_FREQ [5]	Input Signal	Information BT using channel which overlaps WLAN channel or not
F4 [1]	UART_SIN [4]	Input signal	Serial data input to peripheral device
	IO9 [3]	Digital I/O	General Purpose IO – GPIO[9]
	BT_STATE [5]	Input signal	Information BT_REQ priority (1- or 2-bit) and direction BT RX/TX
F5 [1]	UART_RTS [4]	Output signal	Request-to-Send output to peripheral device
	IO11 [3]	Digital I/O	General Purpose IO – GPIO[11]
	BT_REQ [5]	Input signal	BT device request access to medium
F6	IO12	Digital I/O	General Purpose IO – GPIO[12]
F7	CNTL1	Output signal	Do not connect
F8	CNTL0	Input signal	Keep open (DNC) if using SDIO interface for BT or connect with 100 kΩ to GND if using UART interface for BT ⇨ Control Pin Function
F9	GND	Ground pin	Connect to ground
G1	SD_DAT2	Digital I/O	For SDIO specific terminals ⇨ SDIO Pins Function
G2	SD_DAT3	Digital I/O	For SDIO specific terminals ⇨ SDIO Pins Function
G3	VIOSD	Power	1.8 V or 3.3 V Digital I/O SDIO power supply
G4	VIO	Power	1.8 V or 3.3 V power supply for General Purpose IO, if using VIO 3.3V disable the internal 32.768 kHz crystal oscillator (Pin No B4)
G5 [1]	UART_CTS [4]	Input signal	Clear-to-send input from peripheral device
	IO10 [3]	Digital I/O	General Purpose IO – GPIO[10]
	BT_GRANT [5]	Output signal	Indicate permission to transmit, low BT can transmit
G6	IO13	Digital I/O	General Purpose IO – GPIO[13]
G7	VIORF	Power	3.0 V – 3.6 V (typ. 3.3 V) power supply connection
G8	DNC	NC	Do not connect
G9	GND	Ground pin	Connect to ground
EP1	EPAD1	Thermal pin	Connect to ground
EP2	EPAD2	Thermal pin	Connect to gorund

[4] UART mode: After the dedicated firmware download, the pin is used as Host Controller Interface (HCI) for Bluetooth.

[5] Bluetooth External Coexistence Mode: After enabling the mode by host command, the pin is used as Bluetooth external Coexistence Interface.

SDIO Pins Function

<table>
<tr><th rowspan="2">No</th><th rowspan="2">Pin Name</th><th rowspan="2">Pin Type</th><th colspan="2">Description</th></tr>
<tr><th>4-Bit Mode</th><th>1-Bit Mode</th></tr>
<tr><td>E1</td><td>SD_CLK</td><td>Digital I/O</td><td>Clock</td><td>Clock</td></tr>
<tr><td>E2</td><td>SD_CMD</td><td>Digital I/O</td><td>Command Line</td><td>Command Line</td></tr>
<tr><td>F1</td><td>SD_DAT0</td><td>Digital I/O</td><td>Data Line bit [0]</td><td>Data Line</td></tr>
<tr><td>F2</td><td>SD_DAT1</td><td>Digital I/O</td><td>Data Line bit [1] or Interrupt (optional)</td><td>Interrupt</td></tr>
<tr><td>G1</td><td>SD_DAT2</td><td>Digital I/O</td><td>Data Line bit [2] or Read Wait (optional)</td><td>Read Wait (optional)</td></tr>
<tr><td>G2</td><td>SD_DAT3</td><td>Digital I/O</td><td>Data Line bit [3]</td><td>Not used</td></tr>
</table>

RF-Switch Pins Function

<table>
<tr><th rowspan="2">No</th><th rowspan="2">Pin Name</th><th rowspan="2">Pin Type</th><th colspan="2">Logical Level for Activation</th></tr>
<tr><th>On-Board Chip Antenna</th><th>RF OUT Pin</th></tr>
<tr><td>A7</td><td>RF_SW1</td><td>Input signal</td><td>3.0 V-3.6 V (typ. 3.3 V)</td><td>GND (0 V)</td></tr>
<tr><td>B7</td><td>RF_SW2</td><td>Input signal</td><td>GND (0 V)</td><td>3.0 V-3.6 V (typ. 3.3 V)</td></tr>
</table>

Control Pin Function

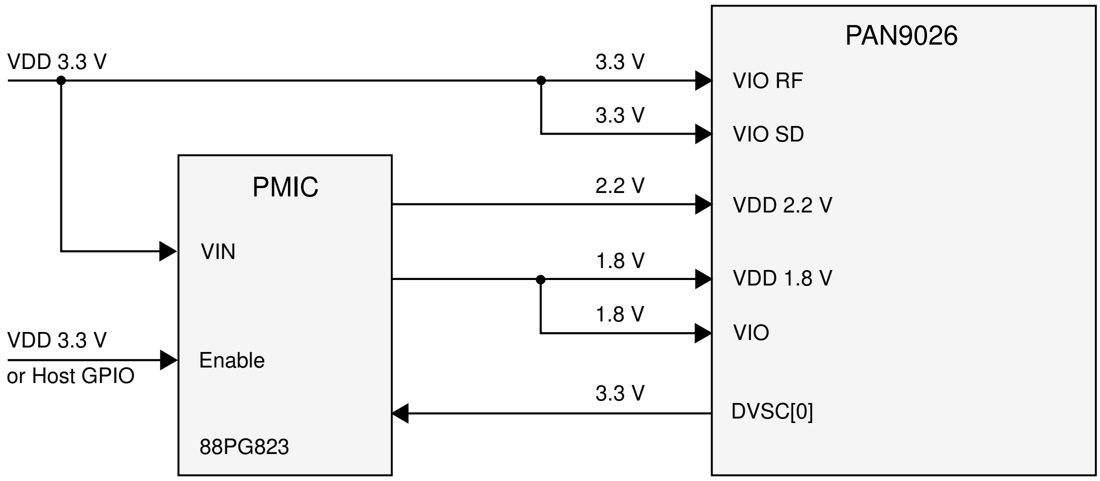
The control pin is used as configuration input to set parameters following a reset. The definition of the pin changes immediately after a reset to its usual function. To set a configuration bit to 0, attach a 100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

<table>
<tr><th rowspan="2">No</th><th rowspan="2">Pin Name</th><th rowspan="2">Pin Type</th><th rowspan="2">Strap Value</th><th rowspan="2">WLAN</th><th rowspan="2">BT/BLE</th><th colspan="2">Firmware Download</th><th rowspan="2">Number SDIO Functions</th></tr>
<tr><th>Type</th><th>Mode</th></tr>
<tr><td rowspan="2">F8</td><td rowspan="2">CNTL0</td><td rowspan="2">Input Signal</td><td>0</td><td>SDIO</td><td>UART</td><td>SDIO+UART</td><td>Parallel/Serial</td><td>1 (WLAN)</td></tr>
<tr><td>1</td><td>SDIO</td><td>SDIO</td><td>SDIO+SDIO</td><td>Parallel/Serial</td><td>2 (WLAN, BT)</td></tr>
</table>

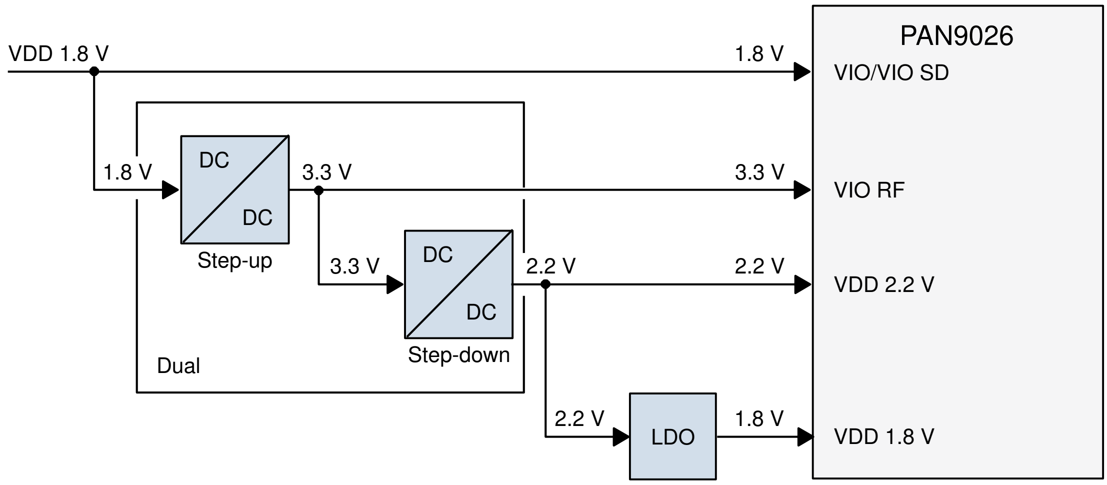
The configuration of the control pin is used for the firmware boot option. The software reads and boots accordingly.

2.3 Power Management

2.3.1 Power Configuration Example with 3.3 V Host Operation



2.3.2 Power Configuration Example with 1.8 V Host Operation



Further information ⇨ 4.3.4 Power-up Sequence.

2.4 Host Interfaces

The bus interface connects several host interface bus units to the CPU bus of the device through the internal bus. The connection of each unit is multiplexed with other bus units.

The high-speed UART interface is connected to the CPU bus through a separate bus.

Type	Features
High-speed UART interface	The device supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant with the industry standard 16550 specification. • FIFO mode permanently selected for transmit and receive operations • Two pins for transmit and receive operations • Two flow control pins • Interrupt triggers for low-power, high throughput operation
SDIO interface	The device supports an SDIO device interface that conforms to the industry standard SDIO full-speed card specification and allows a host controller using the SDIO bus protocol to access the device. • Supports SDIO 3.0 Standard • 1-bit SDIO or 4-bit SDIO transfer modes with full clock range up to 100 MHz • On-chip memory used for CIS • Special interrupt register for information exchange • Allows card to interrupt host

Further information ⇨ 4.3.5 Host Interface

2.5 Peripheral Bus Interface

The Peripheral Bus Unit (PBU) connects several low speed peripherals to the internal bus of the device. The device consists of the GPIO Interface and the One Time Programmable Memory.

Type	Features
General Purpose I/O (GPIO) Interface	• User-defined GPIOs (each configured to either input or output) • Each GPIO controlled independently • Each I/O configurable to output bit from GPIO_OUT
One Time Programmable Memory (OTP)	• Storing device-specific calibration data and hardware information like MAC/BD address, WLAN, and Bluetooth parameter • Programmed during production process of device • Device performs calibration when it is powered up

Further information ⇨ 4.3.6 Peripheral Interface

2.6 PCM Interface

The device supports the PCM interface.

Type	Features
PCM Interface	• Master or slave mode • PCM bit width size of 8 bits or 16 bits • Up to four slots with configurable bit width and start positions • Short frame and long frame synchronization

Further information ⇨ 4.3.7 Audio Interface

2.7 Coexistence

The implemented coexistence framework is based on the IEEE 802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme and the Bluetooth Special Interest Group (BTSIG) Core Specification Volume 7 (Wireless Coexistence Volume).

2.7.1 WLAN/Bluetooth Channel Information Exchange

Since Bluetooth and IEEE 802.11 b/g/n WLAN use the same 2.4 GHz frequency band, each can cause interference with another. The level of interference depends on the respective frequency channel used by Bluetooth and WLAN (other factors can impact interference, like Tx power and Rx sensitivity of the device).

In a system with both Bluetooth and WLAN, the common host receives information about WLAN channel usage and passes the information to the Bluetooth device. For Bluetooth 1.2 devices with Adaptive Frequency Hopping (AFH) enabled, the Bluetooth device can block channel usage that overlaps the WLAN channel in use.

When the Bluetooth device avoids all channels used by the WLAN, the impact of interference is reduced, but not completely eliminated. For Bluetooth 1.1 devices, the Bluetooth device cannot block WLAN channel usage. In this case, a Bluetooth Coexistence Arbiter (BCA) scheme at MAC level is required. The BCA scheme can also be used with Bluetooth 1.2 devices to further reduce the impact of interference to a minimum.

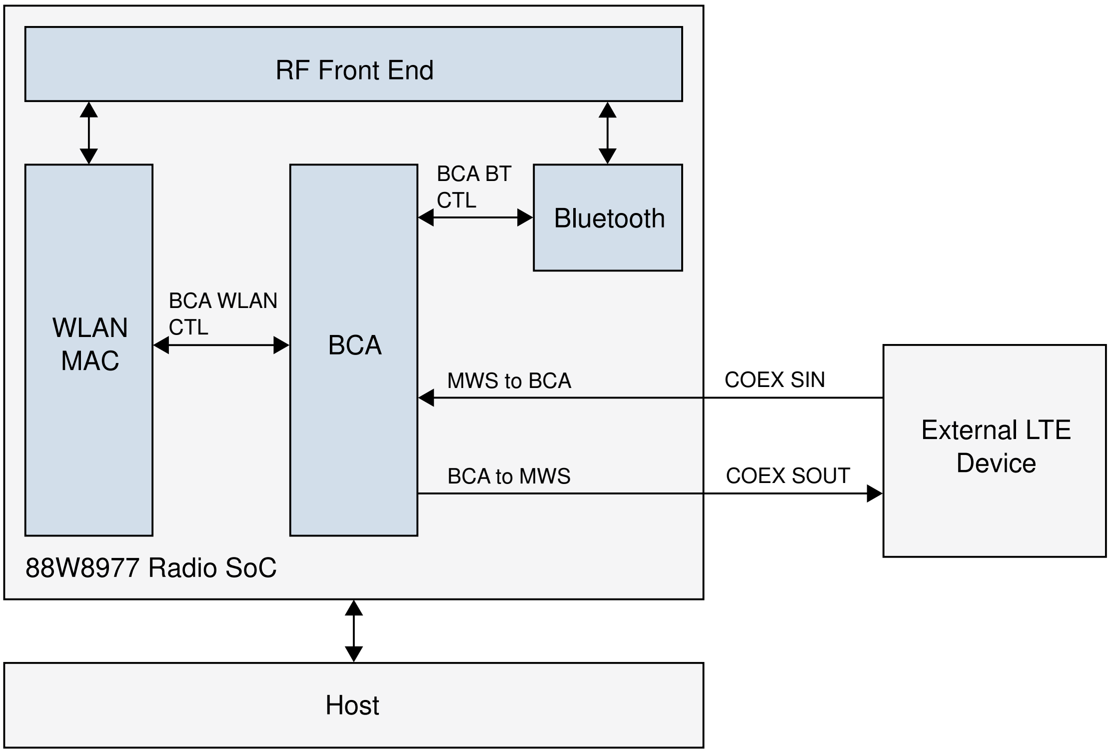
2.7.2 External Mobile Wireless System (LTE/ZigBee) and BCA Exchange

Based on the BTSIG Wireless Coexistence Volume, the device supports a Wireless Coexistence Interface 2 (WCI-2) protocol for WLAN/Bluetooth coexistence with an external Mobile Wireless System (MWS), such as a Long Term Evolution (LTE) or ZigBee device.

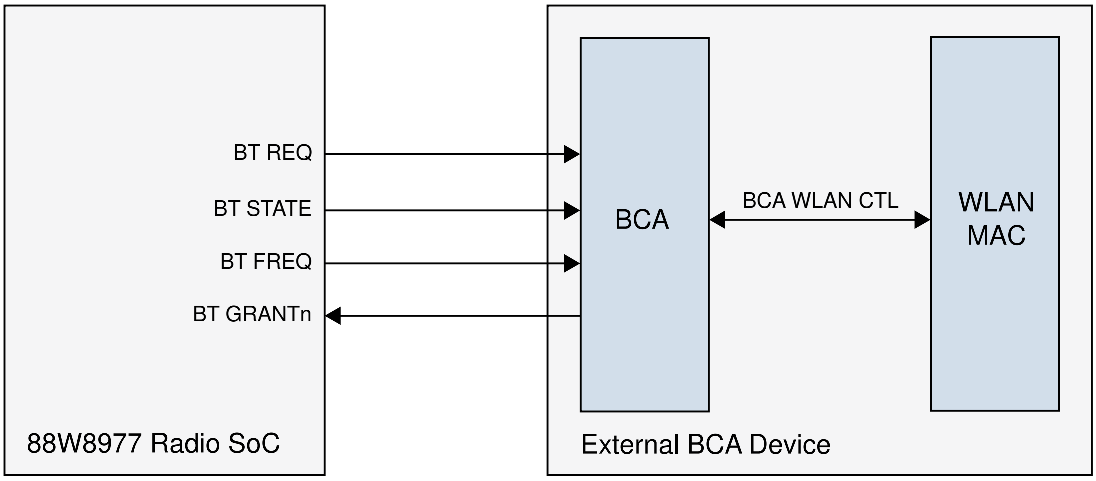
WCI-2 is a 2-wire transport interface. An internal coexistence is used to exchange request/grant with the BCA.

2.7.3 System Configuration

External MWS Device



External BCA Device



2.7.4 WCI-2 Interface

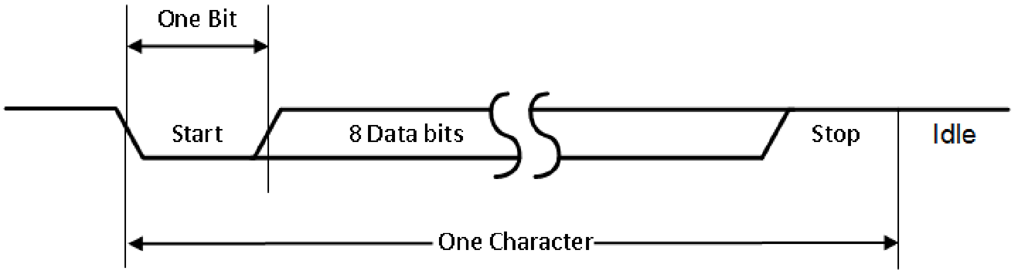
The coexistence interface includes a Mobile Wireless System (MWS) transport controller to accommodate a 2-wire, UART-based serial transport interface. This interface is a standard full-duplex UART (TXD and RXD) carrying logical signals framed as UART characters. In addition, it allows support of multiple logical channels.

Interface Signals

Pin No	Signal Name	Specification Name	Pin Type	Description
C4	COEX_SIN	RXD	Input	Serial data from external MWS device
D4	COEX_SOUT	TXD	Output	Serial data to external MWS device

Signal Waveform Format

The messaging is based on a standard UART format. The UART signals should be connected like a null-modem. For example, the local TXD connected to the remote RXD and vice versa.



Interface Transport Settings

Item	Range	Comment
Baudrate	921 600 ~ 4 000 000	Baud
Data Bits	8	LSB first
Parity Bits	0	No parity
Stop Bit	1	One stop bit
Flow Control	No	No flow control

Supported Baud Rates

Baud			
921 600	2 000 000	3 000 000	4 000 000

Real-Time Signaling Message

The real-time signaling message is used to transport real-time signals over the 2-wire transport interface.

The real-time signaling message conveys the real-time signals (Bluetooth Core Specification, Volume 7, Part A) in one message. The time reference point for the real-time signaling message is the end of message bit 5 (transition to stop bit).

Defined real-time signaling messages include:

- Coexistence Controller to MWS device
- MWS device to Coexistence Controller

Real-Time Signaling	MSG[0]	MSG[1]	MSG[2]	MSG[3]	MSG[4]
MWS to Coexistence Controller (Signal)	FRAME_SYNC	MWS_RX	MWS_TX	PATTERN[0]	PATTERN[1]
Coexistence Controller to MWS (Message)	BT_RX_PRI	BT_TX_ON	802_RX_PRI	802_TX_ON	RFU

Signal Name
FRAME_SYNC
MWS_RX
MWS_TX
PATTERN[1,0]
BT_RX_PRI
BT_TX_ON
802_RX_PRI
802_TX_ON
MWS_INACTIVITY_DURATION
MWS_SCAN_FREQUENCY_OFFSET

Transport Control Message

The transport control messages can modify the state and request state information of the MWS coexistence interface.

Message	MSG[0]	MSG[1]	MSG[2]	MSG[3]	MSG[4]
Transport Control Message	RESEND_REAL_TIME	RFU	RFU	RFU	RFU

Signal Name	Description
RESEND_REAL_TIME	This bit is set if a device wants to get a status update of the real-time signals. The signal is usually used after wake-up from sleep of the transport interface to get an update of the real-time signals. If the receiving device's transport interface is awake it shall send a real-time message with the current status of the real-time signals within 4 UART character period. If the signal is not transmitted within 4 UART character periods, the device is considered asleep. If the receiving device's transport interface is not awake it shall not send a real-time message. Bluetooth initiated: If the MWS is currently scanning or has an ongoing inactivity duration, the MWS shall send a frequency scan message or an inactivity duration message after transmitting the real-time message. If the receiving device's transport interface is not awake it shall not send a frequency scan or inactivity duration message.

Transparent Data Message

The transport control messages can modify the state and request state information of the MWS coexistence interface.

Message	MSG[0]	MSG[1]	MSG[2]	MSG[3]	MSG[4]
Transparent Data Message	NIBBLE_POSITION	DATA[0]/[4]	DATA[1]/[5]	DATA[2]/[6]	DATA[3]/[7]

Signal Name	Description
NIBBLE_POSITION	0 = least significant nibble 1 = most significant nibble
DATA[n]; n=0 .. 7	Data bits of the message octet

MWS Inactivity Duration Message

The inactivity duration messages is used to send the MWS_INACTIVITY_DURATION signal from the MWS device to the Coexistence Controller.

Message	MSG[0]	MSG[1]	MSG[2]	MSG[3]	MSG[4]
MWS Inactivity Duration Message	DURATION[0]	DURATION[1]	DURATION[2]	DURATION[3]	DURATION[4]

The idle duration is encoded in 5 bits given by the formula:

Inactivity_Duration = DURATION * 5 ms

Inactivity durarations smaller than 5 ms are not communicated.

If all bits are set to 1 the inactivity duration is infinite. If all bits are set to 0 or MWS_RX or MWS_TX are set to 1, the inactivity period ends.

MWS Scan Frequency Offset Message

The MWS scan frequency offset message is used to send the MWS_SCAN_FREQUENCY_ OFFSET signal from the MWS device to the Coexistence Controller.

Message	MSG[0]	MSG[1]	MSG[2]	MSG[3]	MSG[4]
MWS Scan Frequency Offset	BAND	FREQ[0]	FREQ [1]	FREQ [2]	FREQ [3]

The RF scan frequency is encoded in 5 bits given by the formula:

RF_FREQ_OFFSET = FREQ * 10 MHz

If BAND is set to o the RF_FREQ_OFFSET is the negative value from the lower edge of the ISM band and if BAND is set to 1, RF_FREQ_OFFSET is the positive value from the top edge of the ISM band.

FREQ set to all 0 indicates the end of the scan period.

2.7.5 Bluetooth Coexistence Arbiter

Type	Features
Capability	• Programmable coexistence interface timing, interface modes, and signal polarity to support a variety of external Bluetooth devices • Programmable decision policies and transaction lock behavior for various use cases • Interface with external or on-chip Bluetooth device • Support Bluetooth 1.1 or Bluetooth 1.2 AFH • WLAN-/Bluetooth-coordinated low-power design • Enhanced information sharing between WLAN and Bluetooth for combo systems • WLAN/Bluetooth/MWS (LTE/ZigBee) coexistence support
Arbitration	• Contention resolved by a customizable decision matrix that allows independent grant decision for each device • Vectors for the decision matrix: – WLAN priority (2-bit) – WLAN direction – Bluetooth priority (1- or 2-bit) – Bluetooth direction – Bluetooth frequency in/out band – MWS priority (2-bit) – MWS direction
AFH	If AFH is enabled in the Bluetooth device, and there is a sufficient guard-band outside the WLAN operating frequency, the Bluetooth device uses the Out-Of-Band (OOB) channel with respect to the WLAN device. Otherwise, the Bluetooth device uses the In-Band (IB) and OOB channels with respect to the WLAN device. The IB and OOB information is either provided by the Bluetooth device through the coexistence interface, or it can be provided through firmware controls in a shared-host system. IB/OOB is a vector in the decision matrix.

Type	Features
Decision Policies	System configuration is a major consideration when planning decision policies. The configuration governs how RF paths are shared and how much interference will occur. Interference combinations include: – WLAN TX and Bluetooth TX – WLAN TX and Bluetooth RX – WLAN RX and Bluetooth TX – WLAN RX and Bluetooth RX Interference combinations where WLAN and Bluetooth share the same antenna: – WLAN TX and Bluetooth TX share same antenna, the decision matrix allows either WLAN or Bluetooth TX (both OOB and IB), based on relative packet priorities. – WLAN TX and Bluetooth RX (both OOB and IB) have sizable interference impacts on Bluetooth RX, the decision matrix grants or denies WLAN TX based on relative packet priorities. – WLAN RX and Bluetooth TX (both OOB and IB) have sizable interference impacts on WLAN RX, the decision matrix grants or denies Bluetooth TX based on relative packet priorities. – WLAN RX and Bluetooth RX (both OOB and IB) have no impact on each other, the decision matrix grants both. Interference combinations where WLAN and Bluetooth have their own antenna: – WLAN TX and Bluetooth TX in OOB situation have little interference impact on each other, the decision matrix grants both. – WLAN TX and Bluetooth TX in IB have sizable interference impact on each other, the decision matrix allows either WLAN or Bluetooth TX, based on relative packet priorities. – WLAN TX and Bluetooth RX in OOB situation have little interference impact on each other, the decision matrix grants both provided there is enough antenna isolation between WLAN and Bluetooth antenna. – WLAN TX and Bluetooth RX in IB situation have sizable interference impact on Bluetooth RX, the decision matrix grants or denies WLAN TX based on relative packet priorities. – WLAN RX and Bluetooth TX in OOB situation have little interference impact on each other, the decision matrix grants both provided there is enough antenna isolation between WLAN and Bluetooth antenna. – WLAN RX and Bluetooth TX in IB situation have sizable interference impact on WLAN RX, the decision matrix grants or denies Bluetooth TX based on relative packet priorities. – WLAN RX and Bluetooth RX (both OOB and IB) have no impact on each other, the decision matrix grants both. For the devices running in a basic shared antenna configuration, the linear switching imposes restrictions on simultaneous transfer. Reasonable policies include: – WLAN and Bluetooth are never granted at the same time – Decision matrix grants a device based on relative packet priorities and direction – Priority order: High > Medium High > Medium > Low – For equal priority contention, select one device to win, that optimizes the usage case For the devices running in an enhanced shared antenna configuration, the linear switching imposes restrictions on some simultaneous transfers.

Type	Features
Transaction Stopping	The arbiter allows control of what transfers can be stopped after an initial grant. If allowed, a transaction can be stopped for higher priority request. A transaction stop decision is a function of the decision policies and transaction stopping control. The transaction stopping control is configurable per device and direction.

2.7.6 Bluetooth Capability

Type	Features
Request Schemes	The PTA signals are directly controlled by the hardware to meet timing requirements of the Bluetooth radio. The software controls the type of traffic in priority mode. Mechanism enforced for control include: • Selection of certain types of communication always treated as high priority • Selection of individual frames marked with high priority • Real-time signaling of the next slot marked with high priority • Automatic hardware control based on the grant/denial history of the Bluetooth link
Timing Control	The PTA signal timing scheme is fully programmable relative to the Bluetooth packet timing.