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Panasonic

PAN9420

Fully Embedded Stand-Alone Wi-Fi Module

Product Specification

Rev. 1.2

Wireless Modules

Overview

The PAN9420 is a 2.4 GHz ISM band Wi-Fi-embedded module which includes a wireless radio and an MCU for easy integration of Wi-Fi connectivity into various electronic devices.

Features

- Fully embedded: integrated full-featured network stack
- Contains all necessary IoT functionality (Place & Play)
- Integrated webserver with AJAX/JSON for web applications
- No stack or software implementation needed on a host MCU
- Simultaneous support of Access-Point- & Infrastructure mode
- Fully automatical IP configuration
- DHCP server offers IP configuration in AP mode
- Access by names (http://yourdevice)
- Integrated TCP/IP network stack: IPv4, ARP, and AutoIP
- Supports TLS/SSL, https, and Wi-Fi security (WPA2) for secure data connection
- Over-the-Air firmware update
- Two UART interfaces (command and transparent data)
- Integrated QSPI flash memory for customer web contents and configuration file
- Programming via standard JTAG
- Evaluation kit with pre-installed web application for quick prototyping available
- Evaluation and development tool WiFigurator for Windows
- Getting started tutorials, PC tool, quickstart guide
- Wide temperature range of -40 °C to +85 °C

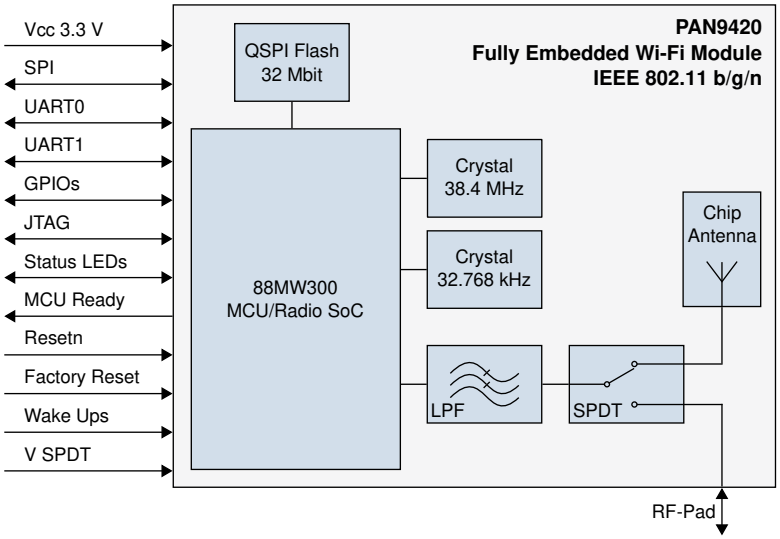
Characteristics

- Surface Mount Type (SMT)
  29.0 mm x 13.5 mm x 2.66 mm
- Marvell® 88MW300 MCU/WLAN System-on-Chip (SoC) inside
- Tx power up to +16 dBm @ IEEE 802.11b
- Rx sensitivity of -97 dBm @ IEEE 802.11b DSSS 1 Mbps
- 20 MHz channels up to 72 Mbps
- Power supply 3.0 to 3.6 V
- Current consumption 150 mA (mix mode Tx/Rx @ 11b, 11 Mbps), 75 mA Rx, 310 mA Tx peak
- Power down mode < 1 mA power consumption
- Low power mode available

Delta PAN9420 vs PAN9320

- PAN9320 replaceable by PAN9420 without changes on mother PCB
- Reduced power consumption in transmit, idle, and power down
- Enhanced temperature range of -40 °C to +85 °C

Block Diagram



By purchase of any of the products described in this document the customer accepts the document's validity and declares their agreement and understanding of its contents and recommendations. Panasonic reserves the right to make changes as required at any time without notification. Please consult the most recently issued Product Specification before initiating or completing a design.

This Product Specification does not lodge the claim to be complete and free of mistakes.

Engineering Samples (ES)

If Engineering Samples are delivered to the customer, these samples have the status “Engineering Samples”. This means that the design of this product is not yet concluded. Engineering Samples may be partially or fully functional, and they may differ from the published Product Specification.

Engineering Samples are not qualified and they are not to be used for reliability testing or series production.

Disclaimer

The customer acknowledges that samples may deviate from the Product Specification and may bear defects due to their status of development and the lack of qualification mentioned above.

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Deviation or lapse in function of the Engineering Sample,

Improper use of the Engineering Sample.

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Table of Contents

1 About This Document

1.1 Purpose and Audience

This Product Specification provides details on the functional, operational, and electrical characteristics of the Panasonic PAN9420 module. It is intended for hardware design, application, and Original Equipment Manufacturers (OEM) engineers. The product is referred to as “the PAN9420” or “the module” within this document.

1.2 Revision History

Revision	Date	Modifications/Remarks
0.1	01.02.2017	1st preliminary version
0.2	31.05.2017	Improved layout
1.0	02.06.2017	Technical data corrected
1.1	19.06.2017	FCC/IC/RED information added
1.2	29.09.2017	Add technical data

1.3 Use of Symbols

Symbol	Description
	**Note** Indicates important information for the proper use of the product. Non-observance can lead to errors.
	**Attention** Indicates important notes that, if not observed, can put the product’s functionality at risk.
⇨ [chapter number] [chapter title]	**Cross reference** Indicates cross references within the document. **Example:** Description of the symbols used in this document ⇨ 1.3 Use of Symbols.

1.4 Related Documents

Please refer to the Panasonic website for related documents ⇨ 7.2.2 Product Information.

2 Overview

The PAN9420 is a 2.4 GHz 802.11 b/g/n embedded Wi-Fi module with integrated stack and API that minimizes firmware development and includes a full security suite. The module is specifically designed for highly integrated and cost-effective applications. The module includes a fully shielded case, integrated crystal oscillators, and a chip antenna.

The module combines a high-performance CPU, high-sensitivity wireless radio, baseband processor, medium access controller, encryption unit, boot ROM with patching capability, internal SRAM, and in-system programmable flash memory. The module's integrated memory is available to the application for storing web content such as HTML pages or image data.

Parallel support of access point and infrastructure mode allows easy setup of simultaneous Wi-Fi connections from the module to smart devices and home network routers.

The pre-programmed Wi-Fi SoC firmware enables client (STA), micro access point (uAP), and Ad-hoc mode (Wi-Fi Direct) applications. With the transparent mode, raw data can be sent from the UART to the air interface to smart devices, web servers, or PC applications.

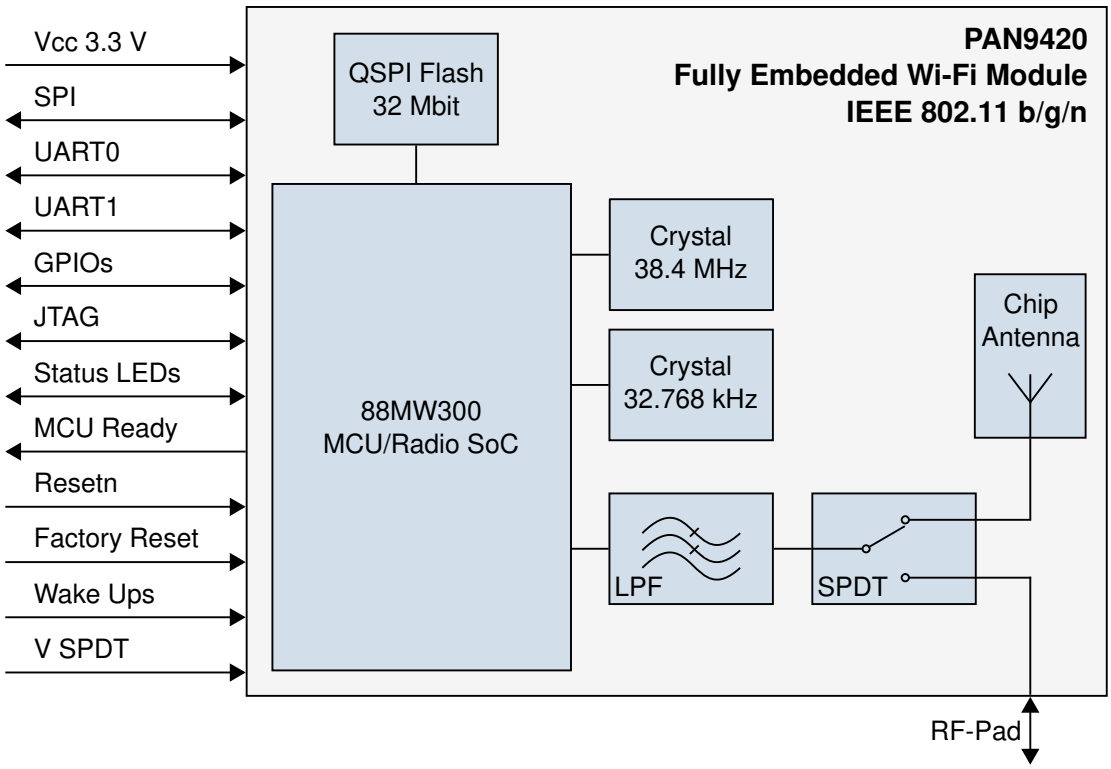
The PAN9420 supports Over-the-Air firmware updates. In order to make use of this feature, the customer needs to ensure that the appropriate preconditions are fulfilled and that a suitable environment is provided, particularly with regard to:

- Module configuration
- Utilization of the related module interface commands
- Server infrastructure and application

Please refer to the Panasonic website for related documents ⇨ 7.2.2 Product Information.

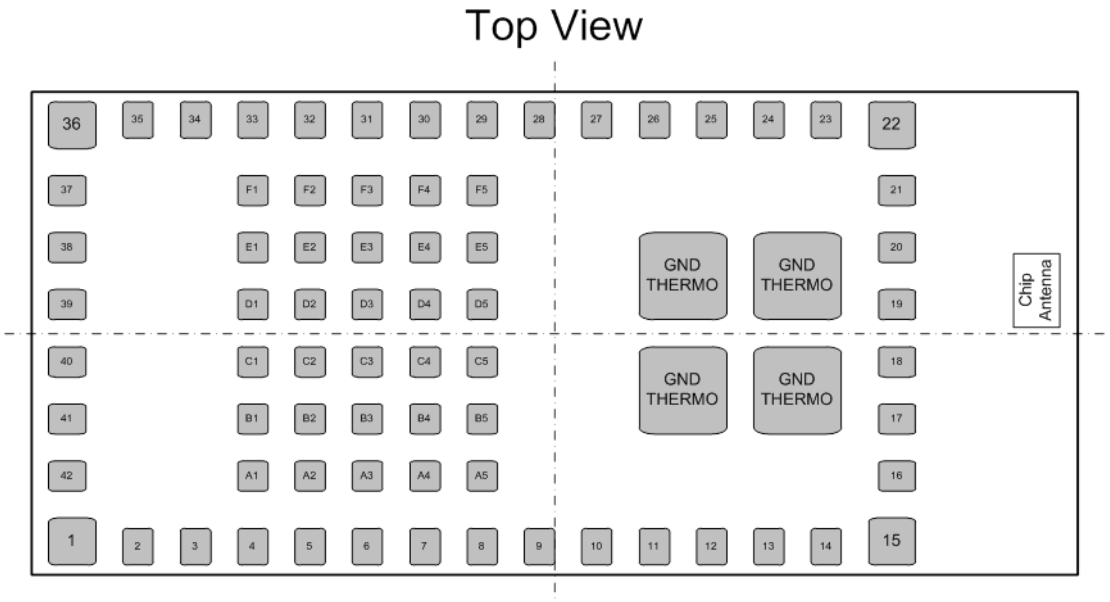
Further information on the variants and versions ⇨ 7.1 Ordering Information.

2.1 Block Diagram



2.2 Pin Configuration

Pin Assignment



Pin Functions

No	Pin Name	Pin Type	Description
1	GND	Ground Pin	Connect to ground
2	GPIO4[1]	Digital I/O	Digital I/O #4
3	GPIO5[1]	Digital I/O	Digital I/O #5
4	NC	NC	Do not connect
5	NC	NC	Do not connect
6	NC	NC	Do not connect
7	3.3 V	Power	3.0 V-3.6 V power supply connection (typical 3.3 V)
8	3.3 V	Power	3.0 V-3.6 V power supply connection (typical 3.3 V)
9	UART1 CTS	Digital In	CTSn for UART1 (using hardware flow control)
10	UART1 RTS	Digital Out	RTSn for UART1 (using hardware flow control)
11	UART1 TXD	Digital Out	TXD for UART1
12	UART1 RXD	Digital In	RXD for UART1
13	NC	NC	Do not connect
14	GND	Ground Pin	Connect to ground
15	GND	Ground Pin	Connect to ground

[1] All GPIOs are initially set to output with low level

No	Pin Name	Pin Type	Description
16	NC/RF	NC/Analog IO	RF in/out over 50Ω bottom pad
17	GND	Ground Pin	Connect to ground
18	GND	Ground Pin	Connect to ground
19	GND	Ground Pin	Connect to ground
20	GND	Ground Pin	Connect to ground
21	GND	Ground Pin	Connect to ground
22	GND	Ground Pin	Connect to ground
23	GND	Ground Pin	Connect to ground
24	GND	Ground Pin	Connect to ground
25	GND	Ground Pin	Connect to ground
26	W STAT LED	Digital Out	Connect to LED wireless (Wi-Fi) status, active low
27	UART0 TXD/DUAL STAT	Digital Out	TXD for UART0/UART1 state (binary data or command)
28	UART0 RXD/DUAL SW	Digital In	RXD for UART0/UART1 toggle switch for the control of the state
29	GPIO49[1]	Digital I/O	Digital I/O #49
30	GPIO48[1]	Digital I/O	Digital I/O #48
31	GPIO47[1]	Digital I/O	Digital I/O #47
32	GPIO46[1]	Digital I/O	Digital I/O #46
33	STAT LED1	Digital Out	Connect to LED MCU status (heartbeat), active low
34	STAT LED2	Digital Out	Connect to LED IP connectivity (allocated IP), active low
35	STAT LED3	Digital Out	Connect to LED Error (active during booting), active low
36	GND	Ground Pin	Connect to ground
37	RESETn	Digital In	Reset MCU, active low
38	WAKE UP0[2]	Digital In	Wake up signal for MCU/WLAN SoC, active high
39	NC	NC	Do not connect
40	NC	NC	Do not connect
41	MCU READY	Digital Out	Connect to LED MCU ready (booting ready), active high
42	FACTORY RESET	Digital In	Factory reset (valid after 10 seconds), active high
A1	NC	NC	Do not connect
A2	NC	NC	Do not connect
A3	NC	NC	Do not connect
A4	SPDT V1	Input Signal	Do not connect if on-board antenna In/Out is desired, for RF-Pad In/Out ⇨ 4.3.2 Module Selectable RF-In/Output.

[2] Connect to HOST MCU (wake up after shut-off mode, active high), use 10 kOhm resistor to GND at pin

No	Pin Name	Pin Type	Description
A5	SPDT V2	Input Signal	Do not connect if on-board antenna In/Out is desired, for RF-Pad In/Out ⇨ 4.3.2 Module Selectable RF-In/Output.
B1	NC	NC	Do not connect
B2	NC	NC	Do not connect
B3	NC	NC	Do not connect
B4	NC	NC	Do not connect
B5	NC	NC	Do not connect
C1	NC	NC	Do not connect
C2	NC	NC	Do not connect
C3	WAKE UP1[2]	Digital In	Wake up signal for MCU/WLAN SoC, active high
C4	NC	NC	Do not connect
C5	NC	NC	Do not connect
D1	TDI	Digital In	TDI for JTAG (option for flashing in production process)
D2	TRSTn	Digital In	TRSTn for JTAG (option for flashing in production process)
D3	NC	NC	Do not connect
D4	NC	NC	Do not connect
D5	NC	NC	Do not connect
E1	TDO	Digital Out	TDO for JTAG (option for flashing in production process)
E2	TCK	Digital Out	TCK for JTAG (option for flashing in production process)
E3	TMS	Digital I/O	TMS for JTAG (option for flashing in production process)
E4	NC	NC	Do not connect
E5	NC	NC	Do not connect
F1	NC	NC	Do not connect
F2	NC	NC	Do not connect
F3	GND	Ground Pin	Connect to ground
F4	GND	Ground Pin	Connect to ground
F5	GND	Ground Pin	Connect to ground
GND THERMO		Thermal Pin	Connect to ground
GND THERMO		Thermal Pin	Connect to ground
GND THERMO		Thermal Pin	Connect to ground
GND THERMO		Thermal Pin	Connect to ground

2.3 Host Interfaces

UART0 Interface

- 2-wire data transfer (RX, TX)
- Programmable baud rate (300 bps to 1.5 Mbps)
- Data format (LSB first)
- Data bit: (5-8 bit)
- Parity bit: (0-3 bit)
- Stop bit: (1-2 bit)

UART1 Interface

- 4-wire data transfer (RX, TX, RTS, CTS)
- Programmable baud rate (300 bps to 1.5 Mbps)
- Data format (LSB first)
- Data bit: (5-8 bit)
- Parity bit: (0-3 bit)
- Stop bit: (1-2 bit)

Further information ⇨ 4.3.7 Host Interface Specification.

2.4 Peripheral Bus Interface

Embedded MCU and WLAN Radio (SoC)

Features	Characteristics
JTAG	• Standard JTAG interface
General Purpose I/O (GPIO) Interface	• Defined GPIOs, I/O configured to either input or output (on/off) • GPIOs with LED status functionality (ready, heartbeat, IP-connectivity, error and WLAN connectivity)
Wake Up 0 / 1	• External signal for wake-up after shut-off mode

Further information ⇨ 4.3.8 Peripheral Interface Specification.

2.5 WLAN Features

Type	Features
IEEE 802.11/Standards	• 802.11 data rates 1 and 2 Mbps (DSSS) • 802.11b data rates 5.5 and 11 Mbps (CCK) • 802.11g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbps (OFDM) • 802.11b/g performance enhancements • 802.11n-compliant with maximum data rates up to 72 Mbps (20 MHz channel) • 802.11d international roaming[3] • 802.11i enhanced security • 802.11k radio resource measurement[3] • 802.11r fast hand-off for AP roaming[3] • 802.11w protected management frames[3] • Support clients (stations) implementing IEEE Power Save mode • Wi-Fi direct connectivity[3]
WLAN MAC	• Simultaneous peer-to-peer and Infrastructure Modes • RTS/CTS for operation and DCF • Hardware filtering of 32 multicast addresses • On-chip Tx and Rx FIFO for maximum throughput • Open System and Shared Key Authentication services • A-MPDU RX (de-aggregation) and TX (aggregation) • Reduced Inter-Frame Spacing (RIFS) bursting • Management information base counters • Radio resource measurement counters • Quality of service queues • Block acknowledgement extensions • Multiple-BSSID and Multiple-Station operation • Transmit rate adaptation • Transmit power control • Long and short preamble generation on a frame-by-frame basis for 802.11b frames • Marvell® Mobile Hotspot

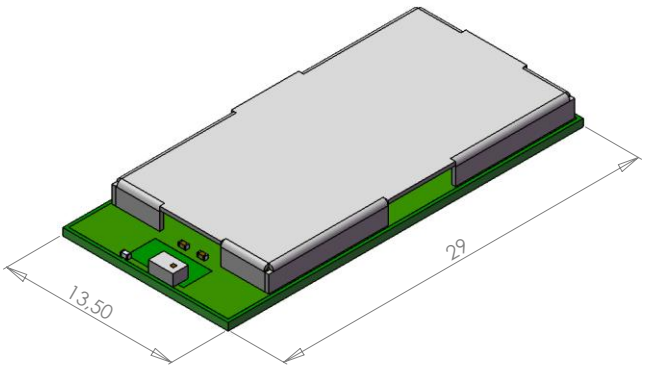
[3] Hardware-supported, not implemented in the pre-installed firmware stack

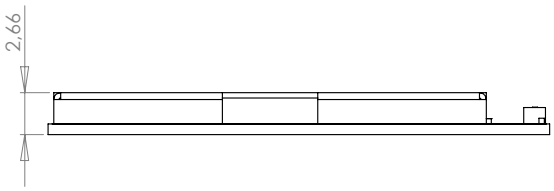
Type	Features
WLAN Baseband	• 802.11n 1x1 SISO (WLAN SoC with SISO RF radio) • Backward compatibility with legacy 802.11b/g technology • PHY data rates up to 72.2 Mbps • 20 MHz bandwidth/channel • Modulation and Coding Scheme MCS 0 ~ 7 • Radio resource measurement • Optional 802.11n SISO features: – 1 spatial stream (STBC) reception and transmission – Short guard interval – RIFS on receive path for 802.11n packets – 802.11n greenfield Tx/Rx
WLAN Radio	• Integrated direct-conversion radio • 20 MHz channel bandwidth • Embedded WLAN Radio SoC with the following features: – Direct conversion radio (no need for external SAW filter) – 2.4 GHz TX/RX switch, Power Amplifier (PA) and Low Noise Amplifier (LNA) path – Gain selectable LNAs with optimized noise figure and power consumption – Power Amplifiers with power control – Optimized TX gain distribution for linearity and noise performance – Fine channel step with AFC (adaptive frequency control)
WLAN Encryption	• Embedded WLAN Radio SoC with the following features: – WEP 64-bit and 128-bit encryption with hardware TKIP processing (WPA) – AES-CCMP hardware implementation as part of 802.11i security standard (WPA2) – Enhanced AES engine performance – AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard[3]

3 Detailed Description

3.1 Dimensions

All dimensions are in millimeters.

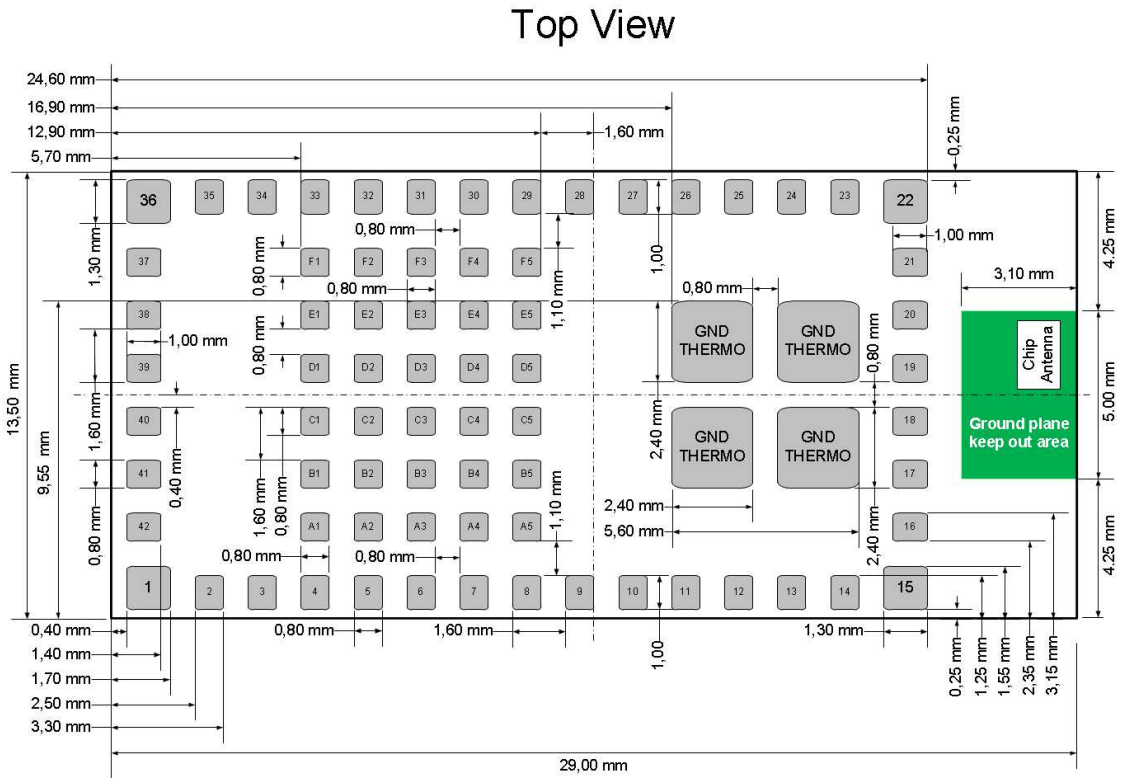




No.	Item	Dimension	Tolerance	Remark
1	Width	13.50	± 0.35	
2	Length	29.00	± 0.35	
3	Height	2.66	± 0.20	with case

3.2 Footprint

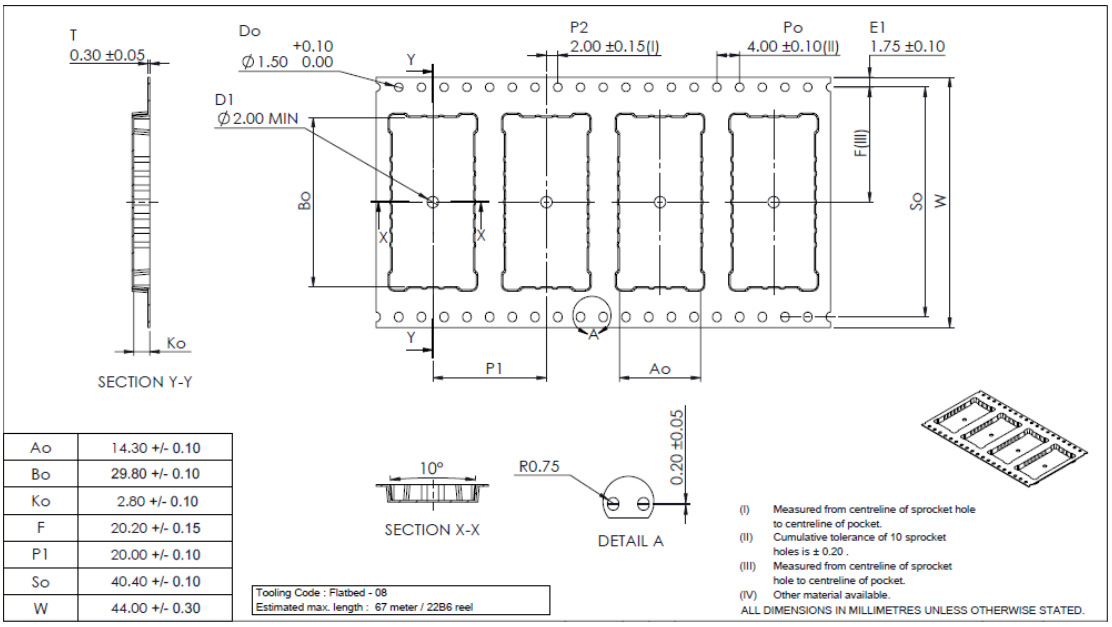
The outer dimensions have a tolerance of ±0.35 mm.



3.3 Packaging

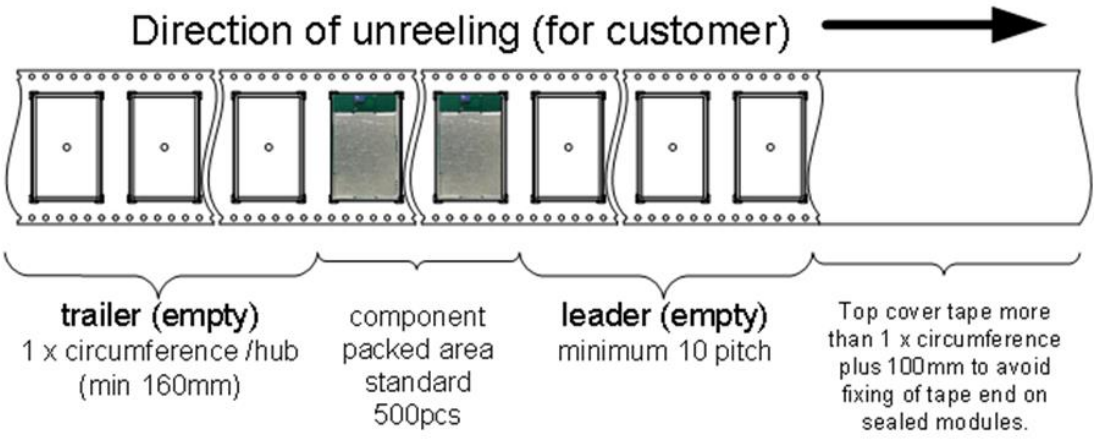
The product is a mass production status product and will be delivered in the package described below.

3.3.1 Tape Dimensions



Ao	14.30 +/- 0.10
Bo	29.80 +/- 0.10
Ko	2.80 +/- 0.10
F	20.20 +/- 0.15
P1	20.00 +/- 0.10
So	40.40 +/- 0.10
W	44.00 +/- 0.30

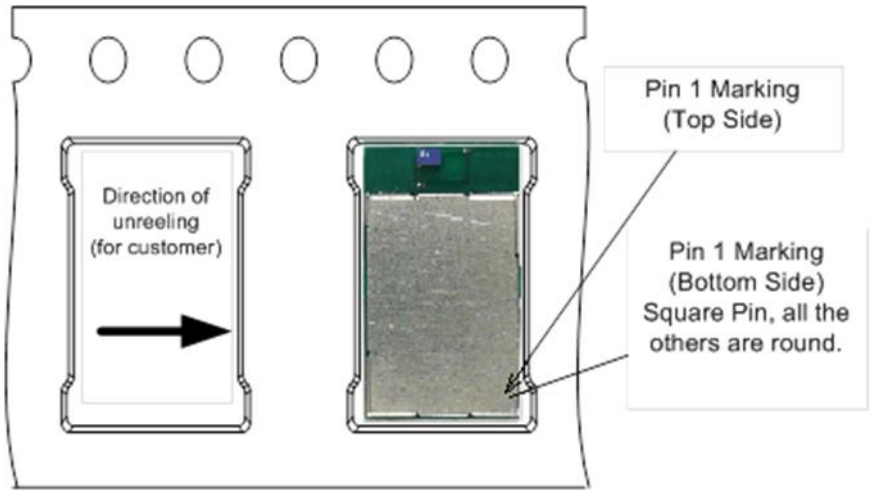
3.3.2 Packing in Tape



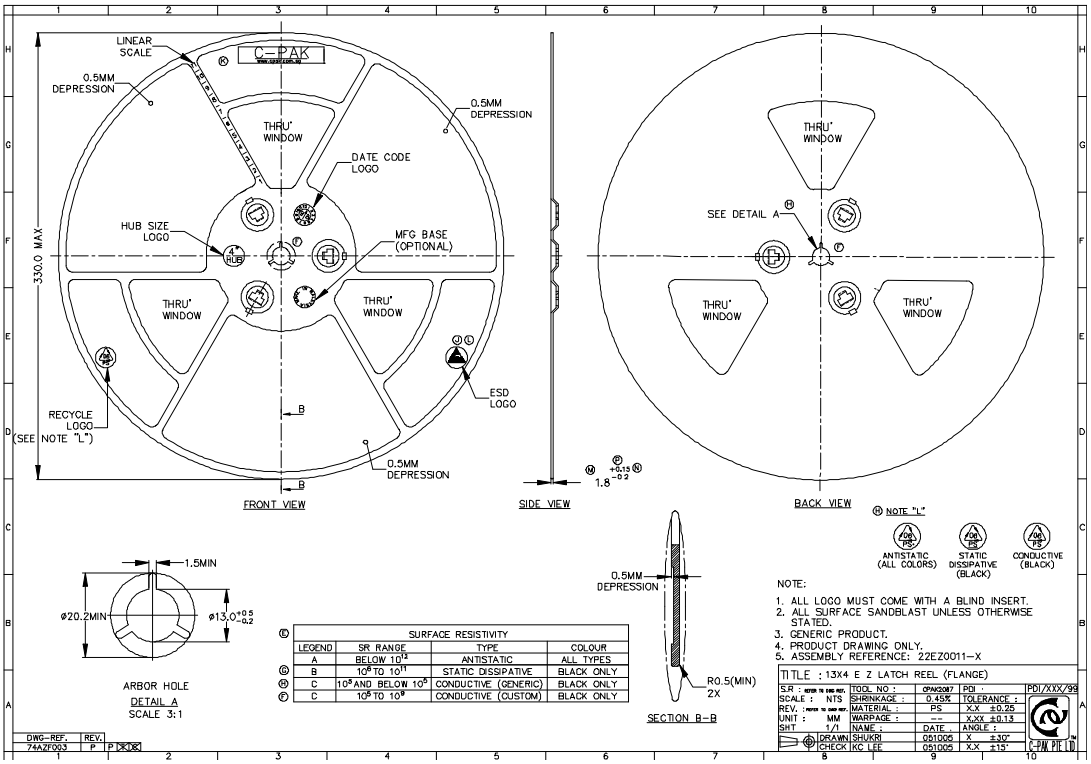
Empty spaces in the component packed area shall be less than two per reel and those spaces shall not be consecutive.

The top cover tape shall not be found on reel holes and it shall not stick out from the reel.

3.3.3 Component Direction

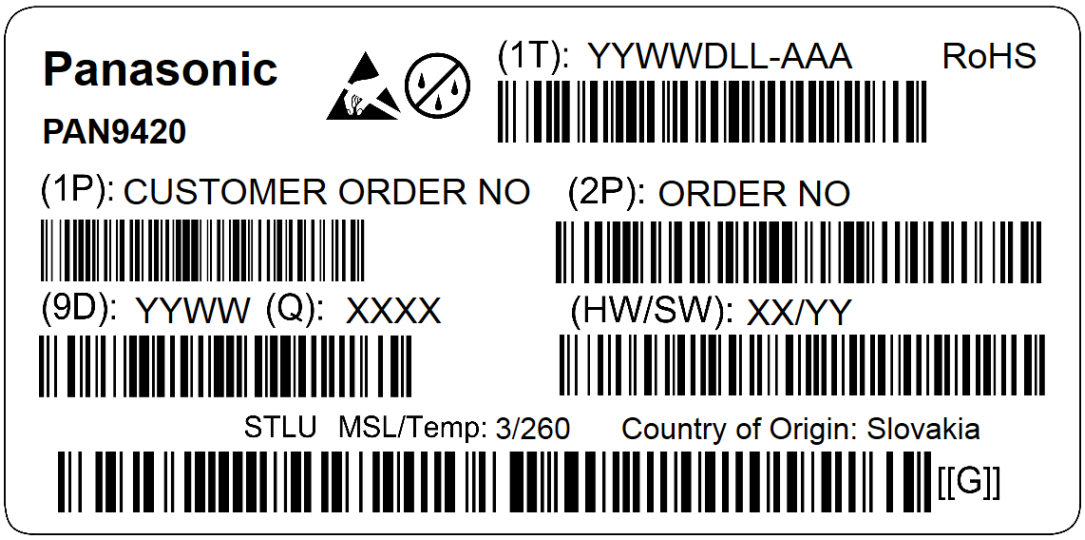


3.3.4 Reel Dimension



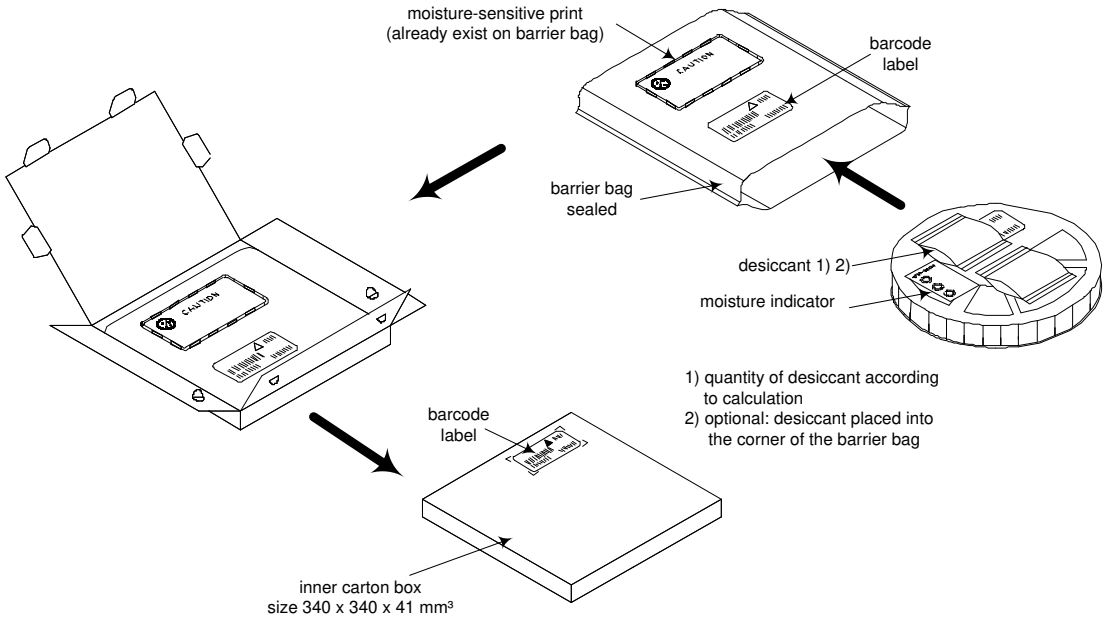
3.3.5 Package Label

Example



(1T)	Lot code
(1P)	Customer order number, if applicable
(2P)	Order number
(9D)	Date code
(Q)	Quantity
(HW/SW)	Hardware/Software version

3.3.6 Total Package



3.4 Case Marking

Example for PAN9420 (FCC version)

1	Brand name
2	Hardware/Software version
3	Engineering Sample (optional)
4	Model Name/ENW number
5	Lot code
6	Serial number
7	WLAN MAC address
8	FCC ID
9	IC Canada
10	Marking for Pin 1
11	2D-barcode, for internal usage only

4 Specification

All specifications are over temperature and process, unless indicated otherwise.

4.1 Default Test Conditions

Temperature:	25 ± 10 °C
Humidity:	40 to 85 % RH
Supply Voltage:	3.3 V

4.2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{STOR}	Storage temperature		-40		+85	°C
V_{ESD}	ESD robustness	All pads, according to human body model (HBM), JEDEC STD 22, method A114			1 000	V
		According to charged device model (CDM), JEDEC STD 22, method C101			500	V
P_{RF}	RF input level				+20	dBm
V_{DDMAX}	Maximum voltage	Maximum power supply voltage from any pin with respect to V_{SS} (GND)	-0.4		3.6	V
V_{DIG}	Voltage on any digital pins	GPIOs, RESETn, UART, QSPI, Coex I/F	-0.4		V_{DDMAX}	V

4.3 Recommended Operating Conditions

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_A	Ambient operating temperature range	Industrial grade	-40		+85	°C
V_{DD}	3V3 Supply voltage[4]	Voltage on pins 7, 8 (3.3 V) I/O supply voltage internally connected to V_{DD}/V_{CC}	3.0	3.3	3.6	V

4.3.1 Digital Pin Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage[5]	3.3 V operation ($V_{IO} = V_{DD}$)	0.7 V_{DD}		V_{DD}+0.3	V
V_{IL}	Low level input voltage[5]	3.3 V operation ($V_{IO} = V_{DD}$)	-0.4		0.3 V_{DD}	V
I_{OH} @ V_{DD}-0.5 V	High level output current[5]	3.3 V operation ($V_{IO} = V_{DD}$)	3			mA
I_{OL} @ 0.4 V	Low level output current[5]	3.3 V operation ($V_{IO} = V_{DD}$)	4			mA

4.3.2 Module Selectable RF-In/Output

Module RF-Output can be switched between on-board ceramic chip antenna and 50 Ohm RF-pad (pin 16) output by adjusting voltage level on pin A4 and A5. If pin A4 and A5 are not connected (NC), output state will be on-board ceramic chip antenna.

RF In/Output	Pin A4	Pin A5
On-board ceramic chip antenna output	NC or 3.0 V – 3.6 V (typ. 3.3V)	NC or GND (0 V)
Module 50 Ohm RF-pad output (pin 16)	GND (0 V)	3.0 V – 3.6 V (typ. 3.3 V)

[4] The supply current must be limited to max. 1A

[5] The capacitive load should not be larger than 50 pF for all I/Os when using the default driver strength settings. Large capacitance loads generally increase the overall current consumption.

4.3.3 Current Consumption

The current consumption depends on the user scenario and on the setup and timing in the power modes.

Assume V_{DD} = 3.3 V, T_{amb} = 25 °C, if nothing else stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{TX}	Active Transmit[6]	P_{TX} = +16 dBm for 802.11b		310		
I_{TX-Rx}	Active Transmit[7] (Tx / Rx mixed mode)	P_{TX} = +16 dBm for 802.11b @ 11 Mbps		170		mA
		P_{TX} = +14 dBm for 802.11g @ 54 Mbps		115		mA
		P_{TX} = +13 dBm for 802.11n (20 MHz) @ 65Mbps		85		mA
I_{RX}	Active Receive[8]	802.11b @ 11 Mbps		75		mA
		802.11g @ 54 Mbps		75		mA
		802.11n @ 65 Mbps		75		mA
I_{RXIdle}	Receive Idle[9]	Passive receive state, ready to receive packets, but no active decoding		75		mA
$I_{Shut-off}$	Shut-off	MCU and Radio in shut-off mode			1	mA

4.3.4 Internal Operating Frequencies

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{SYSCLK1}$	CPU/System/ Encryption clock speed				200	MHz
$f_{REFCLK1}$	WLAN/MCU Crystal fundamental frequency	Frequency tolerance < ±10 ppm over operating temperature and process		38.4		MHz
$f_{REFCLK2}$	Sleep Clock Crystal fundamental frequency	Frequency tolerance < ±10 ppm over operating temperature and process		32.768		kHz

[6] Peak values for specified output power level and data rate with UDP traffic between the AP and Device (STA).

[7] Average values for specified output power level and data rate with UDP traffic between the AP and Device (STA).

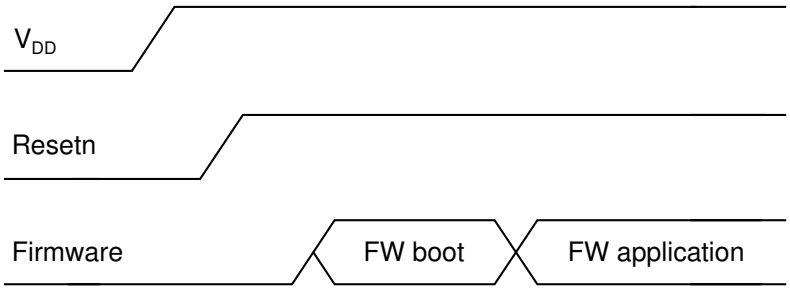
[8] Average values for specified data rate with UDP traffic between the AP and Device (STA).

[9] The device is powered on and is ready to receive packets, but it is not actively decoding.

4.3.5 Power Up Sequence

When the power is turned on, set reset signal to low (RESETn = low).

After the V_{DD} is stable, release the reset (RESETn = high).



4.3.6 Firmware-Related Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{MCU\ READY}$	Time period from Power up or Reset until MCU READY pin is active		4	5	sec
$T_{WAKE\ UP}$	Time period needed to set pin active to wake-up from shut-off mode (afterwards firmware is booting)			100	ms
$T_{FACTORY\ RESET}$	Time period needed to set pin active to release factory reset (afterwards firmware is booting)		8	10	sec
$T_{INFRA\ ASSO}$	Time period in Infrastructure mode from WLAN association request until association with selected Access-Point's SSID		4		sec
$T_{DE\text{-}ASSO\ SCAN}$	Time period between de-association from AP until next scan is released		60		sec
$T_{IP\ DHCP}$	Time period from IP DHCP request until IP assignment			90	sec

4.3.7 Host Interface Specification

4.3.7.1 UART0 Command Interface

Bus Signals

Module Pin No	Signal Name	Function	Description
27	UART0 TXD	Command	Transmit data output
28	UART0 RXD		Receive data input

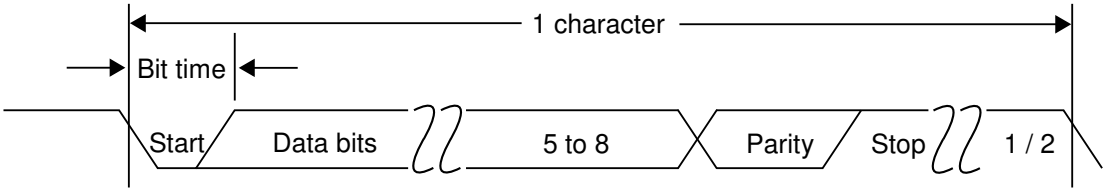
Protocol

Item	Range	Default	Comment
Baud rate	300 ~ 1 500 000	115 200	Baud
Data bits	5 ~ 8 (LSB first)	8	LSB first
Parity bits	0 ~ 3	0	Even, odd, or no parity detection
Stop bit	1/2	1	

Supported Baud Rates

Baud								
300	600	1 200	2 400	4 800	9 600	14 400	19 200	28 800
38 400	56 000	57 600	115 200	128 000	256 000	520 000	780 000	1 500 000

UART0 Timing Diagram



4.3.7.2 UART1 Binary Data Interface

Bus Signals

Module Pin No	Signal Name	Function	Description
9	UART1 CTS	Binary data	Clear to send
10	UART1 RTS		Request to send
11	UART1 TXD		Transmit data output
12	UART1 RXD		Receive data input

Protocol

Item	Range	Default	Comment
Baud rate	300 ~ 1 500 000	115 200	Baud
Data bits	5 ~ 8 (LSB first)	8	LSB first
Parity bits	0 ~ 3	0	Even, odd, or no parity detection
Stop bit	1/2	1	

Supported Baud Rates

Baud								
300	600	1 200	2 400	4 800	9 600	14 400	19 200	28 800
38 400	56 000	57 600	115 200	128 000	256 000	520 000	780 000	1 500 000

UART1 Timing Diagram