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PRODUCT DATA SHEET

PAC5223

Power Application Controller®

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

ARM® Cortex®-M0 Controller Core

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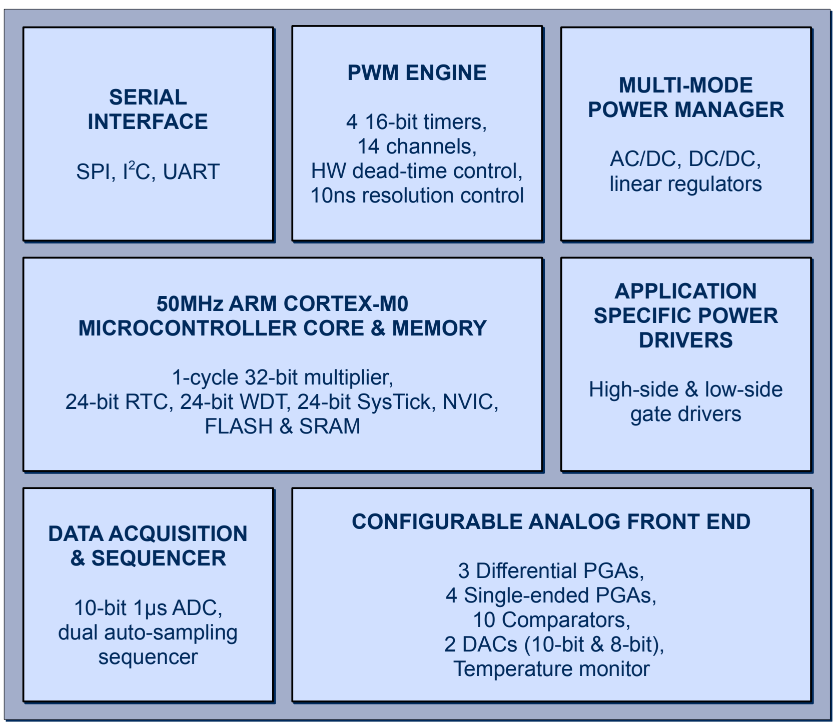
1. GENERAL DESCRIPTION

The PAC5223 belongs to Active-Semi's broad portfolio of full-featured Power Application Controller® (PAC) products that are highly optimized for controlling and powering next generation smart energy appliances, devices, and equipment. These application controllers integrate a 50MHz ARM® Cortex®-M0 32-bit microcontroller core with Active-Semi's proprietary and patent-pending Multi-Mode Power Manager™, Configurable Analog Front End™, and Application Specific Power Drivers™ to form the most compact microcontroller-based power and general purpose application systems ranging from digital power supply to motor control. The PAC5223 microcontroller features up to 32kB of embedded FLASH and 8kB of SRAM memory, a high-speed 10-bit 1μs analog-to-digital converter (ADC) with dual auto-sampling sequencers, 5V/3.3V I/Os, flexible clock sources, timers, a versatile 14-channel PWM engine, and several serial interfaces.

The Multi-Mode Power Manager (MMPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable multi-mode switching supply controller capable of operating in buck, SEPIC or AC/DC Flyback mode, and up to four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are high-voltage power drivers designed for each target set of control applications, including half bridge, H-bridge, 3-phase, intelligent power module (IPM), and general purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals. Together, these modules and microcontroller enable a wide range of compact applications with highly integrated power management, driving, feedback, and control for DC supply up to 70V and for line AC supply.

Figure 1-1. Power Application Controller

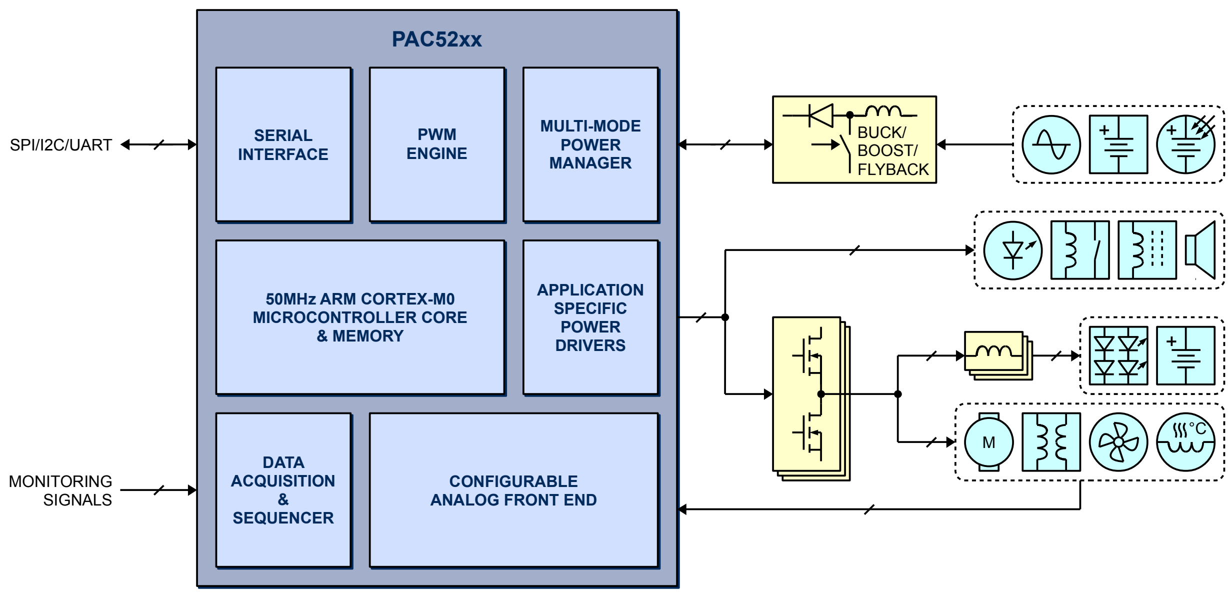


The PAC5223 is available in a 48-pin, 6x6 mm TQFN package. The PAC family includes a range of part numbers optimized to work with different targeted primary applications.

2. PAC FAMILY APPLICATIONS

- General purpose high-voltage system controllers
- Home appliances
- Power tools
- Motor controllers
- LED lighting controllers
- Uninterruptible power supply (UPS)
- Solar micro-inverters
- Wireless power controllers
- Digital power controllers
- Industrial applications

Figure 2-1. Simplified Application Diagram



3. PRODUCT SELECTION SUMMARY

Table 1. Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS			MICROCONTROLLER						PRIMARY APPLICATION
		INPUT VOLTAGE	SWMULTI-MODE	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	POWER DRIVER	PWM CHANNEL	PROTECTFAULT	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	INTERFACE	XTAL	
PAC5223	48-pin 6x6 TQFN	5.2-70V	Y	3	4	10	2	10	3 LS (1A/1A) 3 HS (1A/1A)	6	Int	50	32	8	25	SPI I²C UART SWD	N	3 half bridge, 3-phase control

Notes: DIFF-PGA = differential programmable gain amplifier, GD = gate driver, HS = high-side , LS = low-side, OD = open-drain driver, PGA = programmable gain amplifier, UHV = ultra-high-voltage.

4. ORDERING INFORMATION

Table 2. Ordering Information

PART NUMBER(1)	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5223QM	-40°C to 105°C	TQFN66-48	48 + Exposed Pad	Tray

(1) See *Product Selection Summary* for product features for each part number.

5. ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

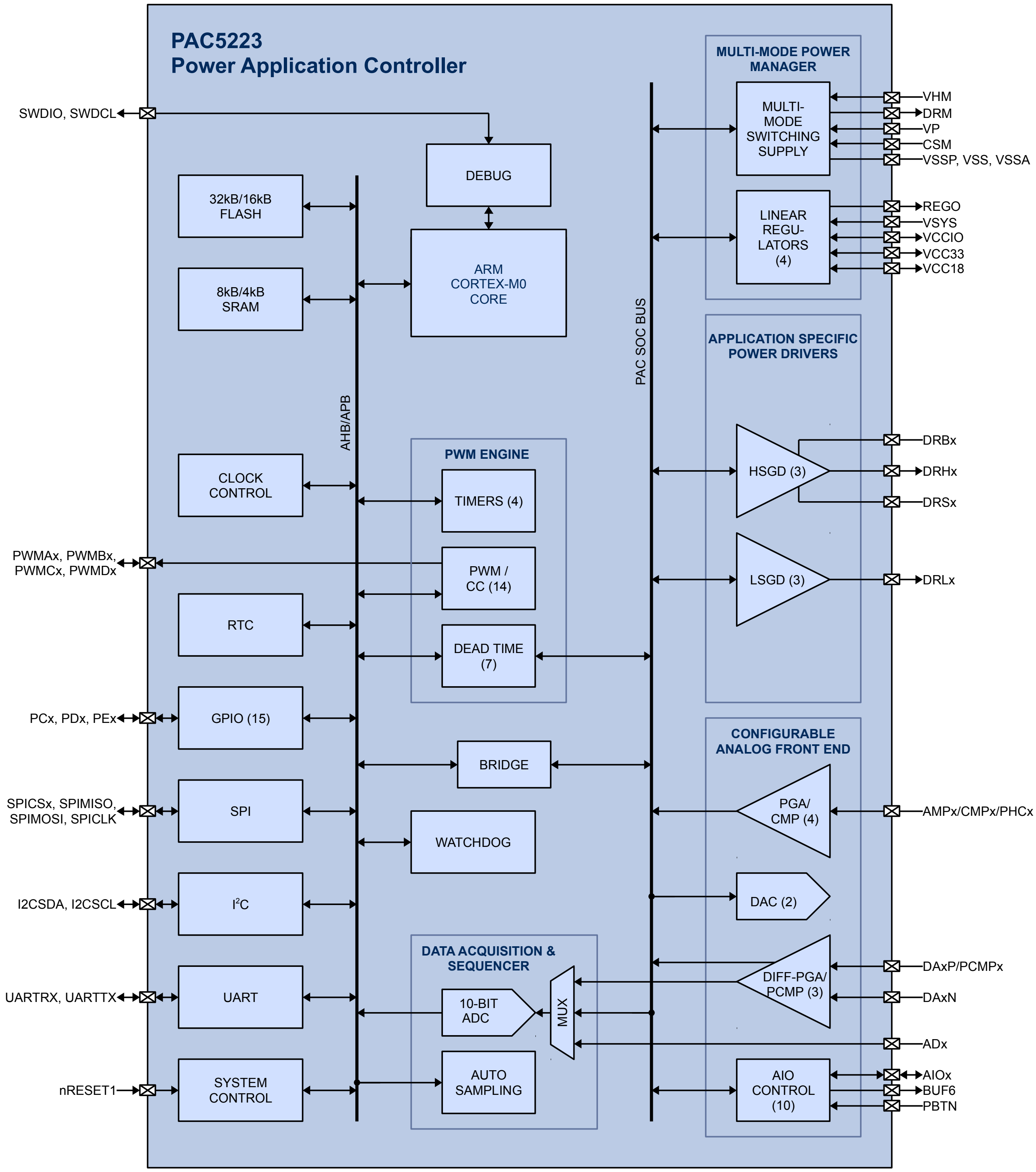
(Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER		VALUE	UNIT
VHM, DRM to VSSP		-0.3 to 72	V
VP to VSS		-0.3 to 20	V
CSM, REGO to VSS		-0.3 to V_P + 0.3	V
VSYS, AIO6/.. to VSS		-0.3 to 6	V
VCC33 to VSS		-0.3 to 4.1	V
VCC18 to VSS		-0.3 to 2.5	V
AIOx/.. (except AIO6/..), VCCIO to VSS		-0.3 to V_{SYS} + 0.3	V
PDx/.., PEx/.. to VSS		-0.3 to V_{CCIO} + 0.3	V
PCx/.. to VSSA		-0.3 to V_{CC33} + 0.3	V
DRLx to VSSP		-0.3 to V_P + 0.3	V
DRBx to VSSP		-0.3 to 84	V
DRSx to VSSP		-6 to 72	V
DRSx allowable offset slew rate (dV_{DRSx}/dt)		5	V/ns
DRBx, DRHx to respective DRSx		-0.3 to 20	V
VSSP, VSSA to VSS		-0.3 to 0.3	V
VSS, VSYS, DRM, DRLx, DRHx, REGO RMS current(1)		0.2	A_{RMS}
VSSP RMS current(1)		0.4	A_{RMS}
VP RMS current(1)		0.6	A_{RMS}
Operating temperature range		-40 to 105	°C
Electrostatic discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV
	Machine model (JEDEC)	200	V

(1) Peak current can be 10 times higher than RMS value for pulses shorter than 10μs.

6. ARCHITECTURAL BLOCK DIAGRAM

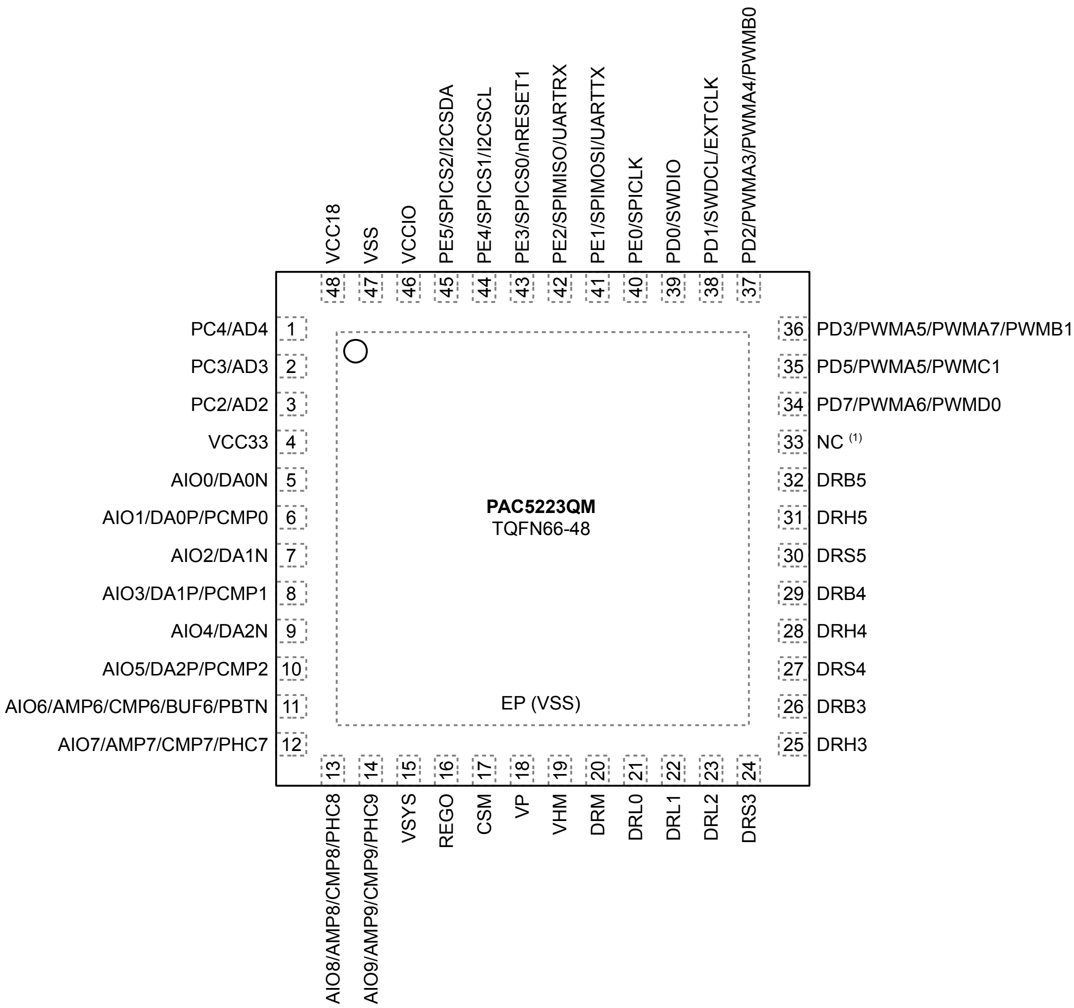
Figure 6-1. Architectural Block Diagram



7. PIN CONFIGURATION

7.1. PAC5223QM

Figure 7-1. PAC5223QM Pin Configuration (TQFN66-48 Package)



(1) Recommend to leave pin 33 unconnected.

8. FEATURES

- Proprietary Multi-Mode Power Manager
  - Multi-mode switching supply controller configurable for high-voltage buck SEPIC or AC/DC Flyback topologies
  - DC supply up to 70V or line AC input
  - 4 linear regulators with power and hibernate management
  - Power and temperature monitor, warning, and fault detection
- Proprietary Configurable Analog Front End
  - 10 analog front end I/O pins
  - 3 differential programmable gain amplifiers
  - 4 single-ended programmable gain amplifiers
  - 10 comparators
  - 2 DACs (10-bit and 8-bit)
- Proprietary Application Specific Power Drivers
  - 3 low-side and 3 high-side gate drivers with 1A gate driving capability
  - Configurable delays and fast fault protection
- 50MHz ARM Cortex-M0 32-bit microcontroller core
  - Fast single cycle 32-bit x 32-bit multiplier
  - 24-bit SysTick timer
  - Nested vectored interrupt controller (NVIC) with 20 external interrupts
  - Wake-up interrupt controller allowing power-saving sleep modes
  - Clock-gating allowing low power operation
- 32kB FLASH and 8kB SRAM memory
- 10-bit 1µs ADC with multi-input/multi-sample control engine
  - 9 ADC inputs including input from configurable analog front end
- 3.3V I/Os
  - 3 general purpose I/Os with tri-state and dedicated analog input to ADC
- True 5V I/Os
  - 12 general purpose I/Os with tri-state, pull-up and pull-down and dedicated I/O supply
  - Configurable as true 5V or 3.3V I/Os
- Flexible clock and PLL from internal 2% oscillator, ring oscillator, external clock, or crystal
- 9 timing generators
  - Four 16-bit timers with up to 16 PWM/CC blocks and 7 independent dead-time controllers
  - 24-bit watchdog timer
  - 4s or 8s watchdog timer
  - 24-bit real time clock
  - 24-bit SysTick timer
  - Wake-up timer for sleep modes from 0.125s to 8s
- SPI, I^2C, and UART communication interfaces
- SWD debug interface with interface disable function

9. PIN DESCRIPTION

Table 4. Multi-Mode Power Manager and System Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
CSM	17	Analog	Switching supply current sense input. Connect to the positive side of the current sense resistor.
DRM	20	Analog	Switching supply driver output. Connect to the base or gate of the external power NPN or n-channel MOSFET. See *PAC User Guide* and application notes.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.
NC	33		No connection pin. Don't make any connection on this pin.
VSS	47	Power	Ground.
REGO	16	Power	System regulator output. Connect to V_{SYS} directly or through an external power-dissipating resistor.
VCC18	48	Power	Internally generated 1.8V core power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VCC33	4	Power	Internally generated 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}. See PCB layout note below.
VCCIO	46	Power	Internally generated digital I/O power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VHM	19	Power	Switching supply controller supply input. Connect a 1µF or higher value ceramic capacitor, or a 0.1µF ceramic capacitor in parallel with a 10µF or higher electrolytic capacitor from V_{HM} to V_{SSP}. This pin requires good capacitive bypassing to V_{SSP}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VP	18	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 0.1µF ceramic capacitor from V_P pin to V_{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. See See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VSYS	15	Power	5V system power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{SYS} to V_{SSP}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.

Table 5. Configurable Analog Front End Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO0/DA0N	5	AIO0	I/O	Analog front end I/O 0.
		DA0N	Analog	Differential PGA 0 negative input.
AIO1/DA0P/PCMP0	6	AIO1	I/O	Analog front end I/O 1.
		DA0P	Analog	Differential PGA 0 positive input.
		PCMP0	Analog	Protection comparator input 0.
AIO2/DA1N	7	AIO2	I/O	Analog front end I/O 2.
		DA1N	Analog	Differential PGA 1 negative input.
AIO3/DA1P/PCMP1	8	AIO3	I/O	Analog front end I/O 3.
		DA1P	Analog	Differential PGA 1 positive input.
		PCMP1	Analog	Protection comparator input 1.
AIO4/DA2N	9	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 2 negative input.
AIO5/DA2P/PCMP2	10	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 2 positive input.
		PCMP2	Analog	Protection comparator input 2.
AIO6/AMP6/CMP6/BUF6/PBTN	11	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AIO7/AMP7/CMP7/PHC7	12	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8/AMP8/CMP8/PHC8	13	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9/AMP9/CMP9/PHC9	14	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

Table 6. Application Specific Power Drivers Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRB3	26	Analog	High-side gate driver bootstrap 3.
DRB4	29	Analog	High-side gate driver bootstrap 4.
DRB5	32	Analog	High-side gate driver bootstrap 5.
DRH3	25	Analog	High-side gate driver 3.
DRH4	28	Analog	High-side gate driver 4.
DRH5	31	Analog	High-side gate driver 5.
DRL0	21	Analog	Low-side gate driver 0.
DRL1	22	Analog	Low-side gate driver 1.
DRL2	23	Analog	Low-side gate driver 2.
DRS3	24	Analog	High-side gate driver source 3.
DRS4	27	Analog	High-side gate driver source 4.
DRS5	30	Analog	High-side gate driver source 5.

Table 7. I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PC2/AD2	3	PC2	I/O	I/O port C2.
		AD2	Analog	ADC input 2.
PC3/AD3	2	PC3	I/O	I/O port C3.
		AD3	Analog	ADC input 3.
PC4/AD4	1	PC4	I/O	I/O port C4.
		AD4	Analog	ADC input 4.

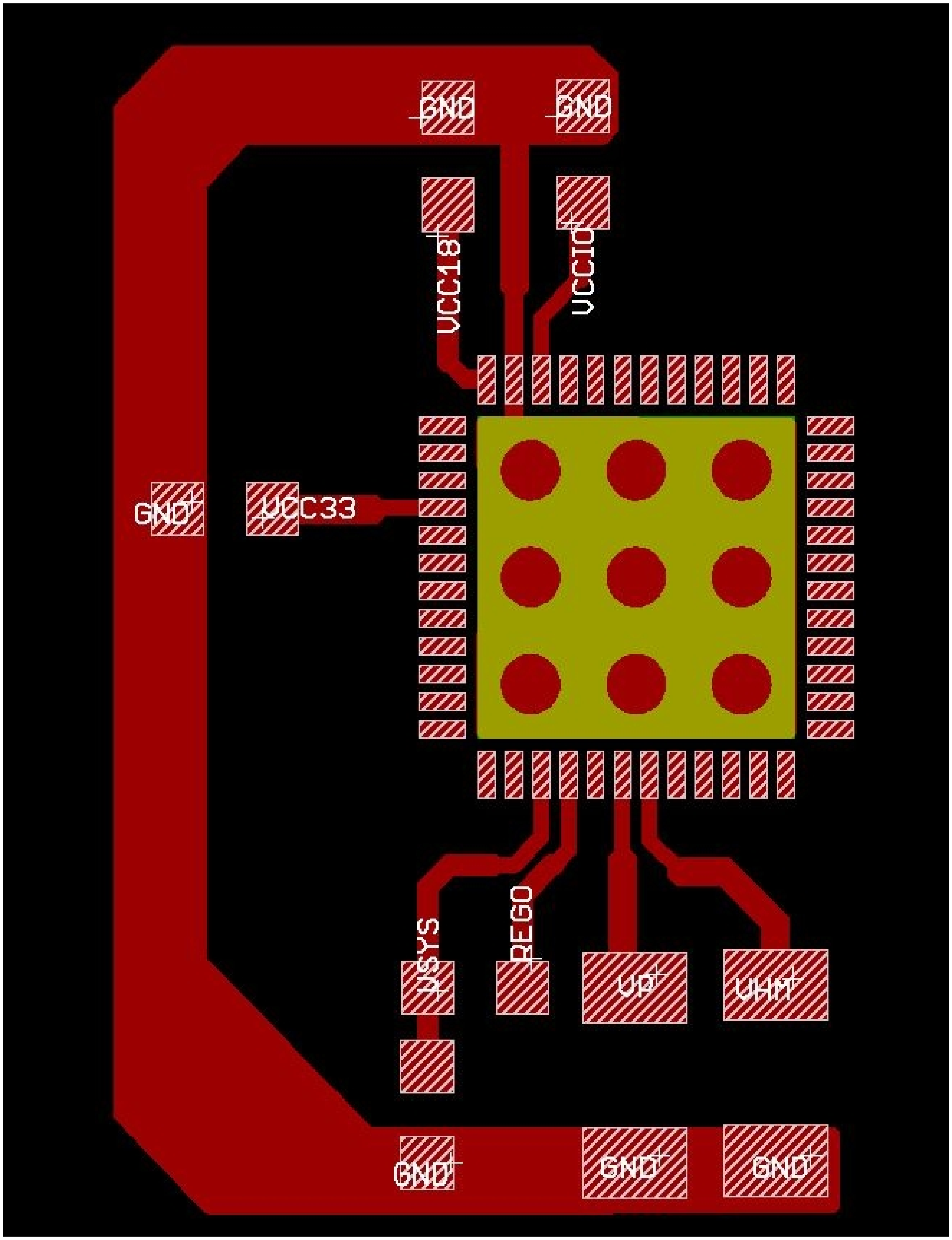
Table 8. I/O Ports Pin Description (Continued)

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PD0/SWDIO	39	PD0	I/O	I/O port D0.
		SWDIO	I/O	Serial wire debug I/O.
PD1/SWDCL/EXTCLK	38	PD1	I/O	I/O port D1.
		SWDCL	I	Serial wire debug clock.
		EXTCLK	I	External clock.
PD2/PWMA3/PWMA4/PWMB0	37	PD2	I/O	I/O port D2.
		PWMA3	I/O	Timer A PWM/capture 3.
		PWMA4	I/O	Timer A PWM/capture 4.
		PWMB0	I/O	Timer B PWM/capture 0.
PD3/PWMA5/PWMA7/PWMB1	36	PD3	I/O	I/O port D3.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMB1	I/O	Timer B PWM/capture 1.
PD5/PWMA5/PWMC1	35	PD5	I/O	I/O port D5.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMC1	I/O	Timer C PWM/capture 1.
PD7/PWMA6/PWMD0	34	PD7	I/O	I/O port D7.
		PWMA6	I/O	Timer A PWM/capture 6.
		PWMD0	I/O	Timer D PWM/capture 0.
PE0/SPICLK	40	PE0	I/O	I/O port E0.
		SPICLK	I/O	SPI clock.
PE1/SPIMOSI/UARTTX	41	PE1	I/O	I/O port E1.
		SPIMOSI	I/O	SPI master out slave in (MOSI).
		UARTTX	O	UART transmit output.
PE2/SPIMISO/UARTRX	42	PE2	I/O	I/O port E2.
		SPIMISO	I/O	SPI master in slave out (MISO).
		UARTRX	I	UART receive input.

Table 9. I/O Ports Pin Description (Continued)

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PE3/SPICS0/nRESET1	43	PE3	I/O	I/O port E3.
		SPICS0	O	SPI chip select 0.
		nRESET1	I	Reset input 1 (active low).
PE4/SPICS1/I2CSCL	44	PE4	I/O	I/O port E4.
		SPICS1	O	SPI chip select 1.
		I2CSCL	I/O	I2C clock.
PE5/SPICS2/I2CSDA	45	PE5	I/O	I/O port E5.
		SPICS2	O	SPI chip select 2.
		I2CSDA	I/O	I2C data.

Figure 9-1. Power Supply Bypass Capacitor Routing



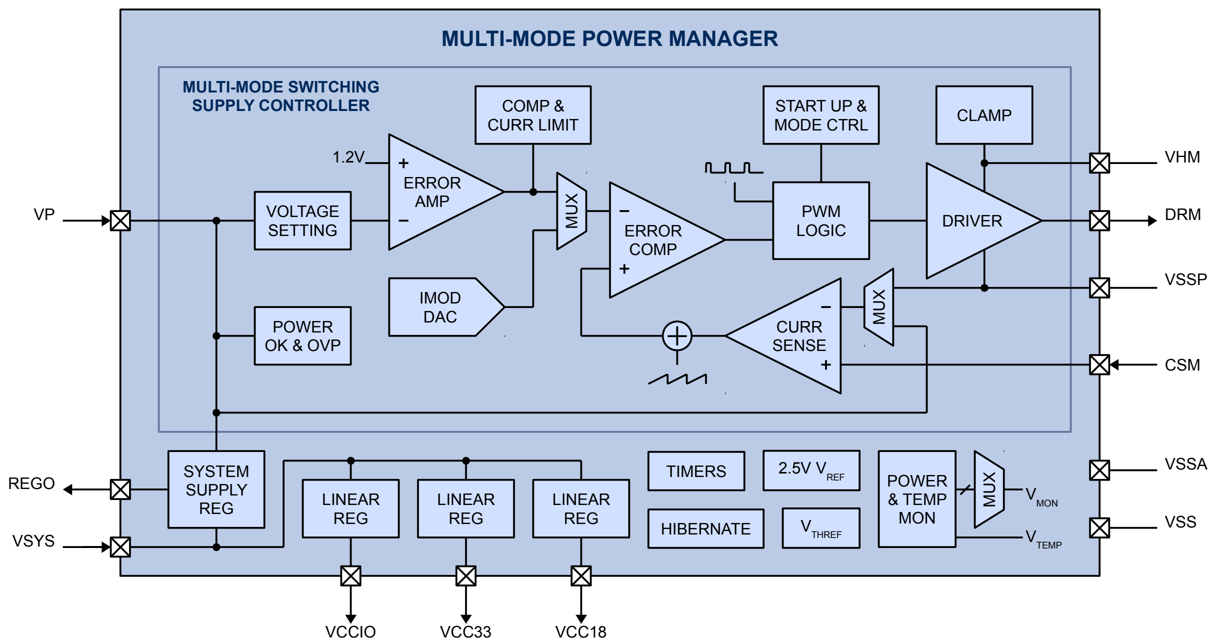
10. MULTI-MODE POWER MANAGER (MMPM)

10.1. Features

- Multi-mode switching supply controller configurable as high voltage buck, SEPIC or AC/DC Flyback
- DC supply up to 70V or line AC input
- 4 linear regulators with power and hibernate management
- Power and temperature monitor, warning, and fault detection

10.2. Block Diagram

Figure 10-1. Multi-Mode Power Manager



10.3. Functional Description

The Multi-Mode Power Manager (Figure 10-1) is optimized to efficiently provide "all-in-one" power management required by the PAC and associated application circuitry from a wide range of input power sources. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a buck, SEPIC or AC/DC flyback converter to efficiently convert power from a DC input source to generate a main supply output V_P. Four linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supplies for 5V system, 5V or 3.3V I/O, 3.3V mixed signal, and 1.8V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

10.3.1. Multi-Mode Switching Supply (MMSS) Controller

The MMSS controller drives an external power transistor for pulse-width modulation switching of an inductor or transformer for power conversion. The DRM output drives the gate of the n-channel MOSFET or the base of the NPN between the V_{HM} on state and V_{SSP} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The V_P regulation voltage is initially set to 15V during start up, and can be reconfigured to be 5V, 9V, or 12V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. In the high-side current sense buck or SEPIC mode, the inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.26V. In the low-side current sense flyback mode, the inductor current signal is sensed differentially between the CSM pin and V_{SSP}, and has a peak current limit threshold of 1V.

The MMSS controller is flexible and configurable as a buck, SEPIC or an AC/DC converter. Input sources include battery supply for buck mode (Figure 10-2) or SEPIC mode (Figure 10-3), and AC Line Supply for AC/DC Flyback (Figure 10-4). The MMSS controller operational mode is determined by external configuration and register settings from the microcontroller after power up. It can operate in either high-side or low-side current sense mode, and does not require external feedback loop compensation circuitry. For optional extended application range, the MMSS also incorporates additional digital control by the microcontroller to add accurate computations for outer feedback loop control such as power factor correction and accurate current control.

Figure 10-2. Buck Mode

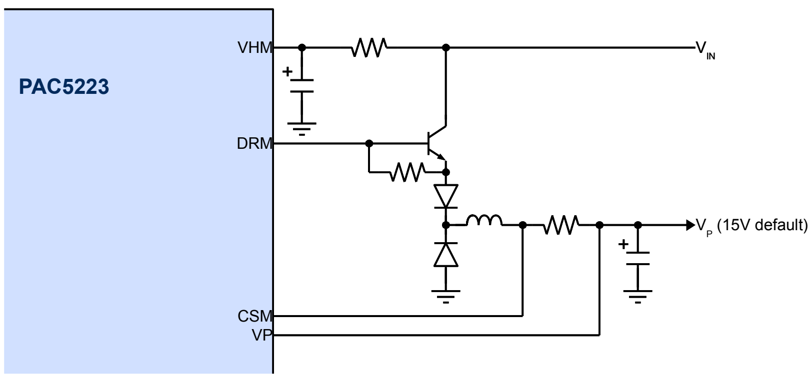


Figure 10-3. SEPIC Mode

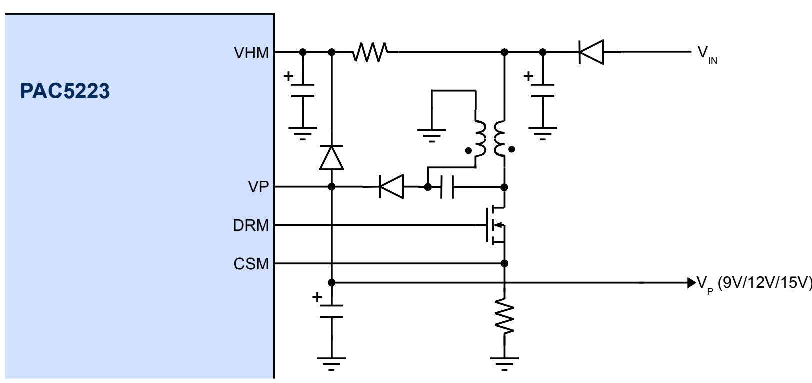
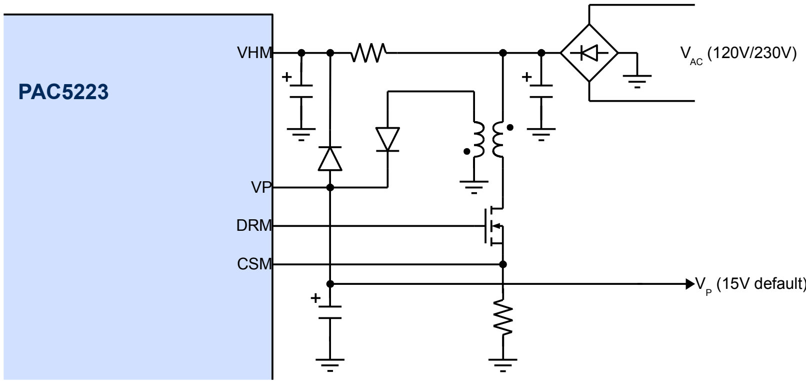


Figure 10-4. Flyback Mode



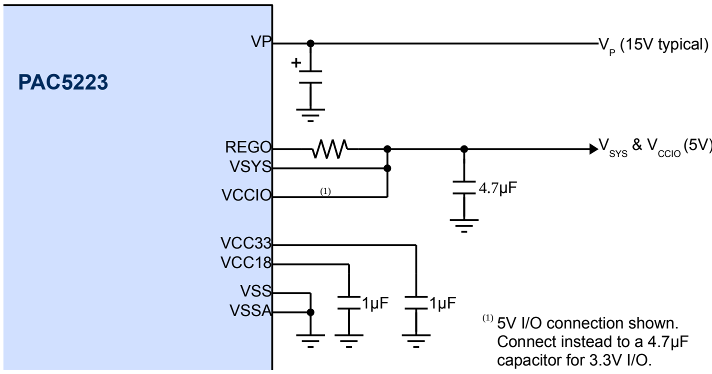
The MMSS detects and selects between high-side and low-side mode during start up based on the placement of the current sense resistor and the CSM pin voltage. It employs a safe start up mode with a 9.5kHz switching frequency until V_P exceeds 4.3V under-voltage-lockout threshold, then transitions to the 45kHz default switching frequency for at least 6ms to bring V_P close to the target voltage, before enabling the linear regulators. Any extra load should only be applied after the supplies are available and the microprocessor has initialized. The switching frequency can be reconfigured by the microprocessor to be 181kHz to 500kHz in the high switching frequency mode for battery-based applications, and to be 45kHz to 125kHz in the low switching frequency mode for AC applications. Upon initialization, the microcontroller must reconfigure the MMSS to the desired settings for V_P regulation voltage, switching mode, switching frequency, and V_{HM} clamp. Refer to the PAC application notes and user guide for MMSS controller design and programming.

If a stable external 5V to 18V power source is available, it can power the V_P main supply and all the linear regulators directly without requiring the MMSS controller to operate. In such applications, V_{HM} can be connected directly to V_P and the microcontroller should disable the MMSS upon initialization to reduce power loss.

10.3.2. Linear Regulators

The MMPM includes up to four linear regulators. The system supply regulator is a medium voltage regulator that takes the V_P supply and sources up to 200mA at REGO until V_{SYS}, externally coupled to REGO, reaches 5V. This allows a properly rated external resistor to be connected from REGO to V_{SYS} to close the current loop and offload power dissipation between V_P and V_{SYS}. Once V_{SYS} is above 4V, the three additional 40mA linear regulators for V_{CCIO}, V_{CC33}, and V_{CC18} supplies sequentially power up. Figure 10-5 shows typical circuit connections for the linear regulators. For 5V I/O systems, short the V_{CCIO} pin to V_{SYS} to bypass the V_{CCIO} regulator. For 3.3V I/O systems, the V_{CCIO} regulator generates 3.3V. The V_{CC33} and V_{CC18} regulators generate 3.3V and 1.8V, respectively. When V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

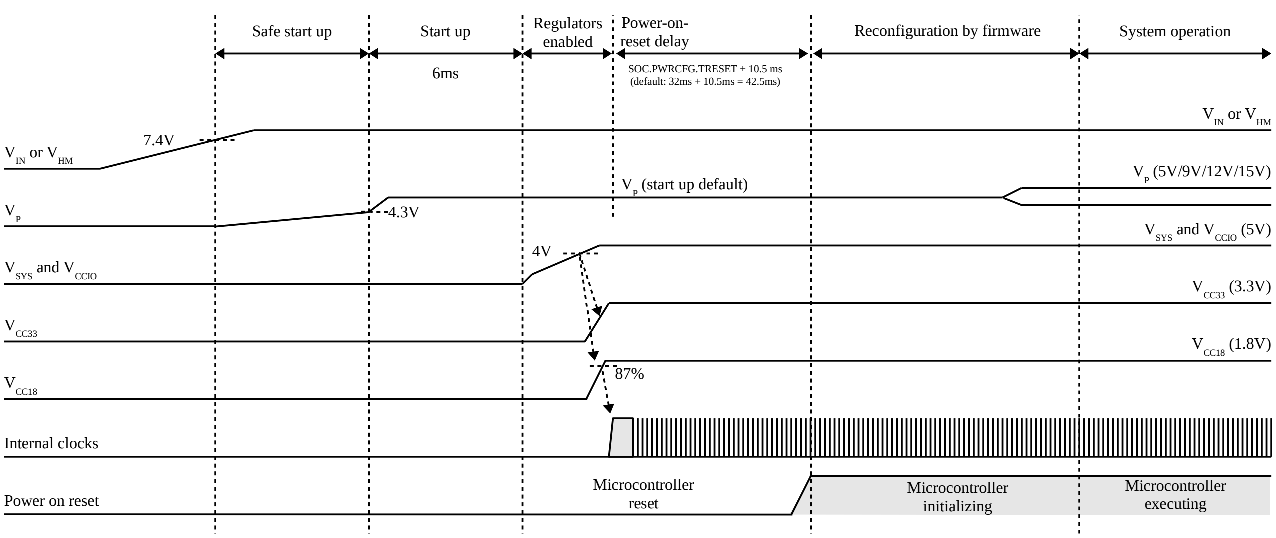
Figure 10-5. Linear Regulators



10.3.3. Power Up Sequence

The MMPM follows a typical power up sequence as in the Figure 10-6 below. A typical sequence begins with input power supply being applied, followed by the safe start up and start up durations to bring the switching supply output V_P to 15V, before the linear regulators are enabled. When all the supplies are ready, the internal clocks become available, and the microcontroller starts executing from the program memory. During initialization, the microcontroller can reconfigure the switching supply to a different V_P regulation voltage such as 15V and to an appropriate switching frequency and switching mode. The total loading on the switching supply must be kept below 25% of the maximum output current until after the reconfiguration of the switching supply is complete. For AC input supply applications, the start up sequence includes an additional charging time for V_{HM} depending on the start-up resistor and capacitor values.

Figure 10-6. Power Up Sequence



10.3.4. Hibernate Mode

The IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount (typically 18µA) of current is used by V_{HM}, and the MMSS controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from

125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

10.3.5. Power and Temperature Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CC18} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 170°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be V_{CC18}, 0.4•V_{CC33}, 0.4•V_{CCIO}, 0.4•V_{SYS}, 0.1•V_{REGO}, 0.1•V_P, 0.0333•V_{HM}, or the internal compensation voltage V_{COMP} for switching supply power monitoring.

For power and temperature warning, a V_P low event at 77% of the regulation voltage and an IC temperature warning event at 140°C are provided as maskable interrupts to the microcontroller. These warnings allow the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal $V_{TEMP} = 1.5 + 5.04e\text{-}3 \cdot (T - 25°C)$ (V) is provided onto the ADC pre-multiplexer for IC temperature measurement.

10.3.6. Voltage Reference

The reference block includes a 2.5V high precision reference voltage that provides the 2.5V reference voltage for the ADC, the DACs, and the 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

10.4. Electrical Characteristics

Table 10. Multi-Mode Switching Supply Controller Electrical Characteristics

(V_{HM} = 24V, V_P = 12V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply (V_{HM})						
$I_{HIB;VHM}$	V_{HM} hibernate mode supply current	V_{HM}, hibernate mode		18	36	µA
$I_{SU;VHM}$	V_{HM} start up supply current	$V_{HM} < V_{UVLOR;VHM}$		75	120	µA
$I_{OP;VHM}$	V_{HM} operating supply current	DRM floating		0.3	0.5	mA
$V_{OP;VHM}$	V_{HM} operating voltage range		5.0		70	V
$V_{UVLOR;VHM}$	V_{HM} under-voltage lockout rising		6.1	7.4	8	V
$V_{UVLOF;VHM}$	V_{HM} under-voltage lockout falling		5.1	6.6	7	V
$V_{CLAMP;VHM}$	V_{HM} clamp voltage	Clamp enabled, sink current = 100µA	14.5	16.9	19.5	V
$I_{CLAMP;VHM}$	V_{HM} clamp sink current limit	Clamp enabled		4		mA
Output Supply and Feedback (V_P)						
$V_{REG;VP}$	V_P output regulation voltage	Programmable to 5V, 9V, 12V, or 15V Load = 0 to 500mA	-7	-1	5	%
$k_{POK;VP}$	V_P power OK threshold	V_P rising, hysteresis = 10%	82	87	92	%
$k_{OVP;VP}$	V_P over voltage protection threshold	V_P rising, hysteresis = 15% MMPM Controller enabled		136		%
Switching Control						
$f_{SWMACC;DRM}$	Switching frequency accuracy		-10		10	%
$f_{SWM;DRM}$	Switching frequency programmable range	High frequency mode, 8 settings	181		500	kHz
		Low frequency mode, 8 settings	45		125	kHz
$f_{SSU;DRM}$	Safe start up switching frequency			9.5		kHz
$t_{ONMIN;DRM}$	Minimum on time			440		ns
$t_{OFFMIN;DRM}$	Minimum off time	Low duty-cycle & Low-frequency mode		25		%
		Low duty-cycle & High frequency mode		440		nS
		High duty-cycle mode		820		nS