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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# APEX II

## Programmable Logic Device Family

August 2002, ver. 3.0 — Data Sheet

## Features...

- Programmable logic device (PLD) manufactured using a 0.15-µm all-layer copper-metal fabrication process (up to eight layers of metal)
  - 1-gigabit per second (Gbps) True-LVDS™, LVPECL, pseudo current mode logic (PCML), and HyperTransport™ interface
  - Clock-data synchronization (CDS) in True-LVDS interface to correct any fixed clock-to-data skew
  - Enables common networking and communications bus I/O standards such as RapidIO™, CSIX, Utopia IV, and POS-PHY Level 4
  - Support for high-speed external memory interfaces, including zero bus turnaround (ZBT), quad data rate (QDR), and double data rate (DDR) static RAM (SRAM), and single data rate (SDR) and DDR synchronous dynamic RAM (SDRAM)
  - 30% to 40% faster design performance than APEX™ 20KE devices on average
  - Enhanced 4,096-bit embedded system blocks (ESBs) implementing first-in first-out (FIFO) buffers, Dual-Port+ RAM (bidirectional dual-port RAM), and content-addressable memory (CAM)
  - High-performance, low-power copper interconnect
  - Fast parallel byte-wide synchronous device configuration
  - Look-up table (LUT) logic available for register-intensive functions
- High-density architecture
  - 1,900,000 to 5,250,000 maximum system gates (see Table 1)
  - Up to 67,200 logic elements (LEs)
  - Up to 1,146,880 RAM bits that can be used without reducing available logic
- Low-power operation design
  - 1.5-V supply voltage
  - Copper interconnect reduces power consumption
  - MultiVolt™ I/O support for 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces
  - ESBs offer programmable power-saving mode

*Table 1. APEX II Device Features*

| Feature | EP2A15 | EP2A25 | EP2A40 | EP2A70 |
|---|---|---|---|---|
| Maximum gates | 1,900,000 | 2,750,000 | 3,000,000 | 5,250,000 |
| Typical gates | 600,000 | 900,000 | 1,500,000 | 3,000,000 |
| LEs | 16,640 | 24,320 | 38,400 | 67,200 |
| RAM ESBs | 104 | 152 | 160 | 280 |
| Maximum RAM bits | 425,984 | 622,592 | 655,360 | 1,146,880 |
| True-LVDS channels | 36 *(1)* | 36 *(1)* | 36 *(1)* | 36 *(1)* |
| Flexible-LVDS™ channels *(2)* | 56 | 56 | 88 | 88 |
| True-LVDS PLLs *(3)* | 4 | 4 | 4 | 4 |
| General-purpose PLL outputs *(4)* | 8 | 8 | 8 | 8 |
| Maximum user I/O pins | 492 | 612 | 735 | 1,060 |

*Notes to Table 1:*
(1) Each device has 36 input channels and 36 output channels.
(2) EP2A15 and EP2A25 devices have 56 input and 56 output channels; EP2A40 and EP2A70 devices have 88 input and 88 output channels.
(3) PLL: phase-locked loop. True-LVDS PLLs are dedicated to implement True-LVDS functionality.
(4) Two internal outputs per PLL are available. Additionally, the device has one external output per PLL pair (two external outputs per device).

## ...and More Features

- I/O features
  - Up to 380 Gbps of I/O capability
  - 1-Gbps True-LVDS, LVPECL, PCML, and HyperTransport support on 36 input and 36 output channels that feature clock synchronization circuitry and independent clock multiplication and serialization/deserialization factors
  - Common networking and communications bus I/O standards such as RapidIO, CSIX, Utopia IV, and POS-PHY Level 4 enabled
  - 400-megabits per second (Mbps) Flexible-LVDS and HyperTransport support on up to 88 input and 88 output channels (input channels also support LVPECL)
  - Support for high-speed external memories, including ZBT, QDR, and DDR SRAM, and SDR and DDR SDRAM
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Compliant with 133-MHz PCI-X specifications
  - Support for other advanced I/O standards, including AGP, CTT, SSTL-3 and SSTL-2 Class I and II, GTL+, and HSTL Class I and II
  - Six dedicated registers in each I/O element (IOE): two input registers, two output registers, and two output-enable registers
  - Programmable bus hold feature
  - Programmable pull-up resistor on I/O pins available during user mode

  - Programmable output drive for 3.3-V LVTTL at 4 mA, 12 mA, 24 mA, or I/O standard levels
  - Programmable output slew-rate control reduces switching noise
  - Hot-socketing operation supported
  - Pull-up resistor on I/O pins before and during configuration
- Enhanced internal memory structure
  - High-density 4,096-bit ESBs
  - Dual-Port+ RAM with bidirectional read and write ports
  - Support for many other memory functions, including CAM, FIFO, and ROM
  - ESB packing mode partitions one ESB into two 2,048-bit blocks
- Device configuration
  - Fast byte-wide synchronous configuration minimizes in-circuit reconfiguration time
  - Device configuration supports multiple voltages (either 3.3 V and 2.5 V or 1.8 V)
- Flexible clock management circuitry with eight general-purpose PLL outputs
  - Four general-purpose PLLs with two outputs per PLL
  - Built-in low-skew clock tree
  - Eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication (by 1 to 160) and division (by 1 to 256)
  - ClockShift™ feature providing programmable clock phase and delay shifting with coarse (90°, 180°, or 270°) and fine (0.5 to 1.0 ns) resolution
- Advanced interconnect structure
  - All-layer copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allowing one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX II architecture

- LogicLock™ incremental design for intellectual property (IP) integration and team-based design
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Support for popular revision-control software packages, including PVCS, RCS, and SCCS

Tables 2 and 3 show the APEX II ball-grid array (BGA) and FineLine BGA™ device package sizes, options, and I/O pin counts.

*Table 2. APEX II Package Sizes*

| Feature | 672-Pin FineLine BGA | 724-Pin BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.27 | 1.00 | 1.00 |
| Area ($mm^2$) | 729 | 1,225 | 1,089 | 1,600 |
| Length × Width (mm × mm) | 27 × 27 | 35 × 35 | 33 × 33 | 40 × 40 |

*Table 3. APEX II Package Options & I/O Pin Count* *Notes (1), (2)*

| Feature | 672-Pin FineLine BGA | 724-Pin BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|
| EP2A15 | 492 | 492 | | |
| EP2A25 | 492 | 536 | | |
| EP2A40 | 492 | 536 | 735 | |
| EP2A70 | | 536 | | 1,060 |

*Notes to Table 3:*

(1) All APEX II devices support vertical migration within the same package (e.g., the designer can migrate between the EP2A15, EP2A25, and EP2A40 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, LVDS pins, and power pins are the same for a given package across device densities. Migration of I/O pins across densities requires the designer to cross reference the available I/O pins using the device pin-outs. This must be done for all planned densities for a given package type to identify which I/O pins are migratable.

(2) I/O pin counts include dedicated clock and fast I/O pins.

# General Description

APEX II devices integrate high-speed differential I/O support using the True-LVDS interface. The dedicated serializer, deserializer, and CDS circuitry in the True-LVDS interface support the LVDS, LVPECL, HyperTransport, and PCML I/O standards. Flexible-LVDS pins located in regular user I/O banks offer additional differential support, increasing the total device bandwidth. This circuitry, together with enhanced IOEs and support for numerous I/O standards, allows APEX II devices to meet high-speed interface requirements.

APEX II devices also include other high-performance features such as bidirectional dual-port RAM, CAM, general-purpose PLLs, and numerous global clocks.

## Configuration

The logic, circuitry, and interconnects in the APEX II architecture are configured with CMOS SRAM elements. APEX II devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs; APEX II devices can be configured on the board for the specific functionality required.

APEX II devices are configured at system power-up with data either stored in an Altera configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices, which configure APEX II devices via a serial data stream. The enhanced configuration devices can configure any APEX II device in under 100 ms. Moreover, APEX II devices contain an optimized interface that permits microprocessors to configure APEX II devices serially or in parallel, synchronously or asynchronously. This interface also enables microprocessors to treat APEX II devices as memory and to configure the device by writing to a virtual memory location, simplifying reconfiguration.

APEX II devices also support a new byte-wide, synchronous configuration scheme at speeds of up to 66 MHz using EPC16 configuration devices or a microprocessor. This parallel configuration reduces configuration time by using eight data lines to send configuration data versus one data line in serial configuration.

APEX II devices support multi-voltage configuration; device configuration can be performed at 3.3 V and 2.5 V or 1.8 V.

After an APEX II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

### Software

APEX II devices are supported by the Altera Quartus II development system: a single, integrated package that offers hardware description language (HDL) and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software includes the LogicLock incremental design feature. The LogicLock feature allows the designer to make pin and timing assignments, verify functionality and performance, and then set constraints to lock down the placement and performance of a specific block of logic using LogicLock constraints. Constraints set by the LogicLock function guarantee repeatable placement when implementing a block of logic in a current project or exporting the block to another project. The constraints set by the LogicLock feature can lock down logic to a fixed location in the device. The LogicLock feature can also lock the logic down to a floating location, and the Quartus II software determines the best relative placement of the block to meet design requirements. Adding additional logic to a project will not affect the performance of blocks locked down with LogicLock constraints.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can open the Quartus II software from within third-party design tools. The Quartus II software also contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX II devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX II architecture.

## Functional Description

APEX II devices incorporate LUT-based logic, product-term-based logic, memory, and high-speed I/O standards into one device. Signal interconnections within APEX II devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an IOE located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and six registers that can be used for registering input, output, and output-enable signals. When used with a dedicated clock pin, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM and ZBT and QDR SRAM devices.

IOEs provide a variety of features such as: 3.3-V, 64-bit, 66-MHz PCI compliance, 3.3-V, 64-bit, 133-MHz PCI-X compliance, Joint Test Action Group (JTAG) boundary-scan test (BST) support, output drive strength control, slew-rate control, tri-state buffers, bus-hold circuitry, programmable pull-up resistors, programmable input and output delays, and open-drain outputs.

APEX II devices offer enhanced I/O support, including support for 1.5 V, 1.8 V, 2.5 V, 3.3 V, LVCMOS, LVTTL, HSTL, LVDS, LVPECL, HyperTransport, PCML, 3.3-V PCI, PCI-X, GTL+, SSTL-2, SSTL-3, CTT, and 3.3-V AGP I/O standards. High-speed (up to 1.0 Gbps) differential transfers are supported with True-LVDS circuitry for LVDS, LVPECL, HyperTransport, and PCML I/O standards. The optional CDS feature corrects any clock-to-data skew at the True-LVDS receiver channels, allowing for flexible board topologies. Up to 88 Flexible-LVDS channels support differential transfer at up to 400 Mbps (DDR) for LVDS and HyperTransport I/O standards.

An ESB can implement many types of memory, including Dual-Port+ RAM, CAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. The abundance of cascadable ESBs ensures that the APEX II device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs, in conjunction with the ability for one ESB to implement two separate memory blocks, ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX II device.

*Figure 1. APEX II Device Block Diagram*

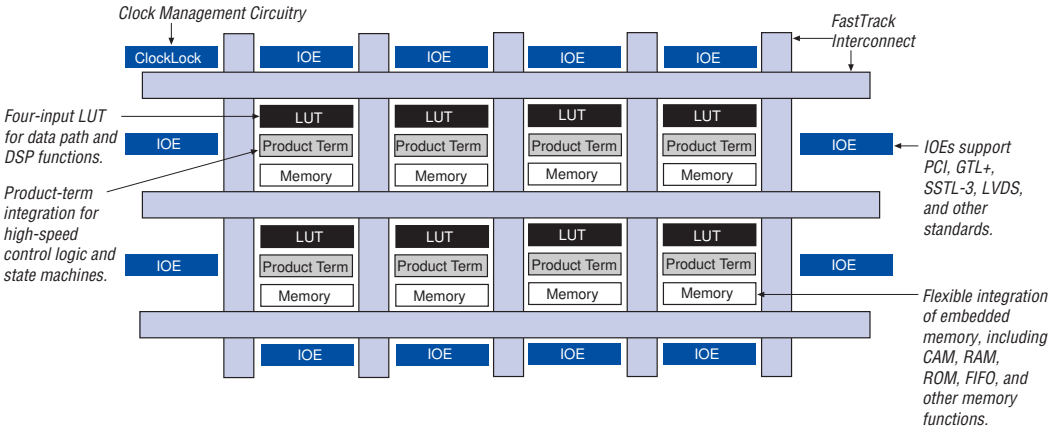



Table 4 lists the resources available in APEX II devices.

*Table 4. APEX II Device Resources*

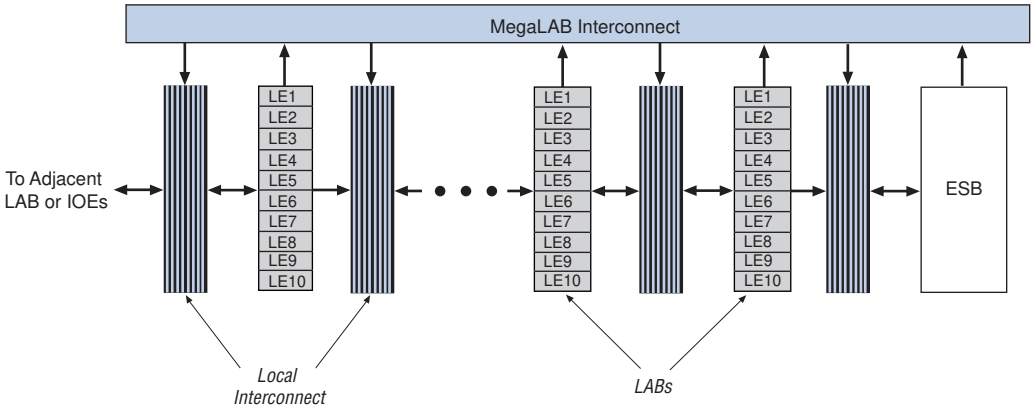
| Device | MegaLAB Rows | MegaLAB Columns | ESBs |
|---|---|---|---|
| EP2A15 | 26 | 4 | 104 |
| EP2A25 | 38 | 4 | 152 |
| EP2A40 | 40 | 4 | 160 |
| EP2A70 | 70 | 4 | 280 |

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

## MegaLAB Structure

APEX II devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. EP2A15 and EP2A25 devices have 16 LABs and EP2A40 and EP2A70 devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

*Figure 2. MegaLAB Structure*




## Logic Array Block

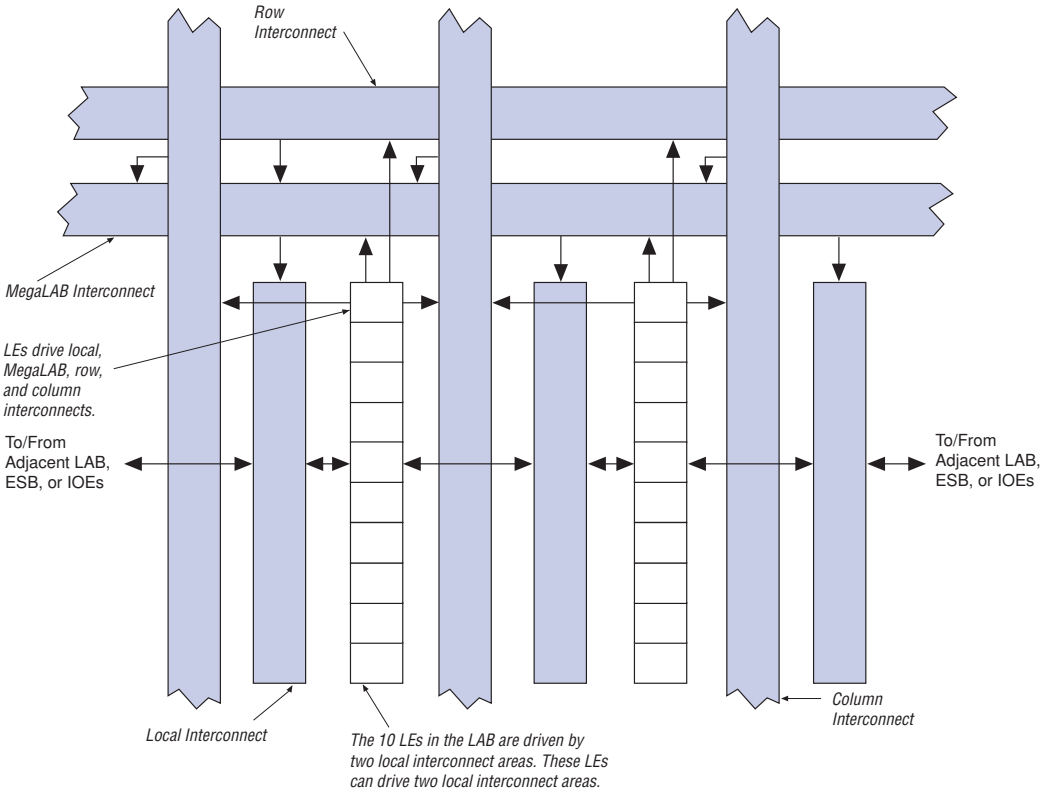
Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs.

The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance.

APEX II devices use an interleaved LAB structure, so that each LAB can drive two local interconnect areas. Every other LE drives to either the left or right local interconnect area, alternating by LE. The local interconnect can drive LEs within the same LAB or adjacent LABs. This feature minimizes the use of the row and column interconnects, providing higher performance and flexibility. Each LAB structure can drive 30 LEs through fast local interconnects.

Figure 3 shows the APEX II LAB.

*Figure 3. APEX II LAB Structure*

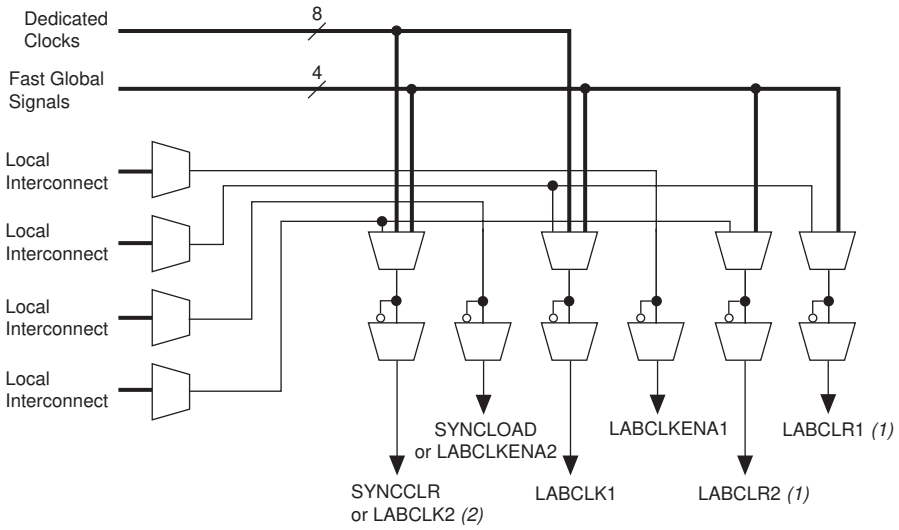



Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. The LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs. If both the rising and falling edges of a clock are used in an LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

*Figure 4. LAB Control Signal Generation*




*Notes to Figure 4:*

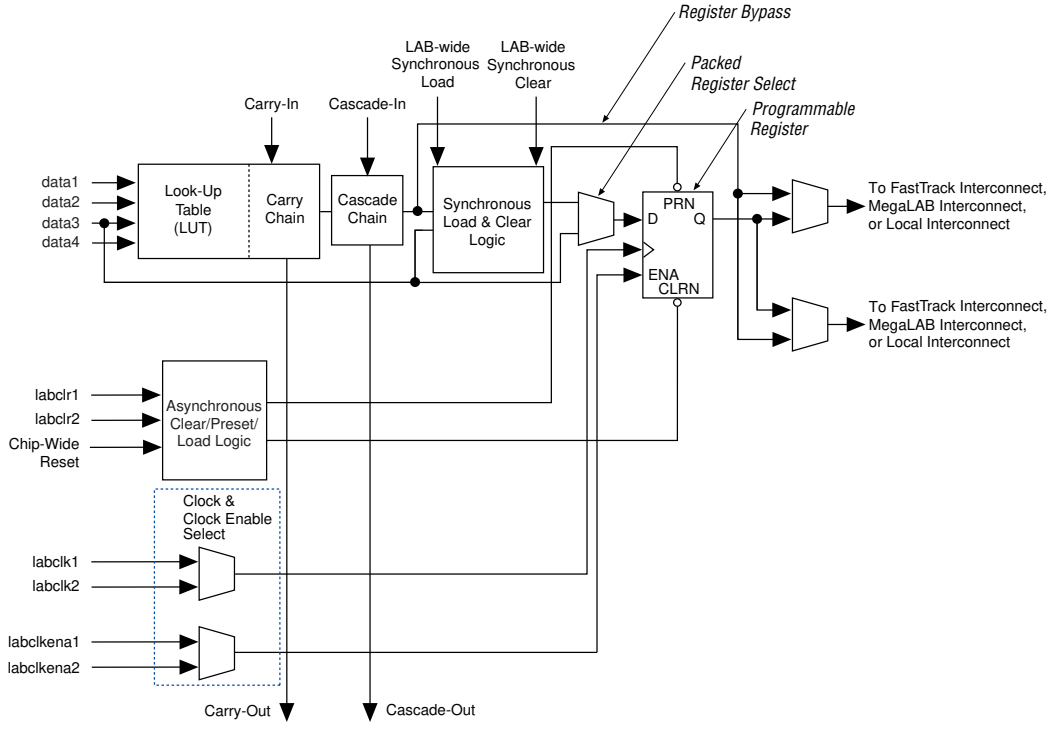
(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

## Logic Element

The LE is the smallest unit of logic in the APEX II architecture. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

*Figure 5. APEX II Logic Element*




Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

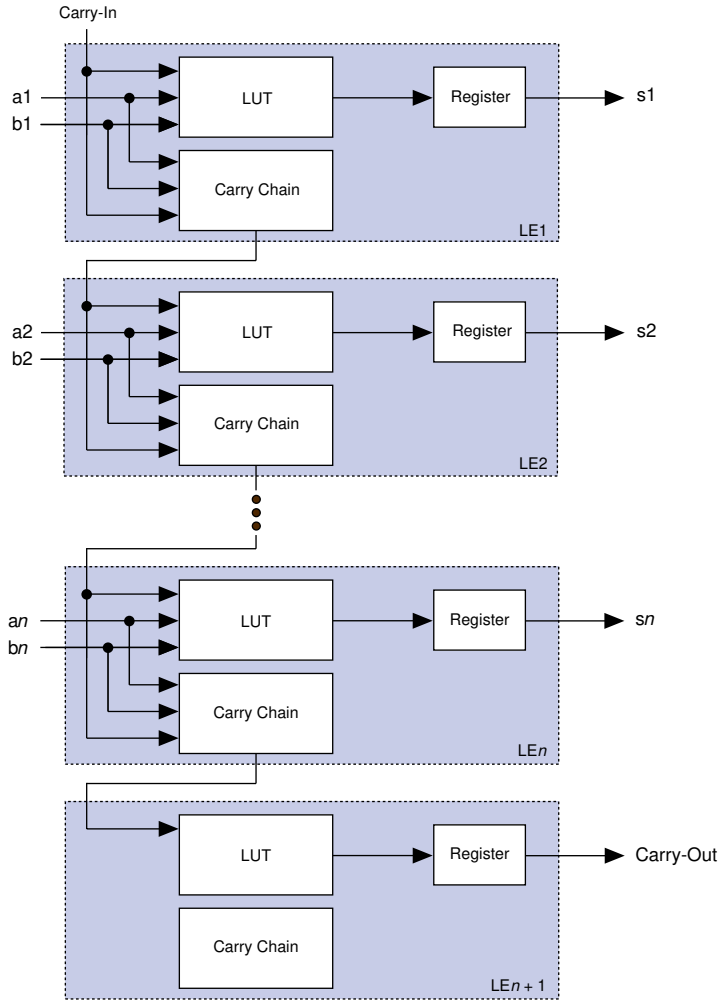
### *Carry Chain*

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

*Figure 6. APEX II Carry Chain*

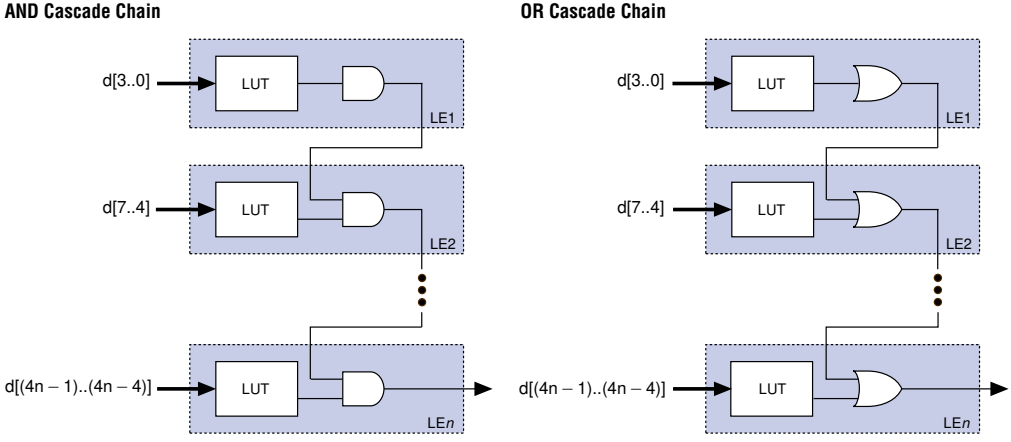


### *Cascade Chain*

With the cascade chain, the APEX II architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via DeMorgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. The Quartus II Compiler can create cascade chain logic automatically during the design process, or the designer can create it manually during design entry.

Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

***Figure 7. APEX II Cascade Chain***



### *LE Operating Modes*

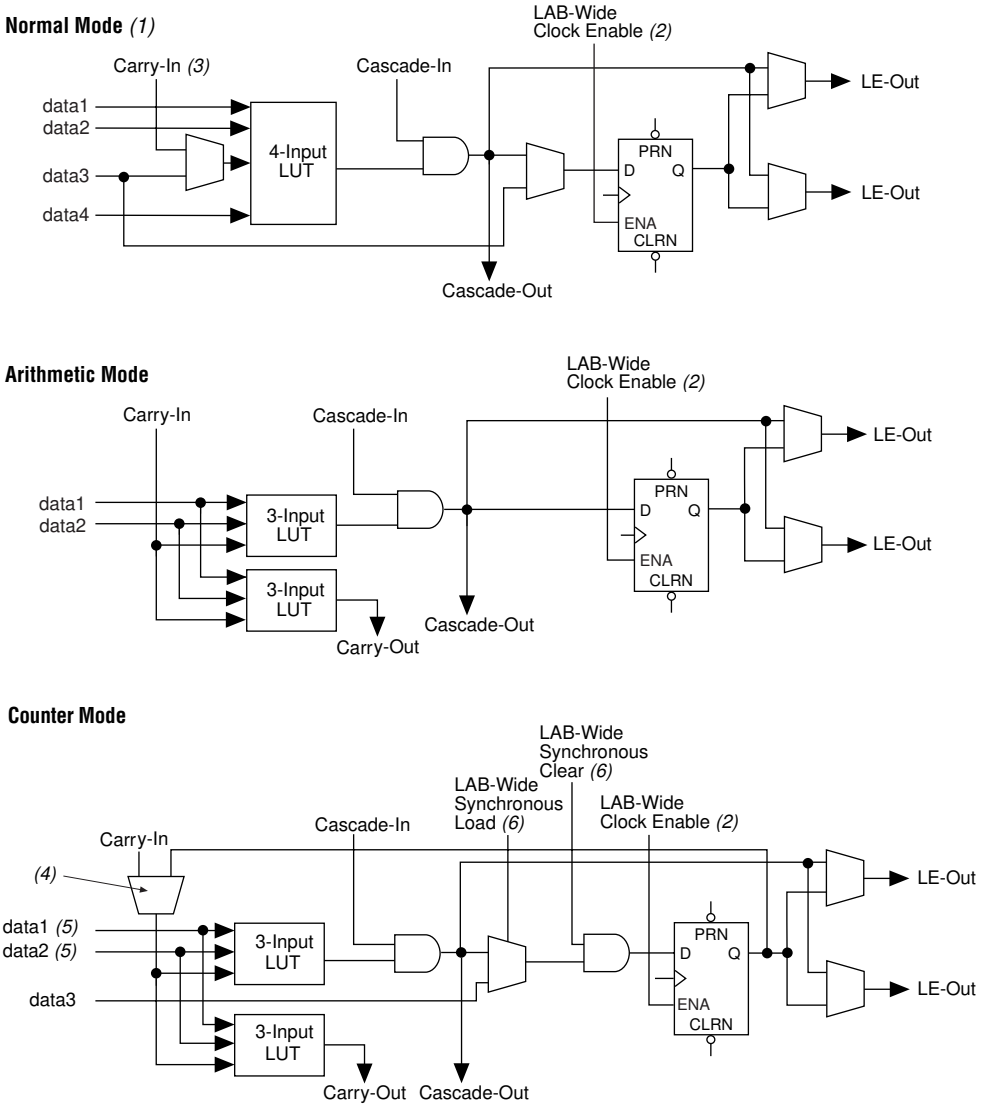
The APEX II LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

*Figure 8. APEX II LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The `DATA1` and `DATA2` input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in a LAB.
(6) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in a LAB.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

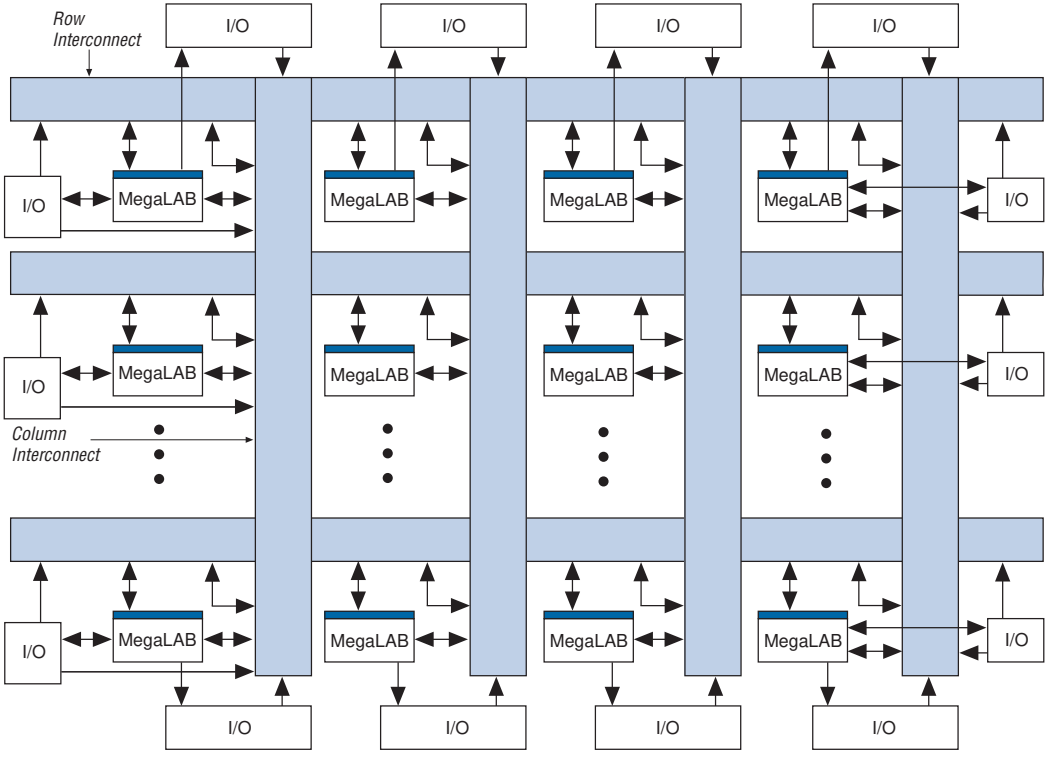
In addition to the two clear and preset modes, APEX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## FastTrack Interconnect

In the APEX II architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

*Figure 9. APEX II Interconnect Structure*




A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by the LEs, IOEs, or ESBs in that column. Row IOEs can drive a column line on a device's left or right edge. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

*Figure 10. FastTrack Connection to Local Interconnect*

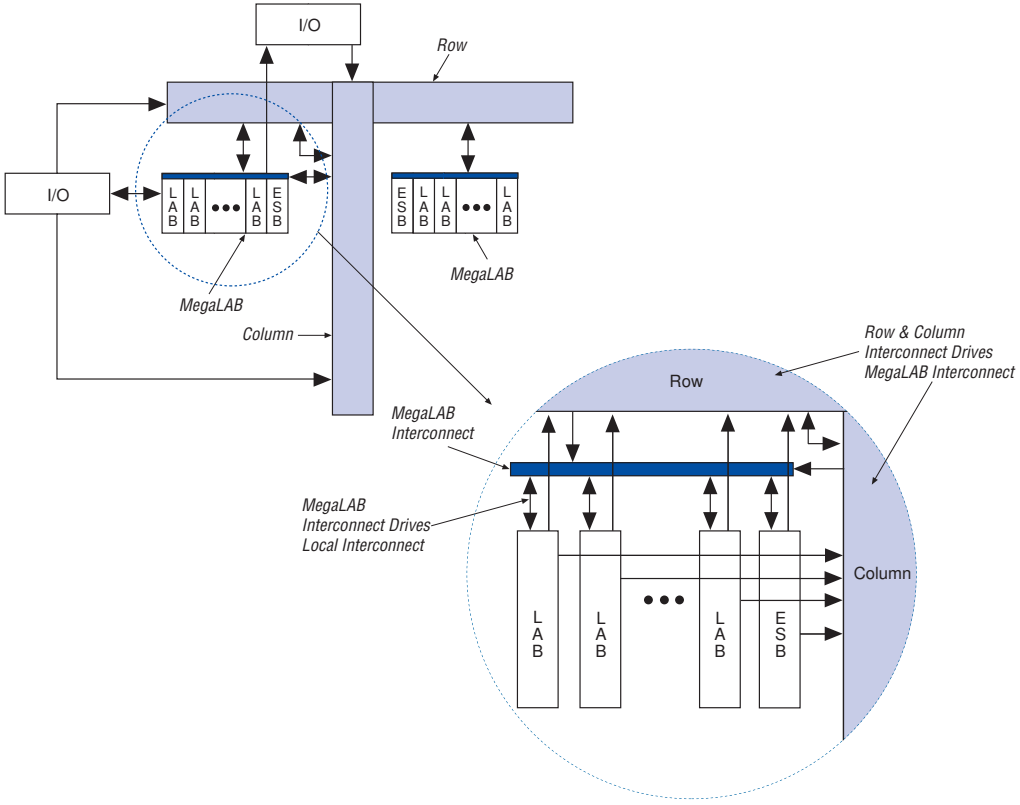
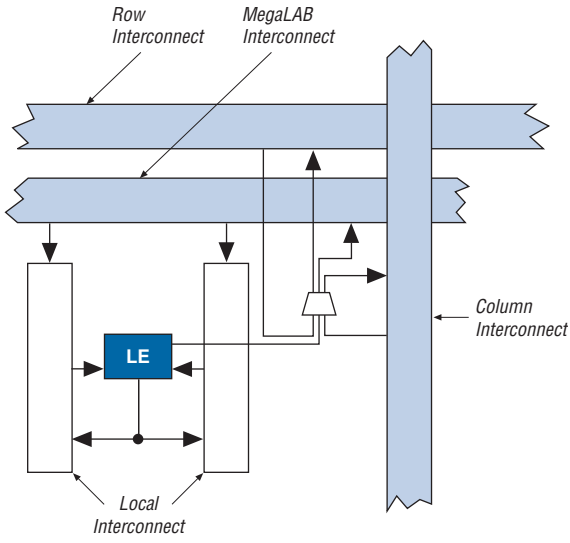



Figure 11 shows the intersection of a row and column interconnect and how these forms of interconnects and LEs drive each other.

*Figure 11. Driving the FastTrack Interconnect*




APEX II devices feature FastRow™ lines for quickly routing input signals with high fan-out. Column I/O pins can drive the FastRow interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. The FastRow interconnect drives the four MegaLABs in the top row and the four MegaLABs in the bottom row of the device. The FastRow interconnect drives all local interconnects in the appropriate MegaLABs. Column pins using the FastRow interconnect achieve a faster set-up time, because the signal does not need to use a MegaLab interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

*Figure 12. APEX II FastRow Interconnect*

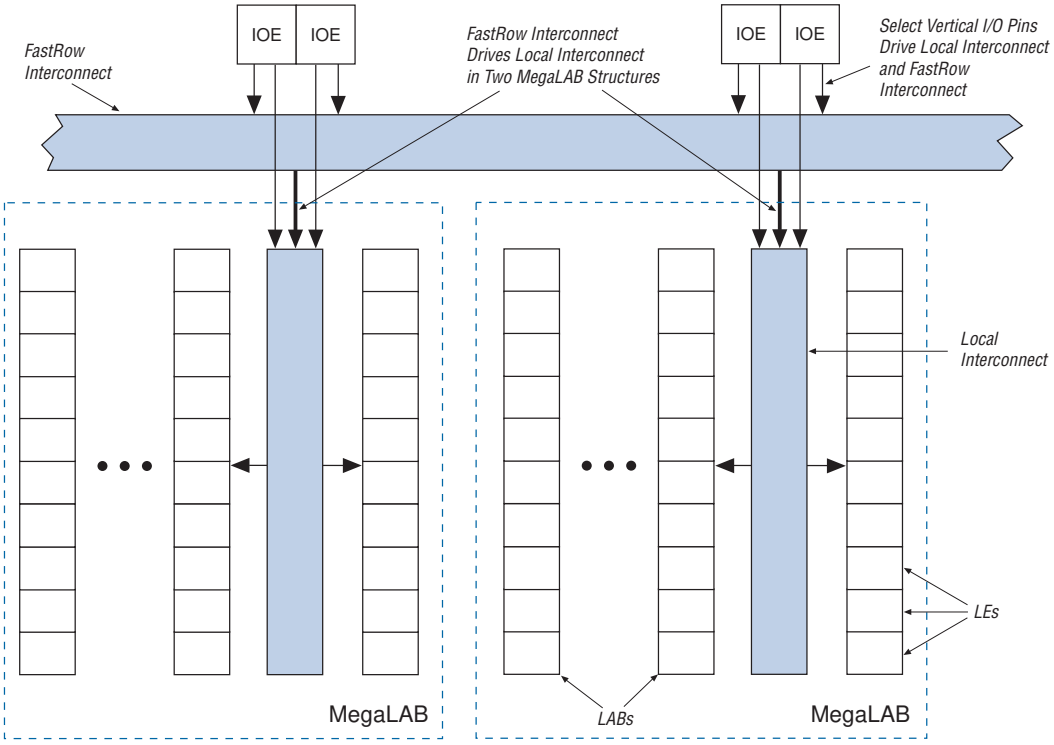


Table 5 summarizes how elements of the APEX II architecture drive each other.

*Table 5. APEX II Routing Scheme*

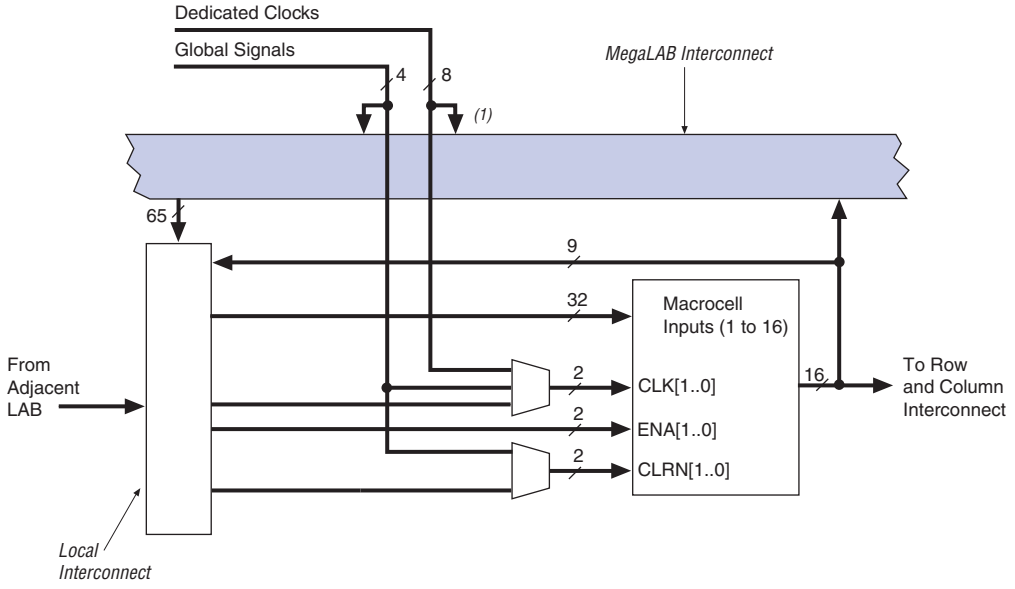
| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Row I/O Pin | Column I/O Pin | LE | ESB | Local Interconnect | MegaLAB Interconnect | Row FastTrack Interconnect | Column FastTrack Interconnect | FastRow Interconnect |
| Row I/O pin | | | | | ✓ | ✓ | ✓ | ✓ | |
| Column I/O pin | | | | | | | | ✓ | ✓ |
| LE | | | | | ✓ | ✓ | ✓ | ✓ | |
| ESB | | | | | ✓ | ✓ | ✓ | ✓ | |
| Local interconnect | ✓ | ✓ | ✓ | ✓ | | | | | |
| MegaLAB interconnect | | | | | ✓ | | | | |
| Row FastTrack interconnect | | | | | | ✓ | | ✓ | |
| Column FastTrack interconnect | | | | | | ✓ | ✓ | | |
| FastRow interconnect | | | | | ✓ | | | | |

## Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. 32 inputs from the adjacent local interconnect feed each ESB; therefore, the either MegaLAB or the adjacent LAB can drive the ESB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

*Figure 13. Product-Term Logic in ESB*




***Note ot Figure 13:***
(1) PLL outputs cannot drive data input ports.

### *Macrocells*

APEX II macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX II macrocell.