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Section I. Stratix II GX Device Data Sheet

This section provides designers with the data sheet specifications for Stratix® II GX devices. They contain feature definitions of the transceivers, internal architecture, configuration, and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II GX devices.

This section includes the following chapters:

- Chapter 1, Introduction
- Chapter 2, Stratix II GX Architecture
- Chapter 3, Configuration & Testing
- Chapter 4, DC and Switching Characteristics
- Chapter 5, Reference and Ordering Information

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. Introduction

SIIGX51001-1.6

The Stratix® II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock and data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

This section lists the Stratix II GX device features.

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 550 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 71 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory, including quad data rate (QDR and QDRII) SRAM, double data rate (DDR and DDR2) SDRAM, and single data rate (SDR) SDRAM

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM}) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

- Transceiver block features:
  - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
  - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
  - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
  - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
  - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
  - Receiver indicator for loss of signal (available only in PIPE mode)
  - Built-in self test (BIST)
  - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
  - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
  - Built-in byte ordering so that a frame or packet always starts in a known byte lane
  - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

- 8B/10B encoder and decoder perform 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
- Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
- Receiver FIFO resynchronizes the received data with the local reference clock
- Channel aligner compliant with XAUI

Certain transceiver blocks can be bypassed. Refer to the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook* for more details.

Table 1–1 lists the Stratix II GX device features.

Table 1–1. Stratix II GX Device Features (Part 1 of 2)

Feature	EP2SGX30C/D		EP2SGX60C/D/E			EP2SGX90E/F		EP2SGX130/G
	C	D	C	D	E	E	F	G
ALMs	13,552		24,176			36,384		53,016
Equivalent LEs	33,880		60,440			90,960		132,540
Transceiver channels	4	8	4	8	12	12	16	20
Transceiver data rate	600 Mbps to 6.375 Gbps		600 Mbps to 6.375 Gbps			600 Mbps to 6.375 Gbps		600 Mbps to 6.375 Gbps
Source-synchronous receive channels *(1)*	31		31	31	42	47	59	73
Source-synchronous transmit channels	29		29	29	42	45	59	71
M512 RAM blocks (32 × 18 bits)	202		329			488		699
M4K RAM blocks (128 × 36 bits)	144		255			408		609
M-RAM blocks (4K × 144 bits)	1		2			4		6
Total RAM bits	1,369,728		2,544,192			4,520,448		6,747,840
Embedded multipliers (18 × 18)	64		144			192		252
DSP blocks	16		36			48		63
PLLs	4		4	4	8	8		8
Maximum user I/O pins	361		364	364	534	558	650	734

Table 1–1. Stratix II GX Device Features (Part 2 of 2)

Feature	EP2SGX30C/D		EP2SGX60C/D/E			EP2SGX90E/F		EP2SGX130/G
	C	D	C	D	E	E	F	G
Package	780-pin FineLine BGA		780-pin FineLine BGA		1,152-pin FineLine BGA	1,152-pin FineLine BGA	1,508-pin FineLine BGA	1,508-pin FineLine BGA

Note to Table 1–1:
(1) Includes two sets of dual-purpose differential pins that can be used as two additional channels for the differential receiver or differential clock inputs.

Stratix II GX devices are available in space-saving FineLine BGA packages (refer to Table 1–2). All Stratix II GX devices support vertical migration within the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. Table 1–3 lists the Stratix II GX device package sizes.

Table 1–2. Stratix II GX Package Options (Pin Counts and Transceiver Channels)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive *(1)*	Transmit	780-Pin FineLine BGA (29 mm)	1,152-Pin FineLine BGA (35 mm)	1,508-Pin FineLine BGA (40 mm)
EP2SGX30C	4	31	29	361	—	—
EP2SGX60C	4	31	29	364	—	—
EP2SGX30D	8	31	29	361	—	—
EP2SGX60D	8	31	29	364	—	—
EP2SGX60E	12	42	42	—	534	—
EP2SGX90E	12	47	45	—	558	—
EP2SGX90F	16	59	59	—	—	650
EP2SGX130G	20	73	71	—	—	734

Note to Table 1–2:
(1) Includes two differential clock inputs that can also be used as two additional channels for the differential receiver.

Table 1–3. Stratix II GX FineLine BGA Package Sizes			
Dimension	**780 Pins**	**1,152 Pins**	**1,508 Pins**
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	841	1,225	1,600
Length width (mm × mm)	29 × 29	35 × 35	40 × 40

Referenced Document

This chapter references the following document:

- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*

Document Revision History

Table 1–4 shows the revision history for this chapter.

Table 1–4. Document Revision History		
Date and Document Version	**Changes Made**	**Summary of Changes**
October 2007, v1.6	Updated "Features" section.	
	Minor text edits.	
August 2007, v1.5	Added "Referenced Documents" section.	
	Minor text edits.	
February 2007, v1.4	• Changed 622 Mbps to 600 Mbps on page 1-2 and Table 1–1. • Deleted "DC coupling" from the Transceiver Block Features list. • Changed 4 to 6 in the PLLs row (columns 3 and 4) of Table 1–1.	
	Added the "Document Revision History" section to this chapter.	Added support information for the Stratix II GX device.
June 2006, v1.3	• Updated Table 1–2.	
April 2006, v1.2	• Updated Table 1–1. • Updated Table 1–2.	Updated numbers for receiver channels and user I/O pin counts in Table 1–2.
February 2006, v1.1	• Updated Table 1–1.	
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	

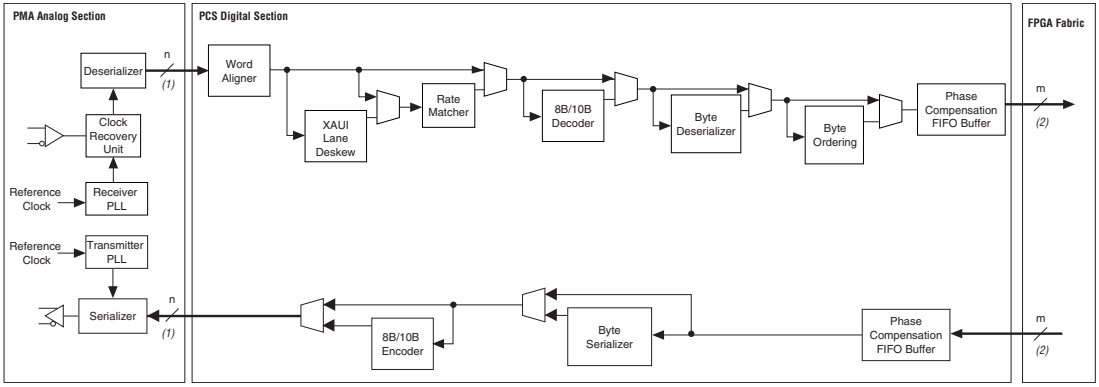
2. Stratix II GX Architecture

SIIGX51003-2.2

Transceivers

Stratix® II GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 6.375-Gbps serial transceiver channels. Each Stratix II GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceivers deliver bidirectional point-to-point data transmissions, with up to 51 Gbps (6.375 Gbps per channel) of full-duplex data transmission per transceiver block. Figure 2–1 shows the function blocks that make up a transceiver channel within the Stratix II GX device.

Figure 2–1. Stratix II GX Transceiver Block Diagram



Notes to Figure 2–1:

(1) *n* represents the number of bits in each word that need to be serialized by the transmitter portion of the PMA or have been deserialized by the receiver portion of the PMA. *n* = 8, 10, 16, or 20.

(2) *m* represents the number of bits in the word that pass between the FPGA logic and the PCS portion of the transceiver. *m* = 8, 10, 16, 20, 32, or 40.

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

There are up to 20 transceiver channels available on a single Stratix II GX device. Table 2–1 shows the number of transceiver channels and their serial bandwidth for each Stratix II GX device.

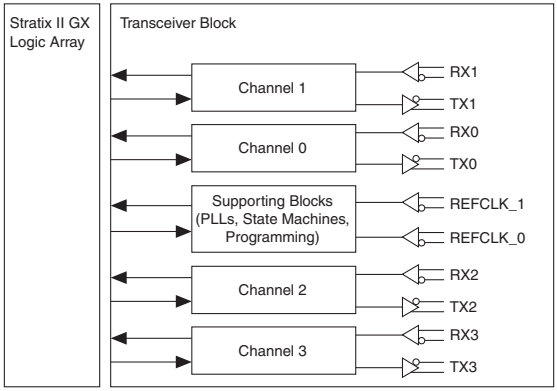
Table 2–1. Stratix II GX Transceiver Channels

Device	Number of Transceiver Channels	Serial Bandwidth (Full Duplex)
EP2SGX30C	4	51 Gbps
EP2SGX60C	4	51 Gbps
EP2SGX30D	8	102 Gbps
EP2SGX60D	8	102 Gbps
EP2SGX60E	12	153 Gbps
EP2SGX90E	12	153 Gbps
EP2SGX90F	16	204 Gbps
EP2SGX130G	20	255 Gbps

Figure 2–2 shows the elements of the transceiver block, including the four transceiver channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains two transmitter PLLs to generate the high-speed clock(s) used by the four transmitters within that block. Each of the four transmitter channels has its own individual clock divider. The four receiver PLLs within each transceiver block generate four recovered clocks. The transceiver channels can be configured in one of the following functional modes:

- PCI Express (PIPE)
- OIF CEI PHY Interface
- SONET/SDH
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps single-width mode and 1 Gbps to 6.375 Gbps double-width mode)
- SDI (HD, 3G)
- CPRI (614 Mbps, 1228 Mbps, 2456 Mbps)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Figure 2–2. Elements of the Transceiver Block



Each Stratix II GX transceiver channel consists of a transmitter and receiver. The transceivers are grouped in four and share PLL resources. Each transmitter has access to one of two PLLs. The transmitter contains the following:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Byte ordering
- Receiver phase compensation FIFO buffer

Designers can preset Stratix II GX transceiver functions using the Quartus® II software. In addition, pre-emphasis, equalization, and differential output voltage (V_{OD}) are dynamically programmable. Each Stratix II GX transceiver channel supports various loopback modes and is

capable of built-in self test (BIST) generation and verification. The ALT2GXB megafunction in the Quartus II software provides a step-by-step menu selection to configure the transceiver.

Figure 2–1 shows the block diagram for the Stratix II GX transceiver channel. Stratix II GX transceivers provide PCS and PMA implementations for all supported protocols. The PCS portion of the transceiver consists of the word aligner, lane deskew FIFO buffer, rate matcher FIFO buffer, 8B/10B encoder and decoder, byte serializer and deserializer, byte ordering, and phase compensation FIFO buffers.

Each Stratix II GX transceiver channel is also capable of BIST generation and verification in addition to various loopback modes. The PMA portion of the transceiver consists of the serializer and deserializer, the CRU, and the high-speed differential transceiver buffers that contain pre-emphasis, programmable on-chip termination (OCT), programmable voltage output differential (V_{OD}), and equalization.

Transmitter Path

This section describes the data path through the Stratix II GX transmitter. The Stratix II GX transmitter contains the following modules:

- Transmitter PLLs
- Access to one of two PLLs
- Transmitter logic array interface
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

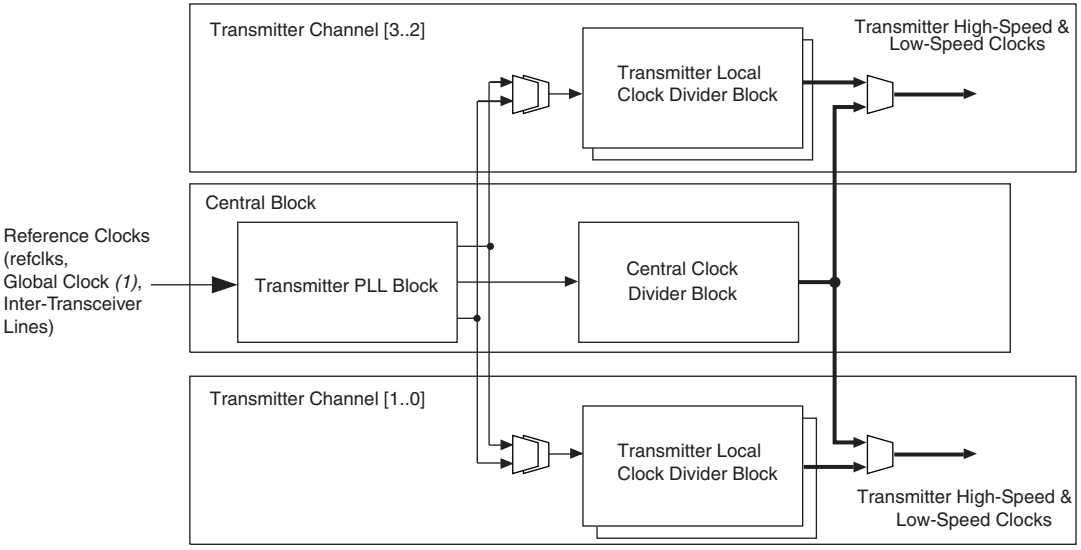
Transmitter PLLs

Each transceiver block has two transmitter PLLs which receive two reference clocks to generate timing and the following clocks:

- High-speed clock used by the serializer to transmit the high-speed differential transmitter data
- Low-speed clock to load the parallel transmitter data of the serializer

The serializer uses high-speed clocks to transmit data. The serializer is also referred to as parallel in serial out (PISO). The high-speed clock is fed to the local clock generation buffer. The local clock generation buffers divide the high-speed clock on the transmitter to a desired frequency on a per-channel basis. Figure 2–3 is a block diagram of the transmitter clocks.

Figure 2–3. Clock Distribution for the Transmitters Note (1)



Note to Figure 2–3:
(1) The global clock line must be driven by an input pin.

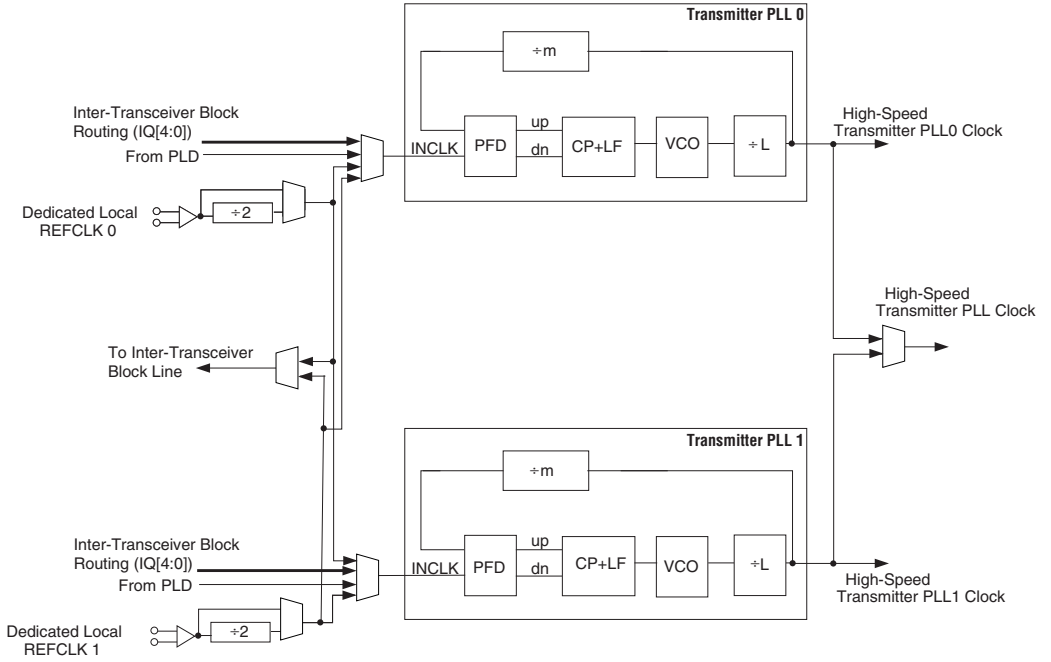
The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. Figure 2–4 is a block diagram of the transmitter PLL.

The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, `REFCLK0` and `REFCLK1`, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines `IQ[4..0]` or from the global clock line that is driven by an input pin.

Figure 2–4. Transmitter PLL Block Note (1)



Note to Figure 2–4:
(1) The global clock line must be driven by an input pin.

The transmitter PLLs support data rates up to 6.375 Gbps. The input clock frequency is limited to 622.08 MHz. An optional `pll_locked` port is available to indicate whether the transmitter PLL is locked to the reference clock. Both transmitter PLLs have a programmable loop bandwidth parameter that can be set to low, medium, or high. The loop bandwidth parameter can be statically set in the Quartus II software.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	50 MHz to 622.08 MHz
Data rate support	600 Mbps to 6.375 Gbps
Multiplication factor (W)	1, 4, 5, 8, 10, 16, 20, 25
Bandwidth	Low, medium, or high

Transmitter Phase Compensation FIFO Buffer

The transmitter phase compensation FIFO buffer resides in the transceiver block at the PCS/FPGA boundary and cannot be bypassed. This FIFO buffer compensates for phase differences between the transmitter PLL clock and the clock from the PLD. After the transmitter PLL has locked to the frequency and phase of the reference clock, the transmitter FIFO buffer must be reset to initialize the read and write pointers. After FIFO pointer initialization, the PLL must remain phase locked to the reference clock.

Byte Serializer

The FPGA and transceiver block must maintain the same throughput. If the FPGA interface cannot meet the timing margin to support the throughput of the transceiver, the byte serializer is used on the transmitter and the byte deserializer is used on the receiver.

The byte serializer takes words from the FPGA interface and converts them into smaller words for use in the transceiver. The transmit data path after the byte serializer is 8, 10, 16, or 20 bits. Refer to Table 2–3 for the transmitter data with the byte serializer enabled. The byte serializer can be bypassed when the data width is 8, 10, 16, or 20 bits at the FPGA interface.

Table 2–3. Transmitter Data with the Byte Serializer Enabled

Input Data Width	Output Data Width
16 bits	8 bits
20 bits	10 bits
32 bits	16 bits
40 bits	20 bits

If the byte serializer is disabled, the FPGA transmit data is passed without data width conversion.

Table 2–4 shows the data path configurations for the Stratix II GX device in single-width and double-width modes.

Refer to the section "8B/10B Encoder" on page 2–8 for a description of the single- and double-width modes.

Table 2–4. Data Path Configurations *Note (1)*

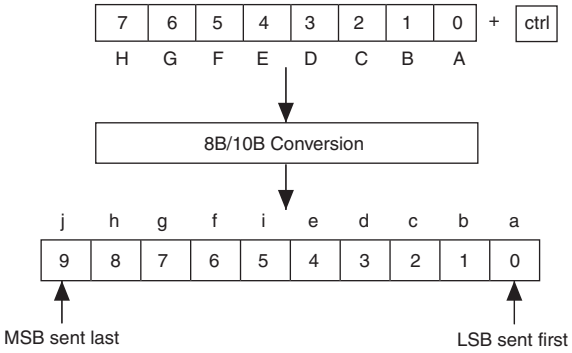
Parameter	Single-Width Mode		Double-Width Mode	
	Without Byte Serialization/ Deserialization	With Byte Serialization/ Deserialization	Without Byte Serialization/ Deserialization	With Byte Serialization/ Deserialization
Fabric to PCS data path width (bits)	8 or 10	16 or 20	16 or 20	32 or 40
Data rate range (Gbps)	0.6 to 2.5	0.6 to 3.125	1 to 5.0	1 to 6.375
PCS to PMA data path width (bits)	8 or 10	8 or 10	16 or 20	16 or 20
Byte ordering *(1)*		✓		✓
Data symbol A (MSB)				✓
Data symbol B		✓		✓
Data symbol C			✓	✓
Data symbol D (LSB)	✓	✓	✓	✓

Note to Table 2–4:
(1) Designs can use byte ordering when byte serialization and deserialization are used.

8B/10B Encoder

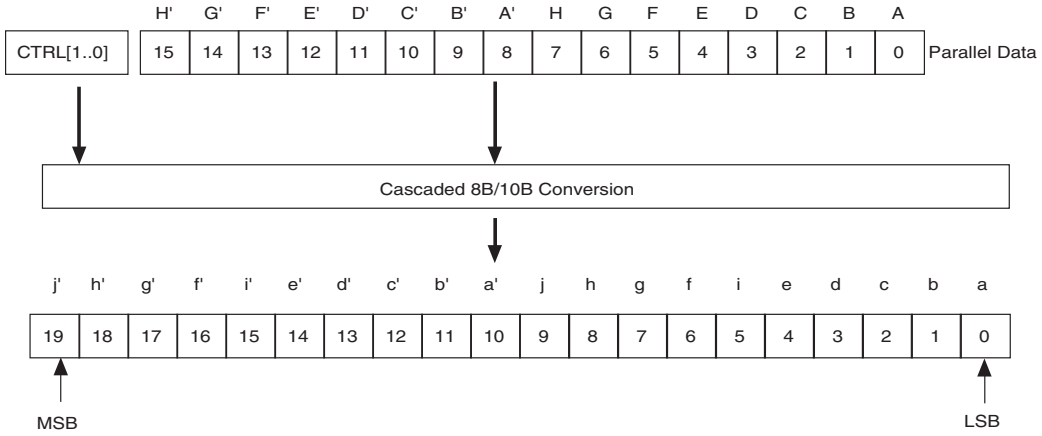
There are two different modes of operation for 8B/10B encoding. Single-width (8-bit) mode supports natural data rates from 622 Mbps to 3.125 Gbps. Double-width (16-bit cascaded) mode supports data rates above 3.125 Gbps. The encoded data has a maximum run length of five. The 8B/10B encoder can be bypassed. Figure 2–5 diagrams the 10-bit encoding process.

Figure 2–5. 8B/10B Encoding Process



In single-width mode, the 8B/10B encoder generates a 10-bit code group from the 8-bit data and 1-bit control identifier. In double-width mode, there are two 8B/10B encoders that are cascaded together and generate a 20-bit (2 × 10-bit) code group from the 16-bit (2 × 8-bit) data + 2-bit (2 × 1-bit) control identifier. Figure 2–6 shows the 20-bit encoding process. The 8B/10B encoder conforms to the IEEE 802.3 1998 edition standards.

Figure 2–6. 16-Bit to 20-Bit Encoding Process



Upon power on or reset, the 8B/10B encoder has a negative disparity which chooses the 10-bit code from the RD-column. However, the running disparity can be changed via the `tx_forcedisp` and `tx_dispval` ports.

Transmit State Machine

The transmit state machine operates in either PCI Express mode, XAUI mode, or GIGE mode, depending on the protocol used. The state machine is not utilized for certain protocols, such as SONET.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–5 shows the code conversion.

Table 2–5. Code Conversion

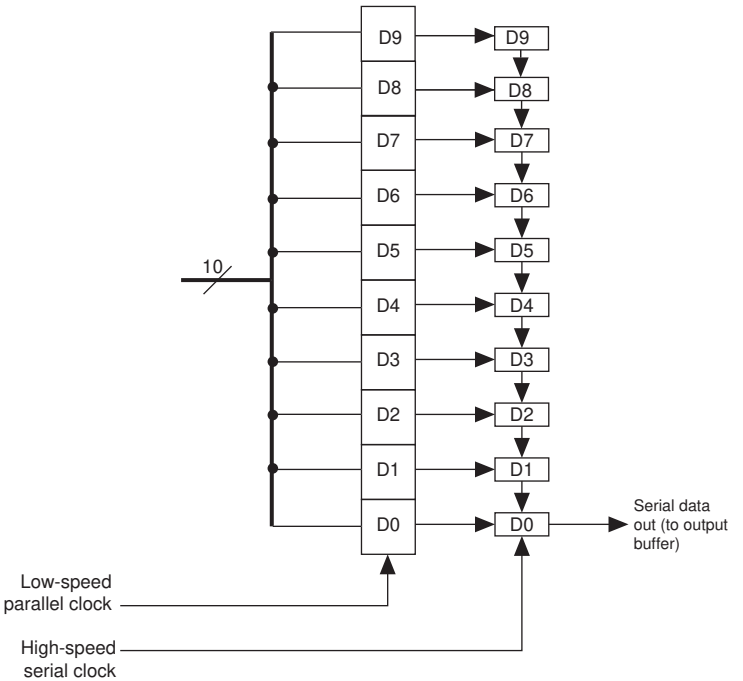
XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $x^7 + x^6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is done automatically by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8, 10, 16, or 20-bit data into a serial data bit stream, transmitting the least significant bit (LSB) first. The serialized data stream is then fed to the high-speed differential transmit buffer. Figure 2–7 is a diagram of the serializer.

Figure 2–7. Serializer *Note (1)*



Note to Figure 2–7:
(1) This is a 10-bit serializer. The serializer can also convert 8, 16, and 20 bits of data.

Transmit Buffer

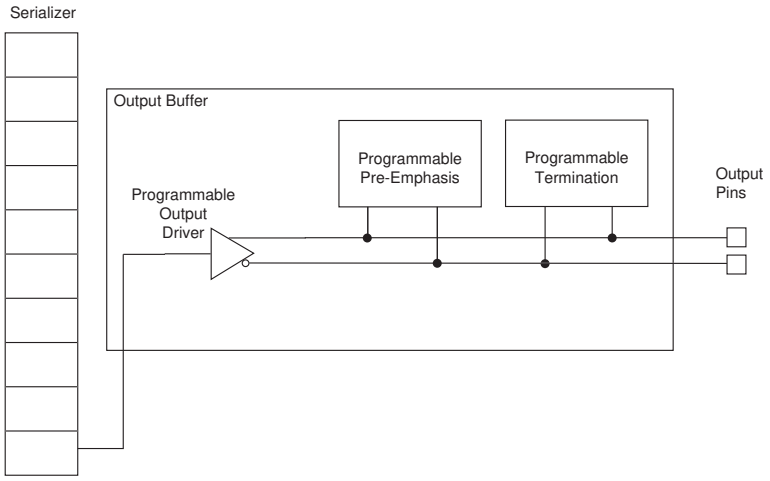
The Stratix II GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage (V_{CM}) of the output driver is programmable. The following V_{CM} values are available when the buffer is in 1.2- and 1.5-V PCML.

- V_{CM} = 0.6 V
- V_{CM} = 0.7 V

Refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Handbook*.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, a programmable termination, and a programmable V_{CM}.

Figure 2–8. Output Buffer



Programmable Output Driver

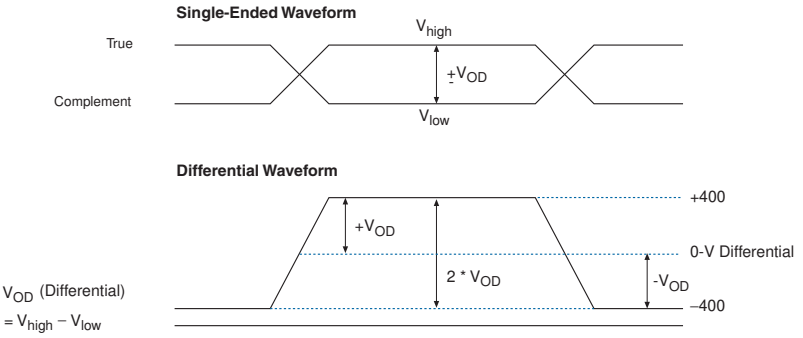
The programmable output driver can be set to drive out differentially 200 to 1,400 mV. The differential output voltage (V_{OD}) can be changed dynamically, or statically set by using the ALT2GXB megafunction or through I/O pins.

The output driver may be programmed with four different differential termination values:

- 100 Ω
- 120 Ω
- 150 Ω
- External termination

Differential signaling conventions are shown in Figure 2–9. The differential amplitude represents the value of the voltage between the true and complement signals. Peak-to-peak differential voltage is defined as $2 \times (V_{HIGH} - V_{LOW}) = 2 \times$ single-ended voltage swing. The common mode voltage is the average of V_{high} and V_{low}.

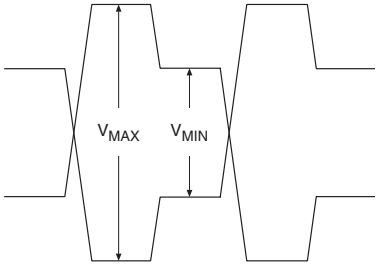
Figure 2–9. Differential Signaling



Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost the high frequency components, and compensate for losses in the transmission medium, as shown in Figure 2–10. The pre-emphasis is set statically using the ALT2GXB megafunction or dynamically through the dynamic reconfiguration controller.

Figure 2–10. Pre-Emphasis Signaling



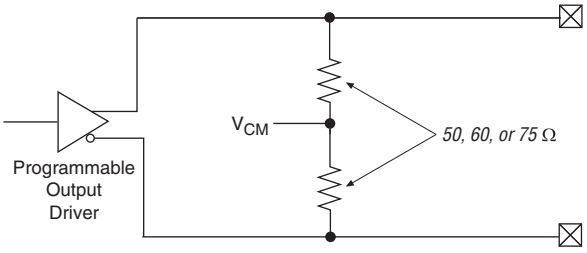
$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1\right) \times 100$$

Pre-emphasis percentage is defined as ($V_{MAX}/V_{MIN} - 1$) × 100, where V_{MAX} is the differential emphasized voltage (peak-to-peak) and V_{MIN} is the differential steady-state voltage (peak-to-peak).

Programmable Termination

The programmable termination can be statically set in the Quartus II software. The values are 100 Ω, 120 Ω, 150 Ω, and external termination. Figure 2–11 shows the setup for programmable termination.

Figure 2–11. Programmable Transmitter Terminations



PCI Express Receiver Detect

The Stratix II GX transmitter buffer has a built-in receiver detection circuit for use in PIPE mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires the transmitter buffer to be tri-stated (in electrical idle mode).

PCI Express Electric Idles (or Individual Transmitter Tri-State)

The Stratix II GX transmitter buffer supports PCI Express electrical idles. This feature is only active in PIPE mode. The `tx_forceelecidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express power-down modes and has specific usage in each mode.

Receiver Path

This section describes the data path through the Stratix II GX receiver. The Stratix II GX receiver consists of the following blocks:

- Receiver differential input buffer
- Receiver PLL lock detector, signal detector, and run length checker
- Clock/data recovery (CRU) unit
- Deserializer
- Pattern detector
- Word aligner

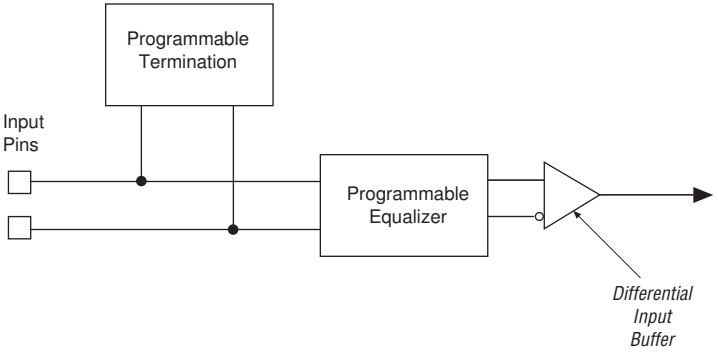
- Lane deskew
- Rate matcher
- 8B/10B decoder
- Byte deserializer
- Byte ordering
- Receiver phase compensation FIFO buffer

Receiver Input Buffer

The Stratix II GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and the 1.2 V common mode voltage for DC-coupled LVDS links.

The receiver has programmable on-chip 100-, 120-, or 150-Ω differential termination for different protocols, as shown in Figure 2–12. The receiver's internal termination can be disabled if external terminations and biasing are provided. The receiver and transmitter differential termination resistances can be set independently of each other.

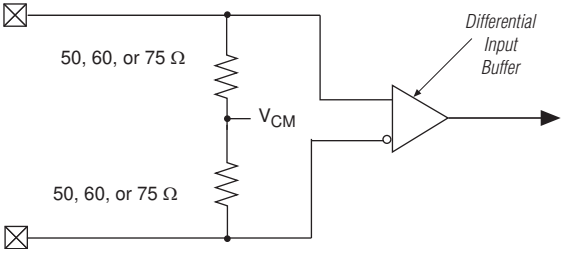
Figure 2–12. Receiver Input Buffer



Programmable Termination

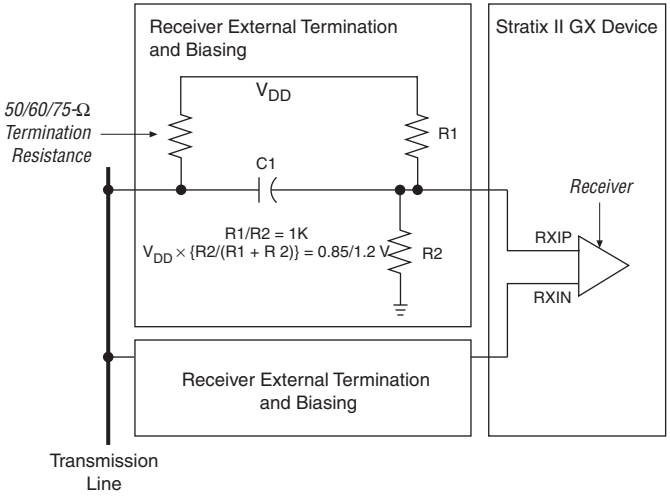
The programmable termination can be statically set in the Quartus II software. Figure 2–13 shows the setup for programmable receiver termination. The termination can be disabled if external termination is provided.

Figure 2–13. Programmable Receiver Termination



If a design uses external termination, the receiver must be externally terminated and biased to 0.85 V or 1.2 V. Figure 2–14 shows an example of an external termination and biasing circuit.

Figure 2–14. External Termination and Biasing Circuit



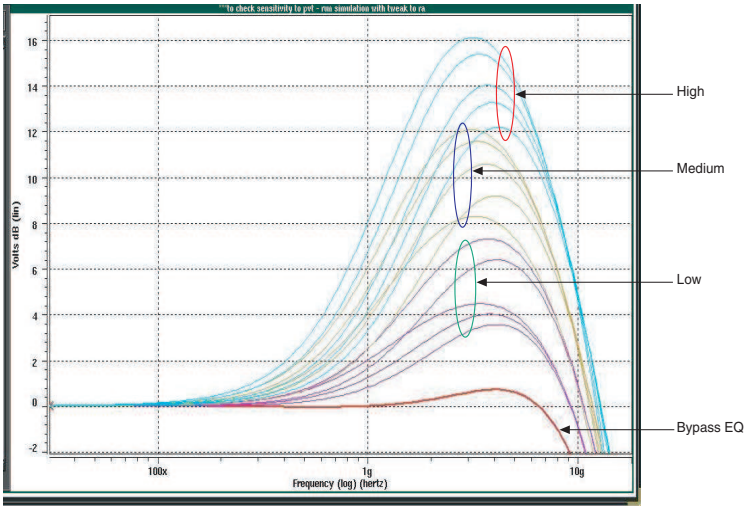
Programmable Equalizer

The Stratix II GX receivers provide a programmable receive equalization feature to compensate the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. The impedance mismatch boundaries can also cause signal degradation. The equalization in the receiver diminishes the lossy attenuation effects of the PCB at high frequencies.

The Stratix II GX receivers also have adaptive equalization capability that adjusts the equalization levels to compensate for changing link characteristics. The adaptive equalization can be powered down dynamically after it selects the appropriate equalization levels.

The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. Figure 2–15 shows the frequency response for the 16 programmable settings allowed by the Quartus II software for Stratix II GX devices.

Figure 2–15. Frequency Response



Receiver PLL and CRU

Each transceiver block has four receiver PLLs, lock detectors, signal detectors, run length checkers, and CRU units, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, the receiver PLL and CRU are powered down for the channel. Figure 2–16 shows the receiver PLL and CRU circuits.