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Stratix III Device Handbook, Volume 2

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Chapter Revision Dates

The chapter in this book was revised on the following date. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1 Stratix III Device Datasheet: DC and Switching Characteristics
Revised: *July 2010*
Part Number: *SIII52001-2.3*

This handbook provides comprehensive information about the Altera® Stratix® III family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, see the following table.

Contact *(Note 1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions that this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, file names, file name extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
“Subheading Title”	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”

Visual Cue	Meaning
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
WARNING	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. DC & Switching Characteristics of Stratix III Devices

When Stratix® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix III devices, system designers must consider the operating requirements discussed in the following chapter:

- Chapter 1, Stratix III Device Datasheet: DC and Switching Characteristics

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. Stratix III Device Datasheet: DC and Switching Characteristics

SIII52001-2.3

Electrical Characteristics

This chapter describes the electrical characteristics, switching characteristics, and I/O timing for Stratix® III devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include core performance specifications and periphery performance. A glossary is also included for your reference.

Operating Conditions

When Stratix III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix III devices, system designers must consider the operating requirements described in this chapter.

Stratix III devices are offered in both commercial and industrial grades. Commercial devices are offered in –2 (fastest), –3, –4, and –4L speed grades. Industrial devices are offered only in –3, –4, and –4L speed grades.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a "C" prefix and industrial with an "I" prefix. For example, commercial devices are indicated as C2, C3, C4, and C4L per respective speed grades. Industrial devices are indicated as I3, I4, and I4L.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods may have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Stratix III Devices *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
V_{CCL}	Selectable core voltage power supply	-0.5	1.65	V
V_{CC}	I/O registers power supply	-0.5	1.65	V
V_{CCD_PLL}	Phase-locked loop (PLL) digital power supply	-0.5	1.65	V
V_{CCA_PLL}	PLL analog power supply	-0.5	3.75	V
V_{CCPT}	Programmable power technology power supply	-0.5	3.75	V
V_{CCPGM}	Configuration pins power supply	-0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V_{CCIO}	I/O power supply	-0.5	3.9	V

Table 1–1. Absolute Maximum Ratings for Stratix III Devices *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
V_{CC_CLKIN}	Differential clock input power supply (top and bottom I/O banks only)	-0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_I	DC Input voltage	-0.5	4.0	V
T_J	Operating junction temperature	-55	125	°C
I_{OUT}	DC output current, per pin	-25	40	mA
T_{STG}	Storage temperature (No bias)	-65	150	°C

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not the power supply.

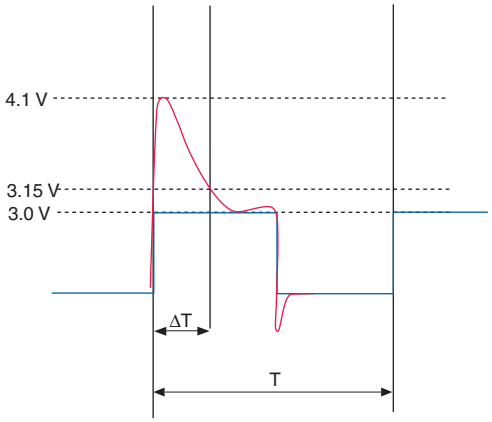
Sinusoidal Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 1–2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 15.8% over the lifetime of the device; for a device lifetime of 10 years, this is equivalent to 15.8% of ten years which is 18.96 months. Figure 1–1 shows how to determine the overshoot duration.

Figure 1–1. Overshoot Duration



In the example shown in Figure 1–1, the overshoot voltage is shown in red and is present at the Stratix III pin, up to 4.1 V. From Table 1–2, for an overshoot of up to 4.1 V, the percentage of high time for overshoot > 3.15 V can be as high as 46% over an 11.4-year period. The percentage of high time is calculated as (delta T/T) * 100. This 11.4-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations where the device is in an idle state, lifetimes are increased.

Table 1–2. Maximum Allowed Overshoot During Transitions

Symbol	Parameter	Condition	Overshoot Duration as a % of High Time	Unit
Vi (AC)	AC Input Voltage *(1)*	4	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%
		4.65	0.130	%
		4.7	0.074	%
		4.75	0.043	%
		4.8	0.025	%
		4.85	0.015	%

Note to Table 1–2:

(1) This input voltage is regardless of the V_{CCIO} supply which is used to power up the input buffer.

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Stratix III devices. Table 1–3 lists the steady-state voltage and current values expected from Stratix III devices. All supplies are required to monotonically reach their full-rail values within t_{RAMP}.

Table 1–3. Recommended Operating Conditions for Stratix III Devices (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCL}	Selectable core voltage power supply for internal logic and input buffers	—	1.05	1.1	1.15	V
	Selectable core voltage power supply for internal logic and input buffers	—	0.86	0.9	0.94	V
V_{CC}	I/O registers power supply	—	1.05	1.1	1.15	V
V_{CCD_PLL}	PLL digital power supply	—	1.05	1.1	1.15	V
V_{CCA_PLL}	PLL analog power supply	—	2.375	2.5	2.625	V
V_{CCPT}	Power supply for the programmable power technology	—	2.375	2.5	2.625	V

Table 1–3. Recommended Operating Conditions for Stratix III Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCPGM}	Configuration pins power supply, 3.3 V	—	3.135	3.3	3.465	V
	Configuration pins power supply, 3.0 V	—	2.85	3	3.15	V
	Configuration pins power supply, 2.5 V	—	2.375	2.5	2.625	V
	Configuration pins power supply, 1.8 V	—	1.71	1.8	1.89	V
V_{CCPD} *(1)*	I/O pre-driver power supply, 3.3 V	—	3.135	3.3	3.465	V
	I/O pre-driver power supply, 3.0 V	—	2.85	3	3.15	V
	I/O pre-driver power supply, 2.5 V	—	2.375	2.5	2.625	V
V_{CCIO}	I/O power supply, 3.3 V	—	3.135	3.3	3.465	V
	I/O power supply, 3.0 V	—	2.85	3	3.15	V
	I/O power supply, 2.5 V	—	2.375	2.5	2.625	V
	I/O power supply, 1.8 V	—	1.71	1.8	1.89	V
	I/O power supply, 1.5 V	—	1.425	1.5	1.575	V
	I/O power supply, 1.2 V	—	1.14	1.2	1.26	V
V_{CC_CLKIN}	Differential clock input power supply (top and bottom I/O banks only)	—	2.375	2.5	2.625	V
V_{CCBAT} *(3)*	Battery back-up power supply for design security volatile key register	—	1.0	—	3.3	V
V_I	DC Input voltage	—	-0.3	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use *(2)*	-40	—	100	°C
t_{RAMP}	Power Supply Ramptime (For V_{CCPT})	Normal POR (PORSEL=0)	50 µs	—	5 ms	—
		Fast POR (PORSEL=1)	50 µs	—	5 ms	—
	Power Supply Ramptime (For all power supplies except V_{CCPT})	Normal POR (PORSEL=0)	50 µs	—	100 ms	—
		Fast POR (PORSEL=1)	50 µs	—	12 ms	—

Notes to Table 1–3:

(1) V_{CCPD} is 2.5, 3.0, or 3.3 V. For a 3.3-V I/O standard, V_{CCPD} = 3.3 V. For a 3.0-V I/O standard, V_{CCPD} = 3.0 V. For a 2.5-V or lower I/O standard, V_{CCPD} = 2.5 V.

(2) For the EP3SL340, EP3SE260, and EP3SL200 devices in the I4L ordering code, the industrial junction temperature range is from 0° C to 100° C, regardless of supply voltage.

(3) Altera recommends a 3.0-V nominal battery voltage when connecting V_{CCBAT} to a battery for volatile key backup. If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.

DC Characteristics

This section lists the input pin capacitances, on-chip termination tolerance, and hot- socketing specifications.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–4 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM}. Use the EPE to get supply current estimates for the remaining power supplies.

Table 1–4. Supply Current Specifications for V_{CC_CLKIN} and V_{CCPGM}

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	250	mA
I_{PGM}	V_{CCPGM} current specifications	0	250	mA

I/O Pin Leakage Current

Table 1–5 lists Stratix III I/O pin leakage current specifications.

Table 1–5. I/O Pin Leakage Current for Stratix III Devices *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	-10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	-10	—	10	µA

Notes to Table 1–5:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10-µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold Specifications

Table 1–6 lists the Stratix III device family bus hold specifications.

Table 1–6. Bus Hold Parameters for Stratix III Devices (Part 1 of 2)

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V/3.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA

Table 1–6. Bus Hold Parameters for Stratix III Devices (Part 2 of 2)

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V/3.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	—	-160	—	-200	—	-300	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for the I/Os connected to the calibration block. Table 1–7 lists the Stratix III OCT calibration block accuracy specifications.

Table 1–7. On-Chip Termination Calibration Accuracy Specifications for Stratix III Devices *(Note 1)*

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3, I3	C4, I4	
25-Ω R_S *(2)* 3.3, 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V	±8	±8	±8	%
50-Ω R_S 3.3, 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V	±8	±8	±8	%
50-Ω R_T 2.5, 1.8, 1.5, 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	±10	±10	±10	%
20-Ω R_S to 60-Ω R_S 3.3, 3.0, 2.5, 1.8, 1.5, 1.2	Expanded range for internal series termination with calibration (Between 20-Ω to 60-Ω setting)	V_{CCIO} = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V *(3)*	±10	±10	±10	%
25-Ω $R_{S_left_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S_left_shift}$ setting)	V_{CCIO} = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V	±10	±10	±10	%
R_{OCT_CAL}	Internal series termination with calibration	*(4)*				

Notes to Table 1–7:

(1) OCT calibration accuracy is valid at the time of calibration only.

(2) 25-Ω R_S not supported for 1.5 V and 1.2 V in Row I/O.

(3) 1.5 V and 1.2 V only supports 40-Ω to 60-Ω expanded range.

(4) For resistance tolerance after power-up calibration, refer to Equation 1–1 and Table 1–9 on page 1–8.

The accuracy listed in Table 1–7 is valid at the time of calibration. If the voltage or temperature changes, the termination resistance value varies. Table 1–8 lists the resistance tolerance for Stratix III OCT.

Table 1–8. On-Chip Termination Resistance Tolerance Specification for Stratix III Devices

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3, I3	C4, I4	
R_{OCT_UNCAL}	Internal series termination without calibration	—				
25-Ω R_S 3.3, 3.0, 2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3, 3.0, 2.5 V	±30	±40	±40	%
25-Ω R_S 1.8, 1.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8, 1.5 V	±30	±50	±50	%
25-Ω R_S 1.2	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±35	±60	±60	%
50-Ω R_S 3.3, 3.0, 2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3, 3.0, 2.5 V	±30	±40	±40	%
50-Ω R_S 1.8, 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5 V	±30	±50	±50	%
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±35	±60	±60	%
R_D	Internal differential termination for LVDS technology (100-Ω setting)	V_{CCIO} = 2.5 V	-15 to 35			%

Table 1–9 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–9 and Equation 1–1 to determine OCT variation without re-calibration.

Equation 1–1. OCT Variation Without Re-Calibration *(Note 1)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1–1:

(1) R_{OCT} value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1–9. On-Chip Termination Variation after Power-up Calibration *(Note 1)*

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3	0.029	%/mV
		2.5	0.036	%/mV
		1.8	0.065	%/mV
		1.5	0.104	%/mV
		1.2	0.177	%/mV
dR/dT	OCT variation with temperature without re-calibration	3	0.294	%/°C
		2.5	0.301	%/°C
		1.8	0.355	%/°C
		1.5	0.344	%/°C
		1.2	0.348	%/°C

Note to Table 1–9:

(1) Valid for V_{CCIO} range of ± 5% and temperature range of 0° to 85° C.

Pin Capacitance

Table 1–10 lists the Stratix III device family pin capacitance.

Table 1–10. Pin Capacitance for Stratix III Device Family

Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	4	pF
C_{IOLR}	Input capacitance on left and right I/O pins	4	pF
C_{CLKTB}	Input capacitance on top and bottom non-dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on left and right non-dedicated clock input pins	4	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Hot-Socketing

Table 1–11 lists the hot-socketing specifications for Stratix III devices.

Table 1–11. Hot-Socketing Specifications for Stratix III Devices

Symbol	Parameter	Maximum
$\|I_{IOPIN}\|$(DC)	DC current per I/O pin	300 μA
$\|I_{IOPIN}\|$(AC)	AC current per I/O pin	8 mA *(1)*

Note to Table 1–11:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 1–12 lists the weak pull-up resistor values for Stratix III devices.

Table 1–12. Internal Weak Pull-Up Resistor for Stratix III Devices *(Note 1)*, *(3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled	V_{CCIO} = 3.3 V ± 5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 3.0 V ± 5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 2.5 V ± 5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 1.8 V ± 5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 1.5 V ± 5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 1.2 V ± 5% *(2)*	—	25	—	kΩ

Notes to Table 1–12:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25k Ω.

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltages (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for all I/O standards supported by Stratix III devices. V_{OL} and V_{OH} values are valid at the corresponding I_{OL} and I_{OH}, respectively.

Table 1–13 through Table 1–18 list the Stratix III device family I/O standard specifications. Refer to "Glossary" on page 1–326 for an explanation of terms used in the Table 1–14 through Table 1–18.

Table 1–13. Single-Ended I/O Standards Specifications

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	IOL (mA)	IOH (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.3-V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	V_{CCIO} - 0.2	0.1	-0.1
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V_{CCIO} - 0.2	0.1	-0.1
2.5-V LVTTL/ LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.2	2.1	0.1	-0.1
		2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
		2.5	2.625	-0.3	0.7	1.7	3.6	0.7	1.7	2	-2
1.8-V LVTTL / LVCMOS	1.71	1.8	1.89	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} - 0.45	2	-2
1.5-V LVTTL/ LVCMOS	1.425	1.5	1.575	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
1.2-V LVTTL / LVCMOS	1.14	1.2	1.26	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	3.6	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 * V_{CCIO}	0.5 * V_{CCIO}	—	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5

Refer to the figure in "Single-Ended Voltage Referenced I/O Standard" in the "Glossary" on page 1–326 for voltage referenced receiver input waveform and explanation of terms used in Table 1–14.

Table 1–14. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 CLASS I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 CLASS I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 CLASS I, II	1.425	1.5	1.575	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	0.47 * V_{CCIO}	V_{REF}	0.53 * V_{CCIO}
HSTL-18 CLASS I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 CLASS I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 CLASS I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—

Table 1–15. Single-Ended SSTL and HSTL I/O Standards Signal Specifications *(Note 1)* (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	IOL (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 CLASS I	-0.3	V_{REF} - 0.15	V_{REF} +0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	VTT - 0.57	VTT + 0.57	8.1	-8.1
SSTL-2 CLASS II	-0.3	V_{REF} - 0.15	V_{REF} +0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	VTT - 0.76	VTT + 0.76	16.2	-16.2
SSTL-18 CLASS I	-0.3	V_{REF} -0.125	V_{REF} +0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	VTT - 0.475	VTT + 0.475	6.7	-6.7
SSTL-18 CLASS II	-0.3	V_{REF} -0.125	V_{REF} +0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	-13.4
SSTL-15 CLASS I	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	-8
SSTL-15 CLASS II	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	-16
HSTL-18 CLASS I	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-18 CLASS II	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-15 CLASS I	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-15 CLASS II	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-12 CLASS I	-0.15	V_{REF} -0.08	V_{REF} +0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75 * V_{CCIO}	8	-8

Table 1–15. Single-Ended SSTL and HSTL I/O Standards Signal Specifications *(Note 1)* (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	IOL (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-12 CLASS II	-0.15	V_{REF} -0.08	V_{REF} +0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75 * V_{CCIO}	16	-16

Note to Table 1–15:

(1) Use the current strength settings that are equal or larger than the I_{OL} and I_{OH} values listed to meet the V_{OL} and V_{OH} specifications for each line. OCT or lower current strengths may provide better signal integrity and lower power.

Refer to the figures for "Differential I/O Standards" in "Glossary" on page 1–326 for the receiver input and transmitter output waveforms, and for all the differential I/O standards (LVDS, mini-LVDS, RSDS). V_{CC_CLKIN} is the power supply for the differential column clock input pins. V_{CCPD} is the power supply for the row I/Os and all other column I/Os.

Table 1–16. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{SWING\ (DC)}$ (V)		$V_{X\ (AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX\ (AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 CLASS I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 CLASS I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 -0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 -0.125	—	V_{CCIO}/2 +0.125
SSTL-15 CLASS I, II	1.425	1.5	1.575	0.2	—	—	V_{CCIO}/2	—	0.35	—	—	V_{CCIO}/2	—

Table 1–17. Differential HSTL I/O Standards Specifications

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 CLASS I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 CLASS I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 CLASS I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	V_{CCIO} + 0.48

Table 1–18. Differential I/O Standard Specifications (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (Row I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.05 *(6)*	$D_{max} \leq 700$ Mbps	1.8 *(6)*	0.247	—	0.6	1.125	1.25	1.375
	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	1.05 *(6)*	$D_{max} > 700$ Mbps	1.55 *(6)*	0.247	—	0.6	1.125	1.25	1.375

Table 1–18. Differential I/O Standard Specifications (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (Column I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.05 *(6)*	$D_{max} \leq 700$ Mbps	1.8 *(6)*	0.247	—	0.6	1.0	1.25	1.5
	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	1.05 *(6)*	$D_{max} > 700$ Mbps	1.55 *(6)*	0.247	—	0.6	1.0	1.25	1.5
RSDS (Row I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (Column I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (Row I/O)	2.375	2.5	2.625	0.2	—	0.6	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.4
Mini-LVDS (Column I/0)	2.375	2.5	2.625	0.2	—	0.6	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.5
LVPECL *(3)*	2.375 *(5)*	2.5 *(5)*	2.625 *(5)*	0.3	—	—	0.6	$D_{max} \leq 700$ Mbps	1.8 *(4)*	—	—	—	—	—	—
	2.375 *(5)*	2.5 *(5)*	2.625 *(5)*	0.3	—	—	1.0	$D_{max} > 700$ Mbps	1.6 *(4)*	—	—	—	—	—	—

Notes to Table 1–18:

(1) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(2) RL range: $90 \leq RL \leq 110\ \Omega$.

(3) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins. Differential clock inputs in column I/O use V_{CC_CLKIN} that must be powered by 2.5 V. Differential clock inputs in row I/O banks are powered by V_{CCPD}.

(4) The receiver voltage input range for the data rate when $D_{max} > 700$ Mbps is $0.85\ V \leq V_{IN} \leq 1.75\ V$.
The receiver voltage input range for the data rate when $D_{max} \leq 700$ Mbps is $0.45\ V \leq V_{IN} \leq 1.95\ V$.

(5) Power supply for the column I/O LVPECL differential clock input buffer is V_{CC_CLKIN}.

(6) The receiver voltage input range for the data rate when $D_{max} > 700$ Mbps is $1.0\ V \leq V_{IN} \leq 1.6\ V$.
The receiver voltage input range for the data rate when $D_{max} \leq 700$ Mbps is zero $V \leq V_{IN} \leq 1.85\ V$.

Power Consumption

Altera offers two ways to estimate power for a design: the Excel-based Early Power Estimator (EPE) and the Quartus® II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides estimation based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimation.

Refer to Table 1–4 on page 1–5 for supply current estimates for V_{CCPGM} and V_{CC_CLKIN}. Use the EPE and PowerPlay Power Analyzer for current estimates of remaining power supplies.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide For Stratix III FPGAs* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Stratix III core and periphery blocks for commercial grade devices.

These characteristics can be designated as **Preliminary** and **Final** and each designation is defined below.

Preliminary—Preliminary characteristics are created using simulation results, process data, and other known parameters.

Final—Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. The upper-right hand corner of a table shows the designation as **Preliminary** or **Final**.

Core Performance Specifications

These sections describe the Clock Tree, PLL, digital signal processing (DSP), TriMatrix, and Configuration and JTAG specifications.

Clock Tree Specifications

Table 1–19 lists the clock tree performance specifications for the logic array, DSP blocks, and TriMatrix Memory blocks for Stratix III devices.

Table 1–19. Clock Tree Performance for Stratix III Devices

Device	C2	C3, I3	C4, I4	C4L, I4L		Unit
	V_{CCL} = 1.1 V	V_{CCL} = 1.1 V	V_{CCL} = 1.1 V	V_{CCL} = 1.1 V	V_{CCL} = 0.9 V	
EP3SL50	730	700	450	450	375	MHz
EP3SL70	730	700	450	450	375	MHz
EP3SL110	730	700	450	450	375	MHz
EP3SL150	730	700	450	450	375	MHz
EP3SL200	730	700	450	450	375	MHz
EP3SE260	730	700	450	450	375	MHz
EP3SL340	730	700	450	450	375	MHz
EP3SE50	730	700	450	450	375	MHz
EP3SE80	730	700	450	450	375	MHz
EP3SE110	730	700	450	450	375	MHz

PLL Specifications

Table 1–20 lists the Stratix III PLL specifications when operating in both the commercial junction temperature range (0 to 85° C) and the industrial junction temperature range (-40 to 100° C), except for EP3SL340, EP3SE260, and EP3SL200 devices in the I4L ordering code, where the industrial junction temperature range is from 0° C to 100° C, regardless of supply voltage. Refer to the figure in "PLL Specifications" in "Glossary" on page 1–326 for the PLL block diagram.

Table 1–20. PLL Specifications for Stratix III Devices (Part 1 of 3)

Symbol	Parameter	C2			C3, I3			C4, I4			C4L, I4L						Unit
		V_{CCL} = 1.1 V			V_{CCL} = 1.1 V			V_{CCL} = 1.1 V			V_{CCL} = 1.1 V			V_{CCL} = 0.9 V			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{IN}	Input clock frequency	5	—	800 *(1)*	5	—	717 *(1)*	5	—	717 *(1)*	5	—	717 *(1)*	5	—	717 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	5	—	325	5	—	325	5	—	325	5	—	325	MHz
f_{VCO}	PLL VCO operating range	600	—	1600	600	—	1300	600	—	1300	600	—	1300	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	40	—	60	40	—	60	40	—	60	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	600 *(2)*	—	—	500 *(2)*	—	—	450 *(2)*	—	—	450 *(2)*	—	—	375 *(2)*	MHz
f_{OUT_EXT}	Output frequency for dedicated external clock output	—	—	800 *(2)*	—	—	717 *(2)*	—	—	717 *(2)*	—	—	717 *(2)*	—	—	717 *(2)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	—	—	10	—	—	10	—	—	10	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain	—	3.5	—	—	3.5	—	—	3.5	—	—	3.5	—	—	3.5	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	—	1	—	—	1	—	—	1	—	—	1	—	scanclk cycles
$f_{SCANCLK}$	`scanclk` frequency	—	—	100	—	—	100	—	—	100	—	—	100	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

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Table 1–20. PLL Specifications for Stratix III Devices (Part 2 of 3)

Symbol	Parameter	C2			C3, I3			C4, I4			C4L, I4L						Unit
		V_{CCL} = 1.1 V			V_{CCL} = 1.1 V			V_{CCL} = 1.1 V			V_{CCL} = 1.1 V			V_{CCL} = 0.9 V			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	—	0.3	—	—	0.3	—	—	0.3	—	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	—	1.5	—	—	1.5	—	—	1.5	—	—	1.5	—	MHz
	PLL closed-loop high bandwidth *(6)*	—	4	—	—	4	—	—	4	—	—	4	—	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	—	—	±50	—	—	±50	—	—	±50	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal	10	—	—	10	—	—	10	—	—	10	—	—	10	—	—	ns
t_{INCCJ} *(3)*, *(4)*	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	—	—	0.15	—	—	0.15	—	—	0.15	—	—	0.1	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	—	—	±750	—	—	±750	—	—	±750	—	—	±500	ps (p-p)
t_{OUTPJ_DC} *(5)*	Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	—	—	175	—	—	175	—	—	175	—	—	225	ps (p-p)
	Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	—	—	17.5	—	—	17.5	—	—	17.5	—	—	22.5	mUI (p-p)
t_{OUTCCJ_DC} *(5)*	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	—	—	175	—	—	175	—	—	175	—	—	225	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	—	—	17.5	—	—	17.5	—	—	17.5	—	—	22.5	mUI (p-p)
t_{OUTPJ_IO} *(5)*, *(8)*	Period Jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz)	—	—	600	—	—	600	—	—	600	—	—	600	—	—	750	ps (p-p)
	Period Jitter for clock output on regular IO ($F_{OUT} < 100$ MHz)	—	—	60	—	—	60	—	—	60	—	—	60	—	—	75	mUI (p-p)