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CIRRUS LOGIC®

FEATURES

- ARM®720T Processor
  - ARM7TDMI CPU operating at speeds of 74 and 90 MHz
  - 8 KBytes of four-way set-associative cache
  - MMU with 64-entry TLB
  - Thumb code support enabled
- Ultra low power
  - 90 mW at 74 MHz typical
  - 108 mW at 90 MHz typical
  - <.03 mW in the Standby State
- Advanced audio decoder/decompression capability
  - Supports bit streams with adaptive bit rates
  - Allows for support of multiple audio decompression algorithms (MP3, WMA, AAC, Audible, etc.)

Plays
Windows
Media™
TM

(cont.)

High-Performance, Low-Power System on Chip with SDRAM and Enhanced Digital Audio Interface

OVERVIEW

The Cirrus Logic™ EP7312 is designed for ultra-low-power portable and line-powered applications such as portable consumer entertainment devices, home and car audio juke box systems, and general purpose industrial control applications, or any device that features the added capability of digital audio compression & decompression. The core-logic functionality of the device is built around an ARM720T processor with 8 KBytes of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720T is an enhanced memory management unit (MMU) which allows for support of sophisticated operating systems like Microsoft® Windows® CE and Linux®.
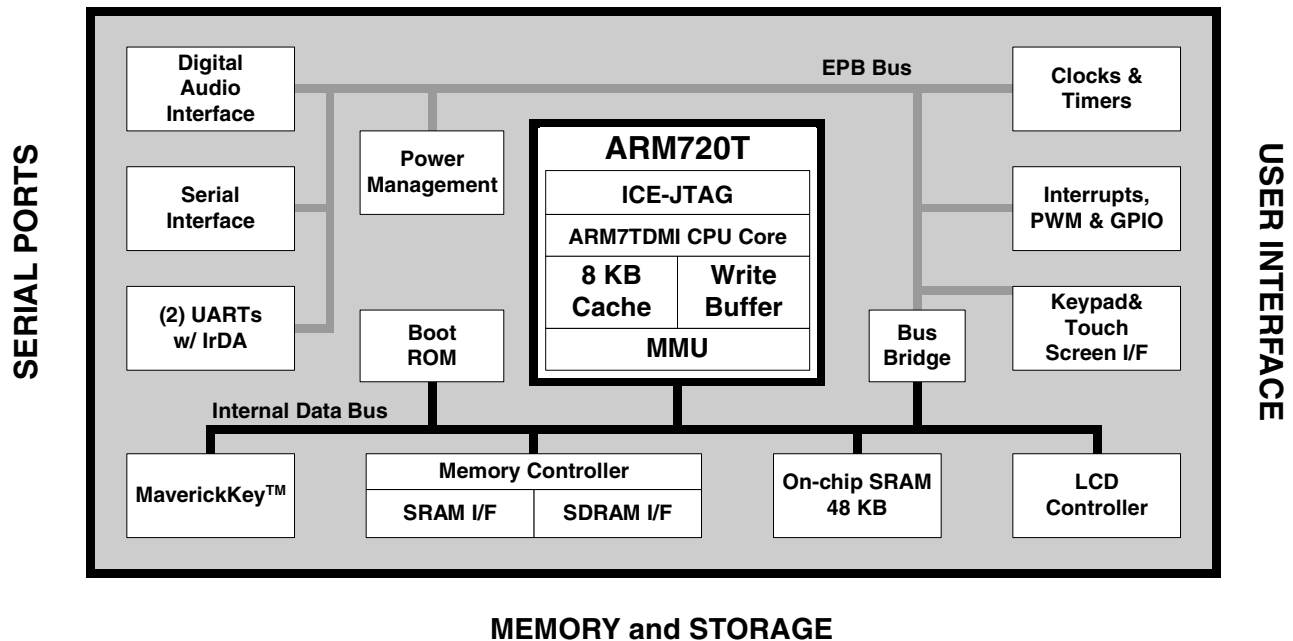
ORDERING INFORMATION:

(cont.)

BLOCK DIAGRAM

MEMORY and STORAGE

CIRRUS LOGIC®

CIRRUS LOGIC®

FEATURES *(cont)*

- 48 KBytes of on-chip SRAM
- MaverickKey™ IDs
  - 32-bit unique ID can be used for DRM compliance 128-bit random ID
- Available in 74 and 90 MHz clock speeds
- LCD controller
  - Interfaces directly to a single-scan panel monochrome STN LCD
  - Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - 32-bit SDRAM Interface up to 2 external banks
  - 8/32/16-bit SRAM/FLASH/ROM Interface
  - Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - Two Synchronous Serial Interfaces (SSI1, SSI2)
  - CODEC Sound Interface
  - 8×8 Keypad Scanner

- — 27 General Purpose Input/Output pins
- — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - Two 16550 compatible UARTs
  - IrDA Interface
  - Two PWM Interfaces
  - Real-time Clock
  - Two general purpose 16-bit timers
  - Interrupt Controller
  - Boot ROM
- Package
  - 208-Pin LQFP
  - 256-Ball PBGA
  - 204-Ball TFBGA
- The fully static EP7312 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

OVERVIEW *(cont.)*

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, high quality ADCs, DACs, or CODECs such as the Cirrus Logic CS53L32A, CS43L42, and CS42L50 are easily added to an EP73xx design via the DAI. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

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Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:

http://www.cirrus.com/corporate/contacts/sales.cfm

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Description of the EP7312's Components, Functionality, and Interfaces

The following sections describe the EP7312 in more detail.

Processor Core - ARM720T

The EP7312 incorporates an ARM 32-bit RISC micro controller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Table 1 shows the power management pin assignments.

Table 1. Power Management Pin Assignments

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density. shows the Static Memory Interface pin assignments.

Table 2. Static Memory Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7312 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State. Table 3 shows the SDRAM Interface pin assignments.

Table 3. SDRAM Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SDCLK	O	SDRAM clock output
SDCKE	O	SDRAM clock enable output
nSDCS[1:0]	O	SDRAM chip select out
WRITE/nSDRAS (Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS (Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE (Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12] (Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]	O	SDRAM internal bank select
PD[7:6]/SDQM[1:0] (Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]	O	SDRAM byte lane mask
D[31:0]	I/O	Data I/O

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27]/DRA[0], A[26]/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table 19 on page 11 for more information.

Digital Audio Capability

The EP7312 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7312

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7312 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to

drive an infrared communication interface directly. Table 4 shows the UART pin assignments.

Table 4. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Digital Audio Interface (DAI)

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal CS43L41/42/43 low-power audio DACs and the Crystal CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions. Table 5 shows the DAI Interface pin assignments.

Table 5. DAI Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SCLK	O	Serial bit clock
SDOUT	O	Serial data out
SDIN	I	Serial data in
LRCK	O	Sample clock
MCLKIN	I	Master clock input
MCLKOUT	O	Master clock output

Note: See Table 18 on page 11 for information on pin multiplexes.

CODEC Interface

The EP7312 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the DAI and SSI2. Table 6 shows the CODEC Interface Pin Assignments.

Table 6. CODEC Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

> *Note: See Table 18 on page 11 for information on pin multiplexes.*

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the DAI and CODEC interfaces through a multiplexer. The SSI2 Interface has these features:

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Table 7 shows the SSI2 Interface pin assignments.

Table 7. SSI2 Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

> *Note: See Table 18 on page 11 for information on pin multiplexes.*

Synchronous Serial Interface

The EP7312 Synchronous Serial Interface has these features:

- ADC (SSI) Interface: Master mode only; SPI and Microwire1-compatible (128 kbps operation)
- Selectable serial clock polarity

Table 8 shows the Synchronous Serial Interface pin assignments.

Table 8. Serial Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
ADCLK	O	SSI1 ADC serial clock
ADCIN	I	SSI1 ADC serial input
ADCOUT	O	SSI1 ADC serial output
nADCCS	O	SSI1 ADC chip select
SMPCLK	O	SSI1 ADC sample clock

LCD Controller

A DMA address generator is provided that fetches video display data for the LCD controller from memory. The display frame buffer start address is programmable, allowing the LCD frame buffer to be in SDRAM, internal SRAM or external SRAM. The LCD controller has these features:

- Interfaces directly to a single-scan panel monochrome STN LCD
- Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits

Table 9 shows the LCD Interface pin assignments.

Table 9. LCD Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
CL1	O	LCD line clock
CL2	O	LCD pixel clock out
DD[3:0]	O	LCD serial display data bus
FRM	O	LCD frame synchronization pulse
M	O	LCD AC bias drive

64-Key Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7312. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state. The Keypad Interface has these features:

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Table 10 shows the Keypad Interface Pin Assignments.

Table 10. Keypad Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7312 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources. The Interrupt controller has these features:

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

Table 11 shows the interrupt controller pin assignments.

.

Table 11. Interrupt Controller Pin Assignments

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Real-Time Clock

The EP7312 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Table 12 shows the Real-Time Clock pin assignments.

Table 12. Real-Time Clock Pin Assignments

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

PLL and Clocking

The EP7312 processor and peripheral clocks have these features:

- Processor and peripheral clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz, and at 45 MHz when the processor is set to 90 MHz.

Table 13 shows the PLL and clocking pin assignments.

Table 13. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

DC-to-DC Converter Interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Table 14 shows the DC-to-DC Converter Interface pin assignments.

Table 14. DC-to-DC Converter Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Table 15 shows the GPIO pin assignments.

Table 15. General Purpose Input/Output Pin Assignments

Pin Mnemonic	I/O	Pin Description
PA[7:0]	I	GPIO port A
PB[7:0]	I	GPIO port B
PD[0]/LEDFLSH (Note)	I/O	GPIO port D
PD[5:1]	I/O	GPIO port D
PD[7:6]/SDQM[1:0] (Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0] (Note)	I	GPIO port E
PE[2]/CLKSEL (Note)	I	GPIO port E

> *Note: Pins are multiplexed. See Table 19 on page 11 for more information.*

Hardware Debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Table 16 shows the Hardware Debug Interface pin assignments.

Table 16. Hardware Debug Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA. Table 17 shows the LED Flasher pin assignments.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Table 17. LED Flasher Pin Assignments

Pin Mnemonic	I/O	Pin Description
PD[0]/LEDFLSH (Note)	O	LED flasher driver

> *Note: Pins are multiplexed. See Table 19 on page 11 for more information.*

Internal Boot ROM

The internal 128-byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7312 is available in a 208-pin LQFP package, 256-ball PBGA package, or a 204-ball TFBGA package.

Pin Multiplexing

Table 18 shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the *EP7312 User's Manual* for more information).

Table 18. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 19 shows the pins that have been multiplexed in the EP7312.

Table 19. Pin Multiplexing

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.
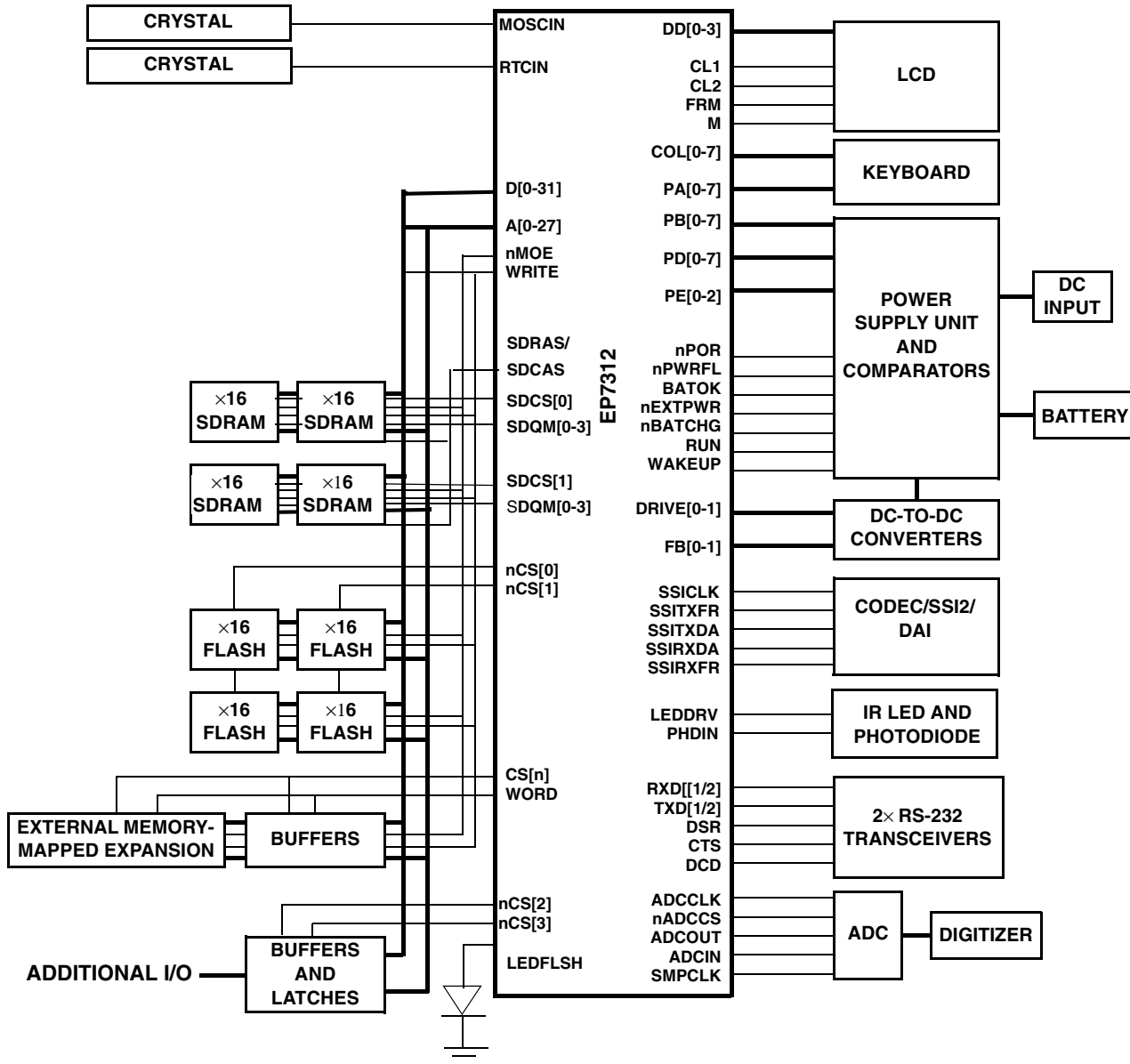

Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	−40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = −0.1 mA IOL = −4 mA IOL = −12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b][c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8	-	10.0	pF	
CI/O	Transceiver capacitance	8	-	10.0	pF	
IDD$_{STANDBY}$ @ 25 C	Standby current consumption Core, Osc, RTC @ 2.5 V	-	77	-	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V$_{DD}$ ± 0.1 V, VIL = GND ± 0.1 V
	I/O @ 3.3 V	-	41	-		
IDD$_{STANDBY}$ @ 70 C	Standby current consumption Core, Osc, RTC @ 2.5 V	-	-	570	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V$_{DD}$ ± 0.1 V, VIL = GND ± 0.1 V
	I/O @ 3.3 V	-	-	111		
IDD$_{STANDBY}$ @ 85 C	Standby current consumption Core, Osc, RTC @ 2.5 V[1]	-	-	1693	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V$_{DD}$ ± 0.1 V, VIL = GND ± 0.1 V
	I/O @ 3.3 V	-	-	163		
IDD$_{idle}$ at 74 MHz	Idle current consumption Core, Osc, RTC @ 2.5 V	-	6	-	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V$_{DD}$ ± 0.1 V, VIL = GND ± 0.1 V
	I/O @ 3.3 V	-	10	-		
IDD$_{IDLE}$ at 90 MHz	Idle current consumption Core, Osc, RTC @ 2.5 V	-	7	-	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V$_{DD}$ ± 0.1 V, VIL = GND ± 0.1 V
	I/O @ 3.3 V	-	11	-		
VDD$_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) *Total power consumption = IDD$_{CORE}$ x 2.5 V + IDD$_{IO}$ x 3.3 V*

2) *A typical design will provide 3.3 V to the I/O supply (i.e., V$_{DDIO}$), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).*

2) *Pull-up current = 50 µA typical at V$_{DD}$ = 3.3 V.*

Timings

Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

Clock

High to Low

High/Low to High

Bus Change

Bus Valid

Undefined/Invalid

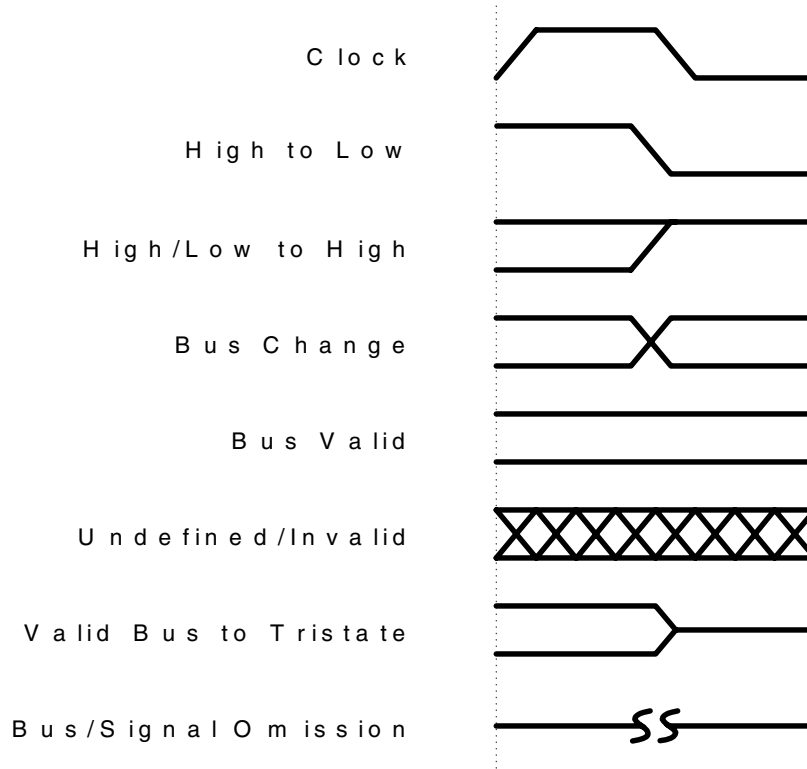Valid Bus to Tristate

Bus/Signal Omission

Figure 2. Legend for Timing Diagrams

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements. All characteristics are specified at V_{DDIO} = 3.1 - 3.5 V and V_{SS} = 0 V over an operating temperature of -40°C to +85°C. Pin loadings is 50 pF. The timing values are referenced to $1/2\ V_{DD}$.

SDRAM Interface

Figure 3 through Figure 6 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK rising edge to SDCS assert delay time	t_{CSa}	0	2	4	ns
SDCLK rising edge to SDCS deassert delay time	t_{CSd}	− 3	2	10	ns
SDCLK rising edge to SDRAS assert delay time	t_{RAa}	1	3	7	ns
SDCLK rising edge to SDRAS deassert delay time	t_{RAd}	− 3	1	10	ns
SDCLK rising edge to SDRAS invalid delay time	t_{RAnv}	2	4	7	ns
SDCLK rising edge to SDCAS assert delay time	t_{CAa}	− 2	2	5	ns
SDCLK rising edge to SDCAS deassert delay time	t_{CAd}	− 5	0	3	ns
SDCLK rising edge to ADDR transition time	t_{ADv}	− 3	1	5	ns
SDCLK rising edge to ADDR invalid delay time	t_{ADx}	− 2	2	5	ns
SDCLK rising edge to SDMWE assert delay time	t_{MWa}	− 2	1	5	ns
SDCLK rising edge to SDMWE deassert delay time	t_{MWd}	− 4	0	4	ns
DATA transition to SDCLK rising edge time	t_{DAs}	-	-	2	ns
SDCLK rising edge to DATA transition hold time	t_{DAh}	-	-	1	ns
SDCLK rising edge to DATA transition delay time	t_{DAd}	0	-	15	ns

SDRAM Load Mode Register Cycle
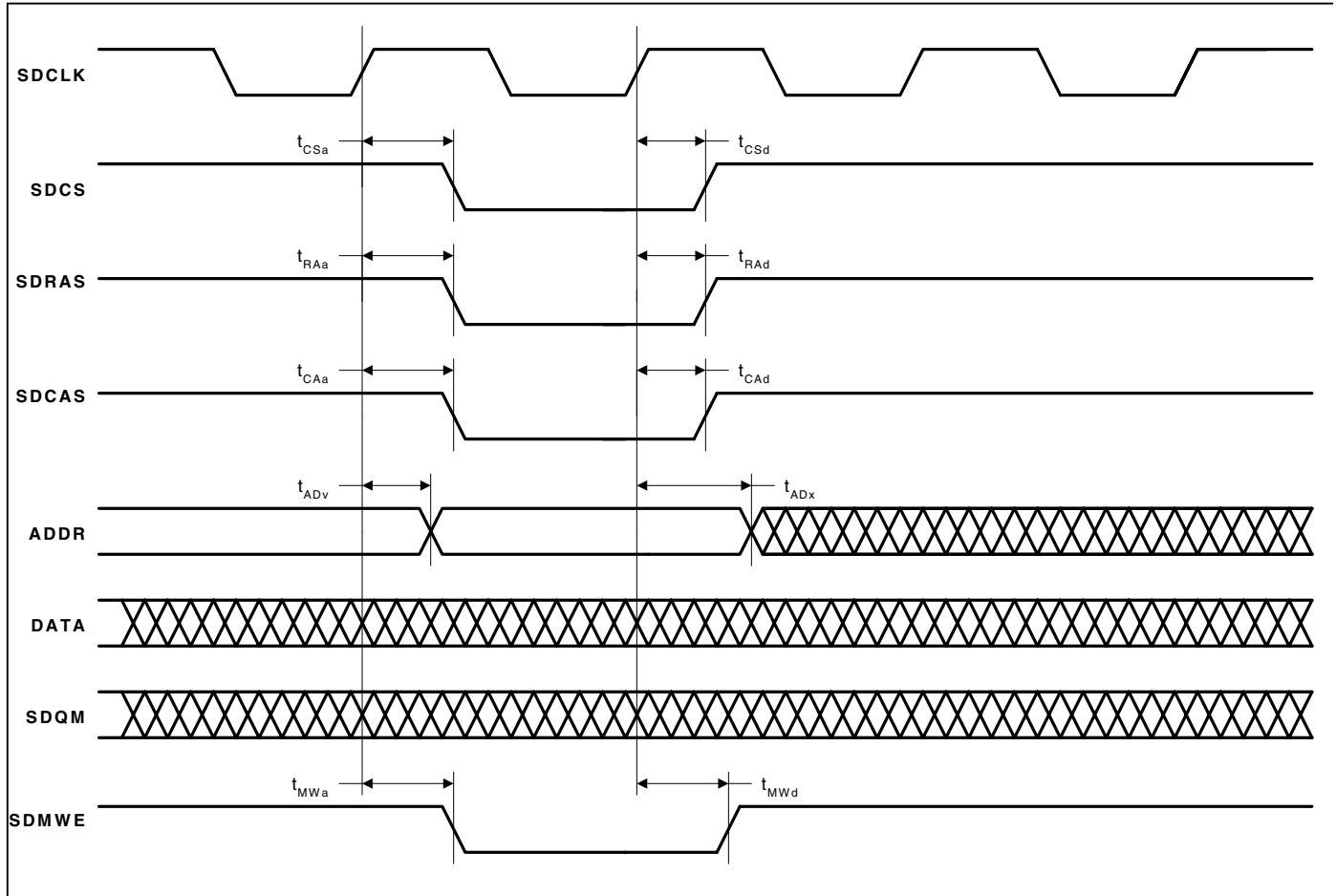
Figure 3. SDRAM Load Mode Register Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
      2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading.
      Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

SDRAM Burst Read Cycle

Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2

2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal.

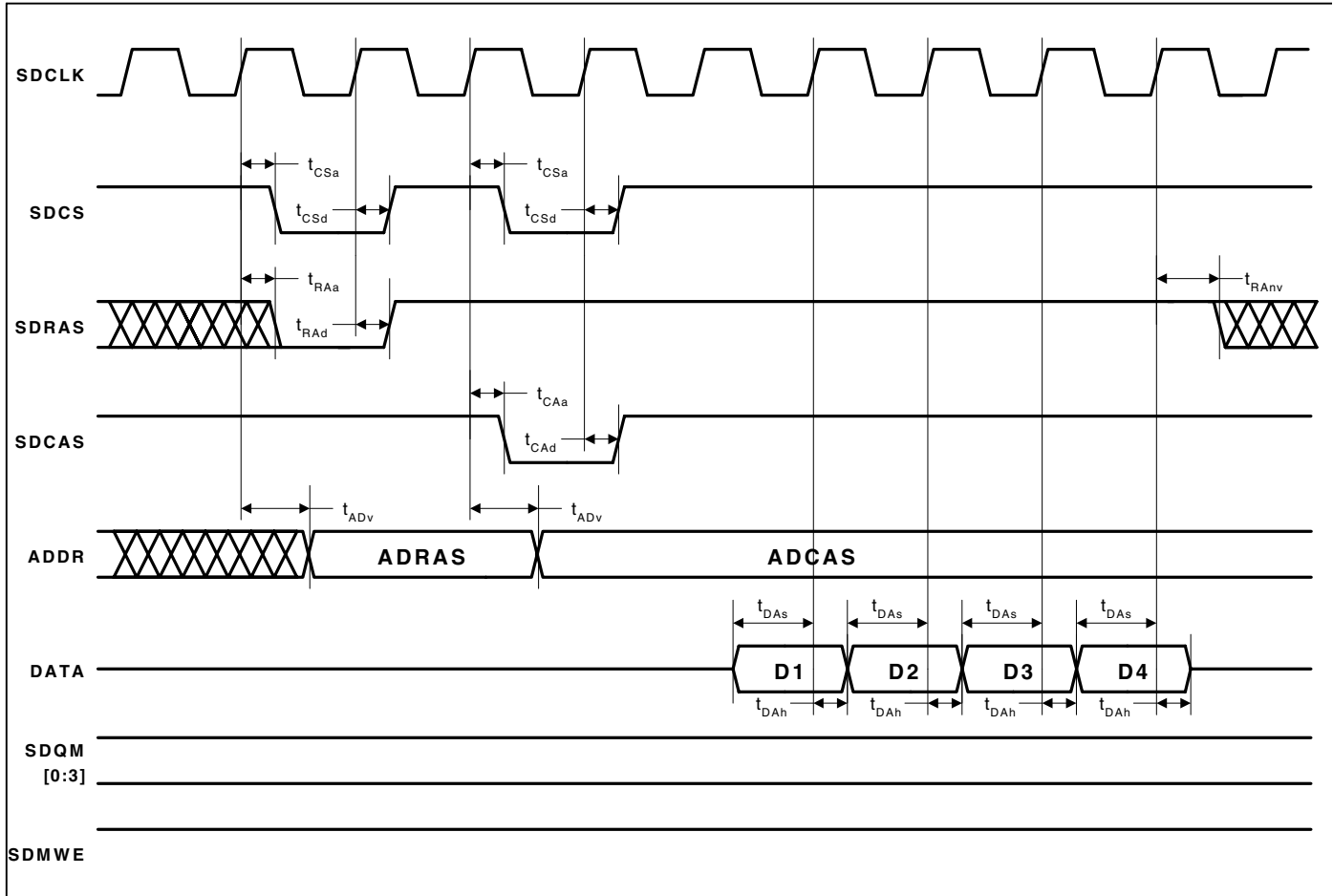## SDRAM Burst Write Cycle

Figure 5. SDRAM Burst Write Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
         2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading.
         Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal
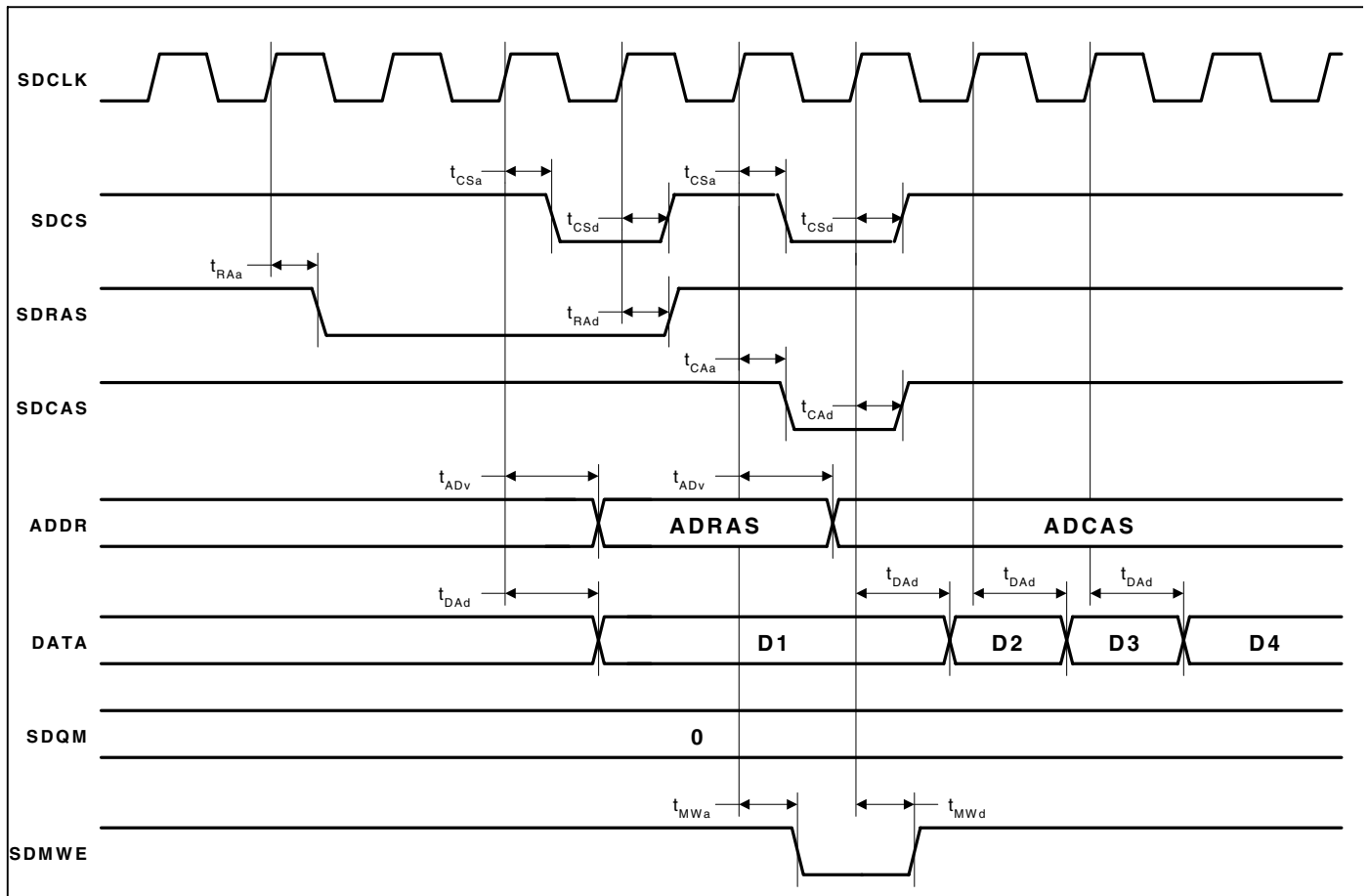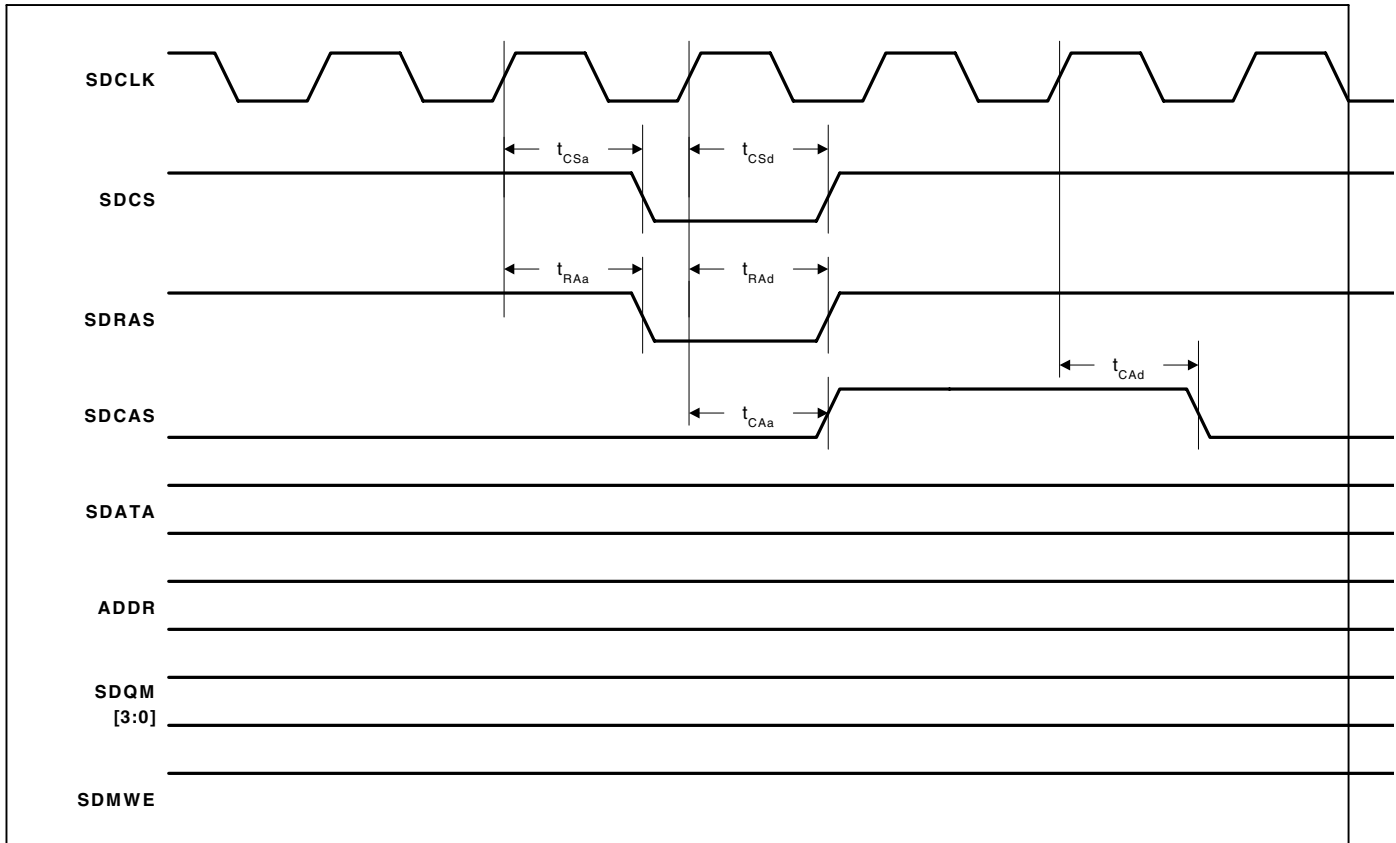
SDRAM Refresh Cycle

Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading.
Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

| Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Read Cycle
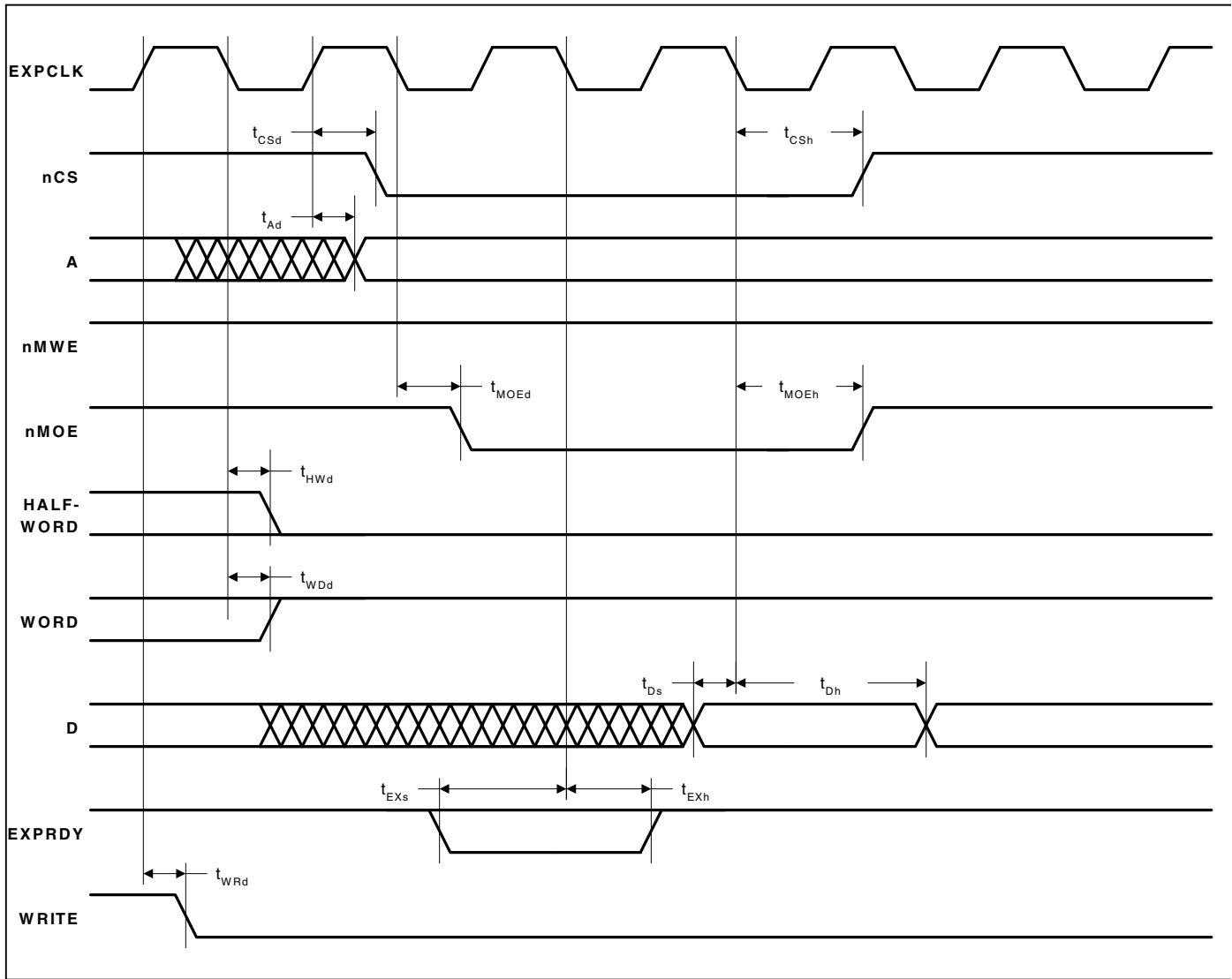
Figure 7. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Single Write Cycle
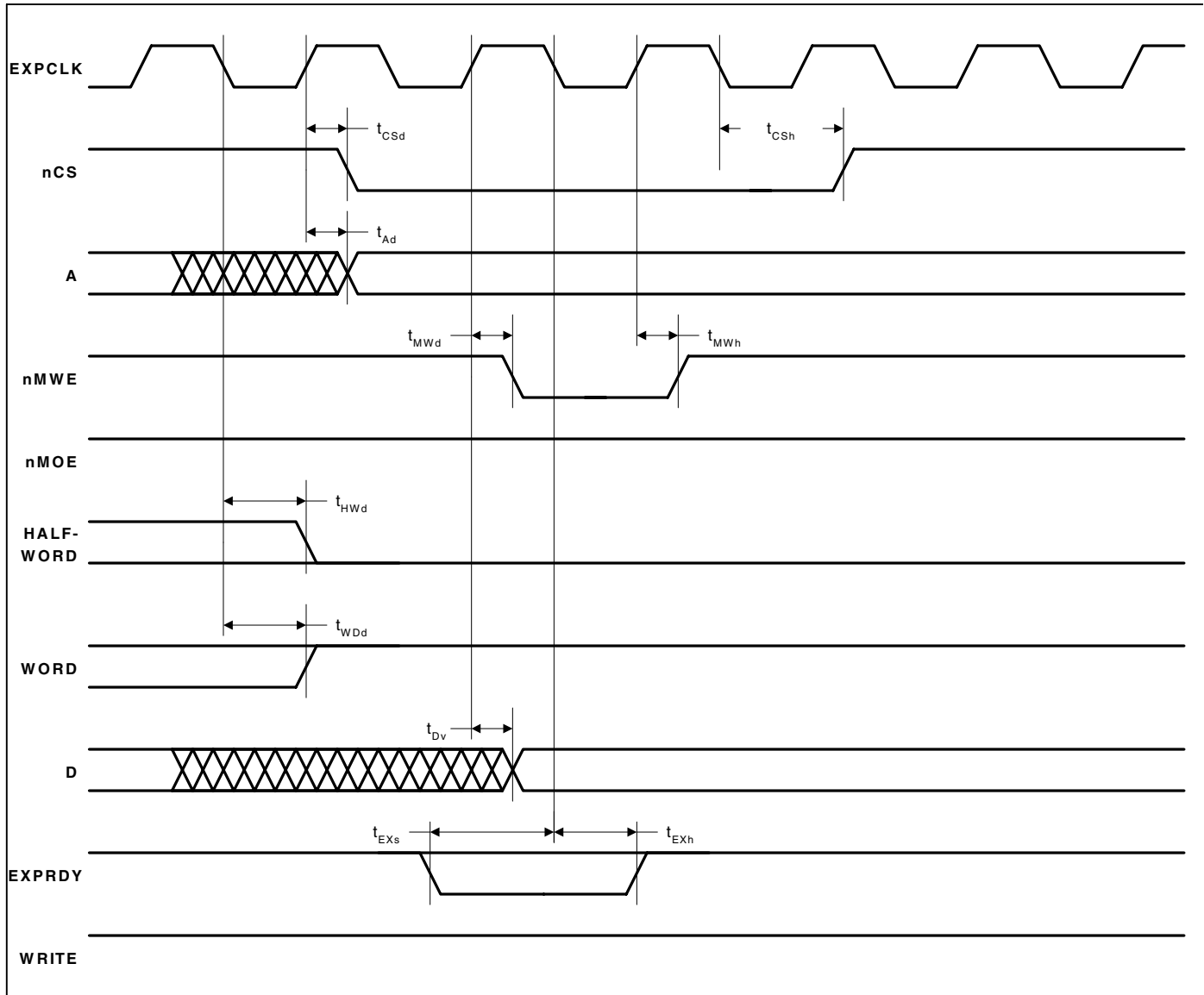
Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.
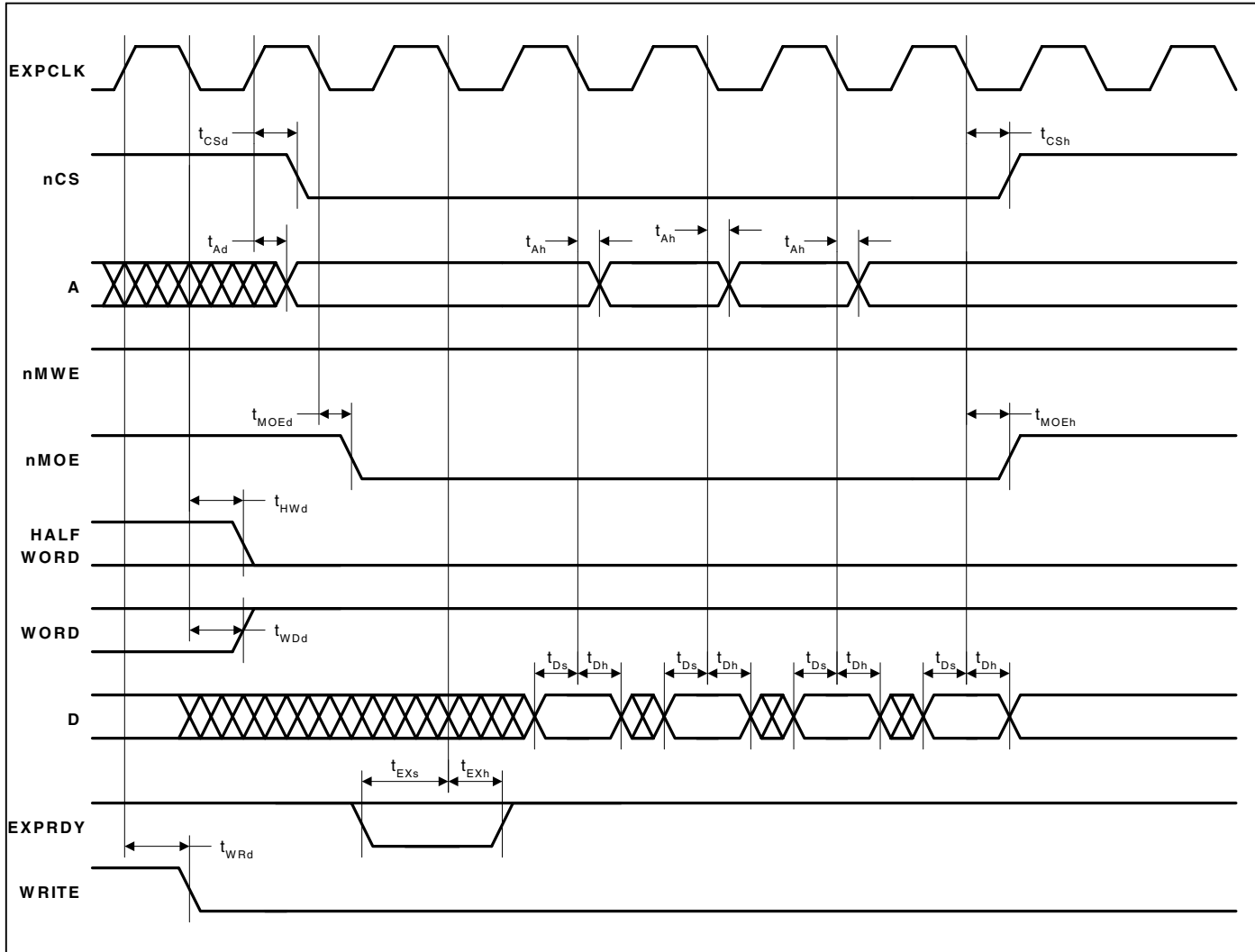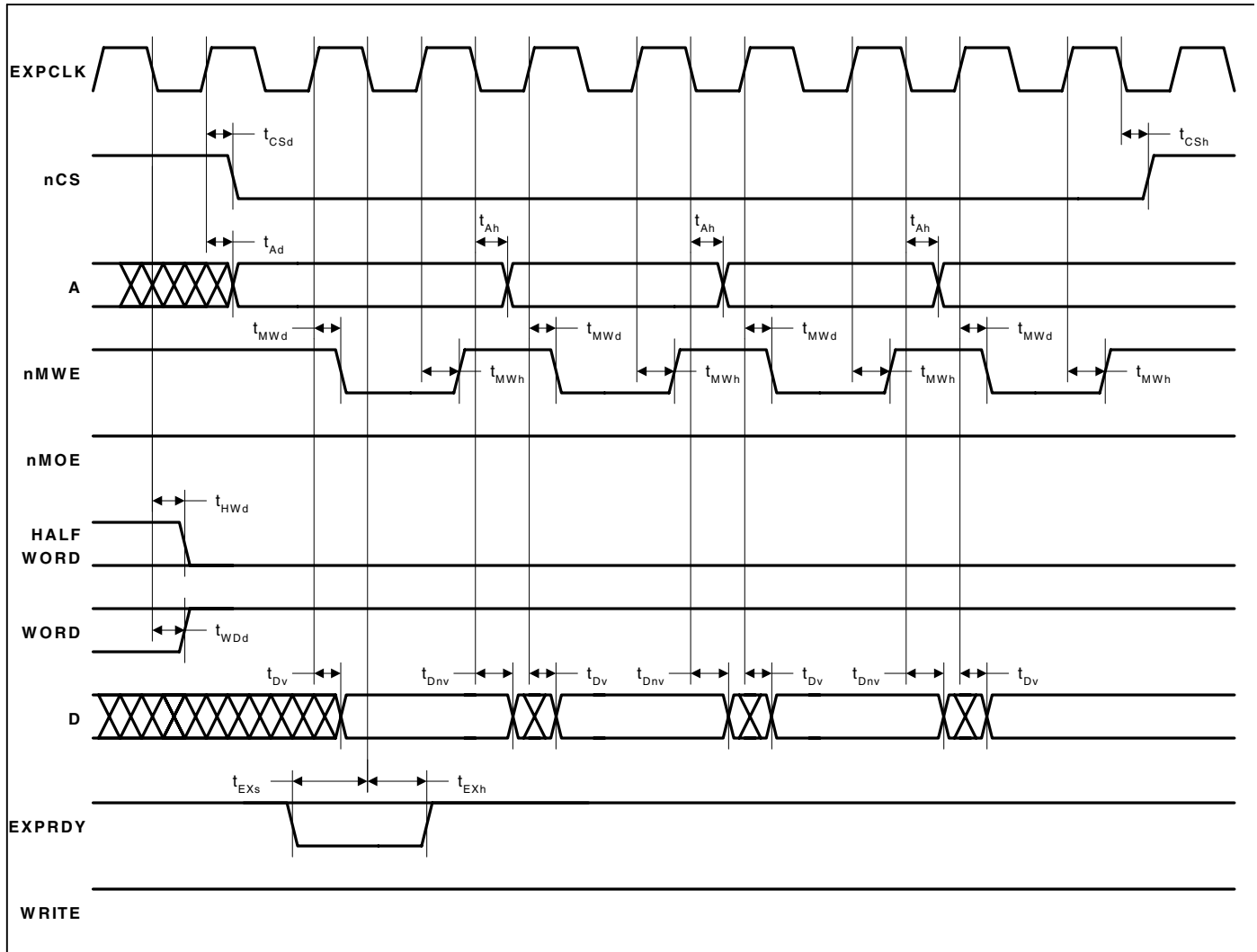
Static Memory Burst Read Cycle

Figure 9. Static Memory Burst Read Cycle Timing Measurement

Note: 1. *Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.*
2. *The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.*
3. *Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.*
4. *Address, Halfword, Word, and Write hold state until next cycle.*

Static Memory Burst Write Cycle

Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.

2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

4. Address, Data, Halfword, Word, and Write hold state until next cycle.