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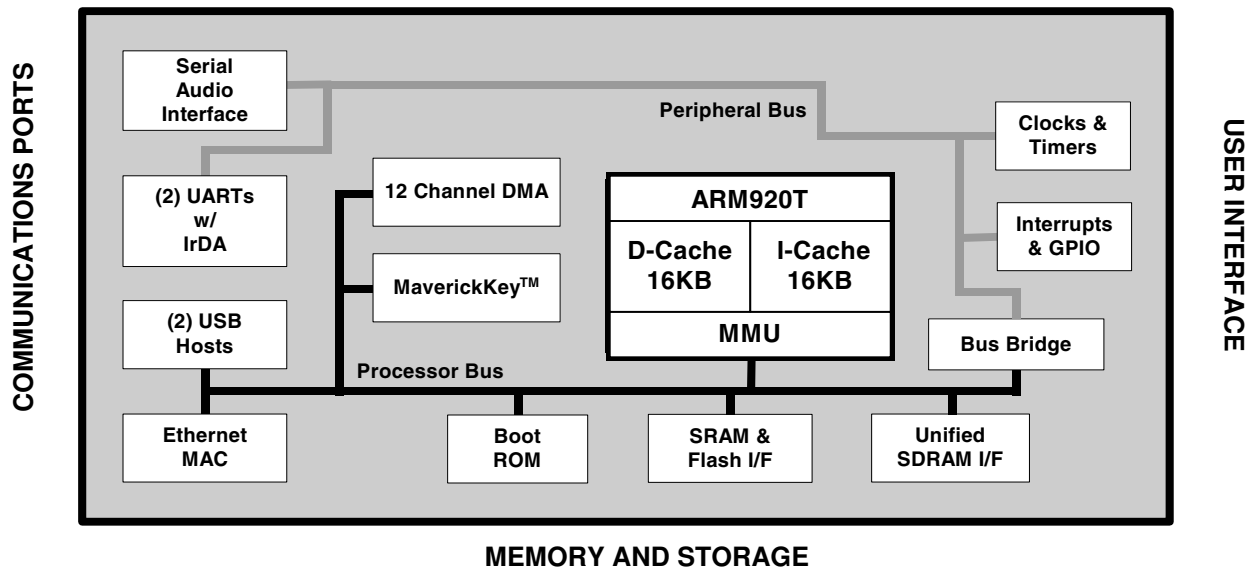


FEATURES

- 166-MHz ARM920T Processor
 - 16-kbyte Instruction Cache
 - 16-kbyte Data Cache
 - Linux[®], Microsoft[®] Windows[®] CE, enabled MMU
 - 66-MHz System Bus
- MaverickKey[™] IDs
 - 32-bit unique ID can be used for DRM-compliant, 128-bit random ID.
- Integrated Peripheral Interfaces
 - 16-bit SDRAM Interface (up to 4 banks)
 - 16-bit SRAM / FLASH / ROM
 - Serial EEPROM Interface
 - 1/10/100 Mbps Ethernet MAC
 - Two UARTs
 - Two-port USB 2.0 Full-speed Host (OHCI) (12 Mbits per second)
 - IrDA Interface
 - ADC
 - Serial Peripheral Interface (SPI) Port
 - 6-channel Serial Audio Interface (I²S)
 - 2-channel Low-cost Serial Audio Interface (AC'97)

**Entry-level ARM9
System-on-chip Processor**

- Internal Peripherals
 - 12 Direct Memory Access (DMA) Channels
 - Real-time Clock with software Trim
 - Dual PLL controls all clock domains.
 - Watchdog Timer
 - Two General-purpose 16-bit Timers
 - One General-purpose 32-bit Timer
 - One 40-bit Debug Timer
 - Interrupt Controller
 - Boot ROM
- Package
 - 208-pin LQFP


Preliminary Product Information

 This document contains information for a new product.
 Cirrus Logic reserves the right to modify this product without notice.

OVERVIEW

The EP9301 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Industrial controls
- Digital media servers
- Integrated home media gateways
- Digital audio jukeboxes
- Streaming audio players
- Set-top boxes
- Point-of-sale terminals
- Thin clients
- Biometric security systems
- GPS & fleet management systems
- Educational toys
- Industrial computers
- Industrial hand-held devices
- Voting machines
- Medical equipment

The EP9301 is one of a series of ARM920T-based devices. Other members of the family have different peripheral sets, a coprocessor, and different package configurations.

The ARM920T microprocessor core has a separate 16-kbyte, 64-way set-associative instruction and data caches.

The MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100 Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, AC'97 and I²S audio. A two-port USB 2.0 Full-speed Host (OHCI) (12 Mbits per second), two UARTs, and a analog voltage measurement analog-to-digital converter (ADC) are included as well.

The EP9301 is a high-performance, low-power RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 166 MHz. The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 675 mW.

Table A. Change History

Revision	Date	Changes
1	October 2003	Initial Release.
2	February 2004	Update timing specifications.
3	July 2004	Update AC data.
4	July 2004	Add ADC data.
5	March 2005	Update with most-current characterization data.

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Processor Core - ARM920T

The ARM920T is a Harvard architecture processor with separate 16-kbyte instruction and data caches with an 8-word line length but a unified memory. The processor utilizes a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16 kbyte Instruction Cache with lockdown
- 16 kbyte Data Cache (programmable write-through or write-back) with lockdown
- MMU for Linux[®], Microsoft[®] Windows[®] CE and other operating systems
- Translation Look Aside Buffers with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 1 Mbyte, 64 kbyte, 4 kbyte, and 1 kbyte
- Independent lockdown of TLB Entries

MaverickKey[™] Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP9301 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP9301 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

General Purpose Memory Interface (SDRAM, SRAM, ROM, FLASH)

The EP9301 features a unified memory address model where all memory devices are accessed over a common address/data bus. Memory accesses are performed via the Processor bus. The SRAM memory controller supports 8- and 16-bit devices and accommodates an internal boot ROM concurrently with 16-bit SDRAM memory.

- 1 to 4 banks of 16-bit, 66 MHz SDRAM
- Address and data bus shared between SDRAM, SRAM, ROM, and FLASH memory
- NOR FLASH memory supported

Table B. General Purpose Memory Interface Pin Assignments

Pin Mnemonic	Pin Description
SDCLK	SDRAM Clock
SDCLKEN	SDRAM Clock Enable
SDCSn[3:0]	SDRAM Chip Selects 3-0
RASn	SDRAM RAS
CASn	SDRAM CAS
SDWEn	SDRAM Write Enable
CSn[7:6] and CSn[3:0]	Chip Selects 7, 6, 3, 2, 1, 0
AD[25:0]	Address Bus 25-0
DA[15:0]	Data Bus 15-0
DQMn[1:0]	SDRAM Output Enables / Data Masks
WRn	SRAM Write Strobe
RDn	SRAM Read / OE Strobe
WAITn	SRAM Wait Input

Ethernet Media Access Controller (MAC)

The MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported. Features include:

- Supports 1/10/100 Mbps transfer rates for home / small-business / large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

Table C. Ethernet Media Access Controller Pin Assignments

Pin Mnemonic	Pin Description
MDC	Management Data Clock
MDIO	Management Data I/O
RXCLK	Receive Clock
MIIRXD[3:0]	Receive Data
RXDVAL	Receive Data Valid
RXERR	Receive Data Error
TXCLK	Transmit Clock
MIITXD[3:0]	Transmit Data
TXEN	Transmit Enable
TXERR	Transmit Error
CRS	Carrier Sense
CLD	Collision Detect

Serial Interfaces (SPI, I²S, and AC '97)

The Serial Peripheral Interface (SPI) port can be configured as a master or a slave, supporting the National Semiconductor[®], Motorola[®], and Texas Instruments[®] signaling protocols.

The AC'97 port supports multiple codecs for multichannel audio output with a single stereo input. The I²S port supports stereo 24-bit audio.

These ports are multiplexed so that the I²S port will take over either the AC'97 pins or the SPI pins.

- Normal Mode: One SPI Port and one AC'97 Port
- I²S on SSP Mode: One AC'97 Port and one I²S Port
- I²S on AC'97 Mode: One SPI Port and one I²S Port

Note: I²S may not be output on AC'97 and SSP ports at the same time.

Table D. Audio Interfaces Pin Assignment

Pin Name	Normal Mode	I ² S on SSP Mode	I ² S on AC'97 Mode
	Pin Description	Pin Description	Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

12-bit Analog-to-digital Converter (ADC)

The ADC block consists of a 12-bit analog-to-digital converter with a analog input multiplexer. The multiplexer can select to measure battery voltage and other miscellaneous voltages on the external measurement pins. Features include:

- 5 external pins for ADC measurement
- Measurement pin input range: 0 to 3.3 V.
- ADC-conversion-complete interrupt signal

Table E. 12-bit Analog-to-Digital Converter Pin Assignments

Pin Mnemonic	Pin Description
ADC[0] (Ym, pin 135)	External Analog Measurement Input
ADC[1] (sXp, pin 134)	External Analog Measurement Input
ADC[2] (sXm, pin 133)	External Analog Measurement Input
ADC[3] (sYp, pin 132)	External Analog Measurement Input
ADC[4] (sYm, pin 131)	External Analog Measurement Input

Universal Asynchronous Receiver/Transmitters (UARTs)

Two 16550-compatible UARTs are supplied. One provides asynchronous HDLC (High-level Data Link Control) protocol support for full duplex transmit and receive. The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency, and optionally passes the CRC to the host at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency. The host must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams. The second UART provides IrDA[®] compatibility.

- UART1 supports modem bit rates up to 115.2 kbps, supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.

Table F. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTS _n	UART1 Clear To Send / Transmit Enable
DSR _n / DCD _n	UART1 Data Set Ready / Data Carrier Detect
DTR _n	UART1 Data Terminal Ready
RTS _n	UART1 Ready To Send
EGPIO[0] / RI	UART1 Ring Indicator
TXD1 / SIROUT	UART2 Transmit / IrDA Output
RXD1 / SIRIN	UART2 Receive / IrDA Input

Dual Port USB Host

The USB Open Host Controller Interface (Open HCI) provides full speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tiered-start” topology.

This includes the following feature:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification

- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections
- Root HUB integrated with 2 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table G. Dual Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2,0]	USB Positive signals
USBm[2,0]	USB Negative Signals

Note: USBm[1] and USBp[1] are not bonded out.

Two-Wire Interface With EEPROM Support

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table H. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Real-Time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ± 1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9301 device will not boot.

Table I. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Table J. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer ensures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free-running down counters or as periodic timers for fixed-interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 μ s to 73.3 hours.

One 40-bit debug timer, plus a 6-bit prescale counter, has a range of 1.0 μ s to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 54 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time-critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active high or active low level sensitive inputs. GPIO pins programmed as interrupts may be programmed as active high level sensitive, active low level sensitive, rising edge triggered, falling edge triggered, or combined rising/falling edge triggered.

- Supports 54 interrupts from a variety of sources (such as UARTs, GPIO and ADC)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Three dedicated off-chip interrupt lines INT[2:0] operate as active-high level-sensitive interrupts
- Any of the 19 GPIO lines maybe configured to generate interrupts

- Software supported priority mask for all FIQs and IRQs

Table K. External Interrupt Controller Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[3] and INT[1:0]	External Interrupts 2, 1, 0

Note: INT[2] is not bonded out.

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table L. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 16 EGPIO and the 3 FGPIO pins may each be configured individually as an output, an input or an interrupt input.

There are 10 pins that may alternatively be used as input, output, or open-drain pins, but do not support interrupts. These pins are:

- Ethernet MDIO
- Both LED Outputs
- EEPROM Clock and Data
- HGPIO[5:2]
- CGPIO[0]

6 pins may alternatively be used as inputs only:

- CTS_n, DSR_n / DCD_n
- 3 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTS_n
- ARST_n

Table M. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[3:1]	Expanded General Purpose Input / Output Pins with Interrupts

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 166 MHz.

Table N. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table O. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Internal Boot ROM

The Internal 16 kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP93xx User's Manual for operational details.

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
Power Supplies	RVDD	-	3.96	V
	CVDD	-	2.16	V
	VDD_PLL	-	2.16	V
	VDD_ADC	-	3.96	V
Total Power Dissipation (Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)		-	±10	mA
Output current per pin, DC		-	±50	mA
Digital Input voltage (Note 2)		-0.3	RVDD+0.3	V
Storage temperature		-40	+125	°C

- Note: 1. Includes all power generated by AC and/or DC output loading.
 2. The power supply pins are at recommended maximum values.
 3. At ambient temperatures above 70° C, total power dissipation must be limited to less than 2.5 Watts.

WARNING: Operation beyond these limits may result in permanent damage to the device.
 Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD	3.0	3.3	3.6	V
	CVDD	1.65	1.80	1.94	V
	VDD_PLL	1.65	1.80	1.94	V
	VDD_ADC	3.0	3.3	3.6	V
Operating Ambient Temperature - Commercial	T _A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T _A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	166	MHz
Processor Clock Speed - Industrial	FCLK	-	-	166	MHz
System Clock Speed - Commercial	HCLK	-	-	66	MHz
System Clock Speed - Industrial	HCLK	-	-	66	MHz

DC Characteristics

($T_A = 0$ to 70°C ; $CVDD = VDD_PLL = 1.8$; $RVDD = 3.3\text{ V}$;
All grounds = 0 V ; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Max	Unit
High level output voltage	$I_{out} = -4\text{ mA}$	(Note 4)	V_{oh}	$0.85 \times RVDD$	-	V
Low level output voltage	$I_{out} = 4\text{ mA}$		V_{ol}	-	$0.15 \times RVDD$	V
High level input voltage		(Note 5)	V_{ih}	$0.65 \times RVDD$	$VDD + 0.3$	V
Low level input voltage		(Note 5)	V_{il}	-0.3	$0.35 \times RVDD$	V
High level leakage current	$V_{in} = 3.3\text{ V}$	(Note 5)	I_{ih}	-	10	μA
Low level leakage current	$V_{in} = 0$	(Note 5)	I_{il}	-	-10	μA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded), 25°C					
Power Supply Current:	CVDD / VDD_PLL Total	-	180	230	mA
	RVDD	-	45	80	mA
Low-Power Mode Supply Current	CVDD / VDD_PLL Total	-	2	3.5	mA
	RVDD	-	1.0	2	mA

Note: 4. For open drain pins, high level output voltage is dependent on the external load.

5. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation (See [Table Q on page 38](#)). If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

Timings

Timing Diagram Conventions

This data sheet contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

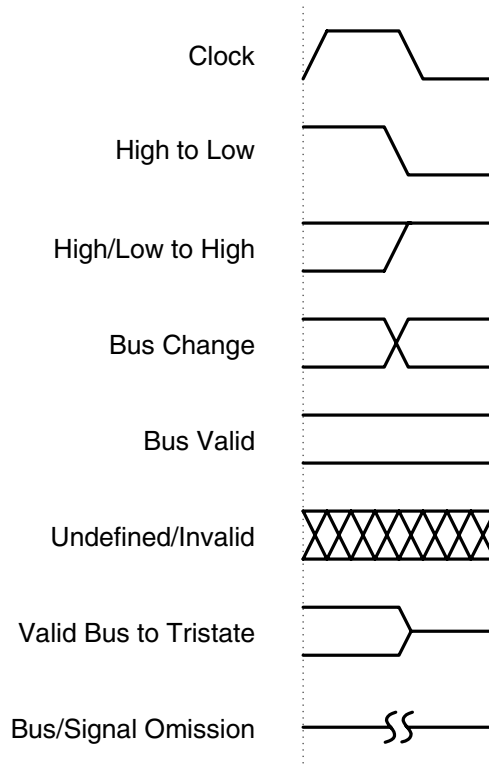


Figure 1. Timing Diagram Drawing Key

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements.

- $T_A = 0$ to 70°C
- $CVDD = VDD_PLL = 1.8\text{V}$
- $RVDD = 3.3\text{V}$
- All grounds = 0V
- Logic 0 = 0V , Logic 1 = 3.3V
- Output loading = 50pF
- Timing reference levels = 1.5V
- The Processor Bus Clock (HCLK) is programmable and is set by the user. The frequency is typically between 33MHz and 100MHz (92MHz for industrial conditions).

Memory Interface

Figure 2 through Figure 5 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK high time	$t_{\text{clk_high}}$	-	$(t_{\text{HCLK}}) / 2$	-	ns
SDCLK low time	$t_{\text{clk_low}}$	-	$(t_{\text{HCLK}}) / 2$	-	ns
SDCLK rise/fall time	t_{clkrf}	-	2	4	ns
Signal delay from SDCLK rising edge time	t_d	-	-	8	ns
Signal hold from SDCLK rising edge time	t_h	1	-	-	ns
DQMn delay from SDCLK rising edge time	t_{DQd}	-	-	8	ns
DQMn hold from SDCLK rising edge time	t_{DQh}	1	-	-	ns
DA valid setup to SDCLK rising edge time	t_{DAs}	2	-	-	ns
DA valid hold from SDCLK rising edge time	t_{DAh}	3	-	-	ns

SDRAM Load Mode Register Cycle

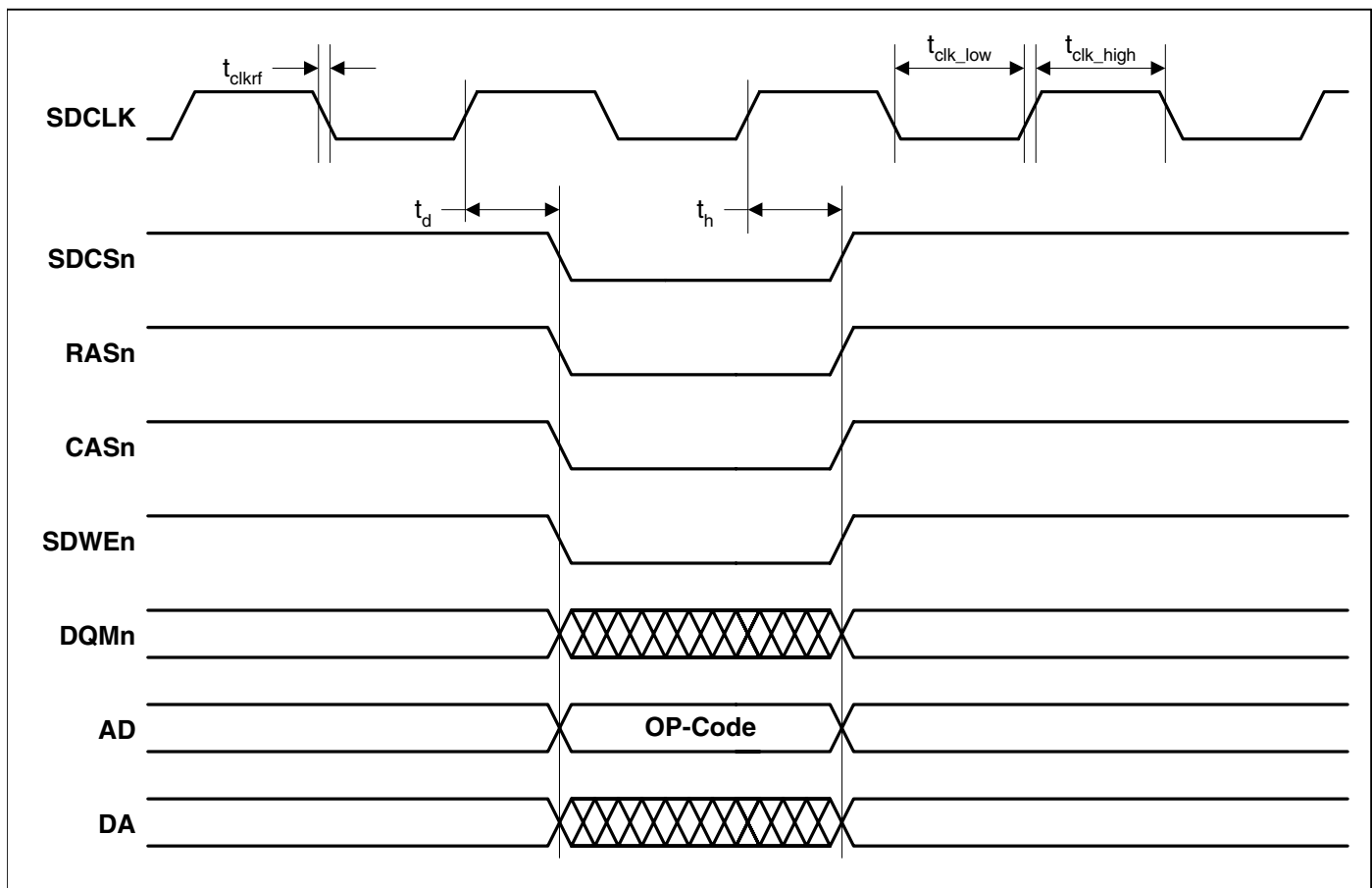
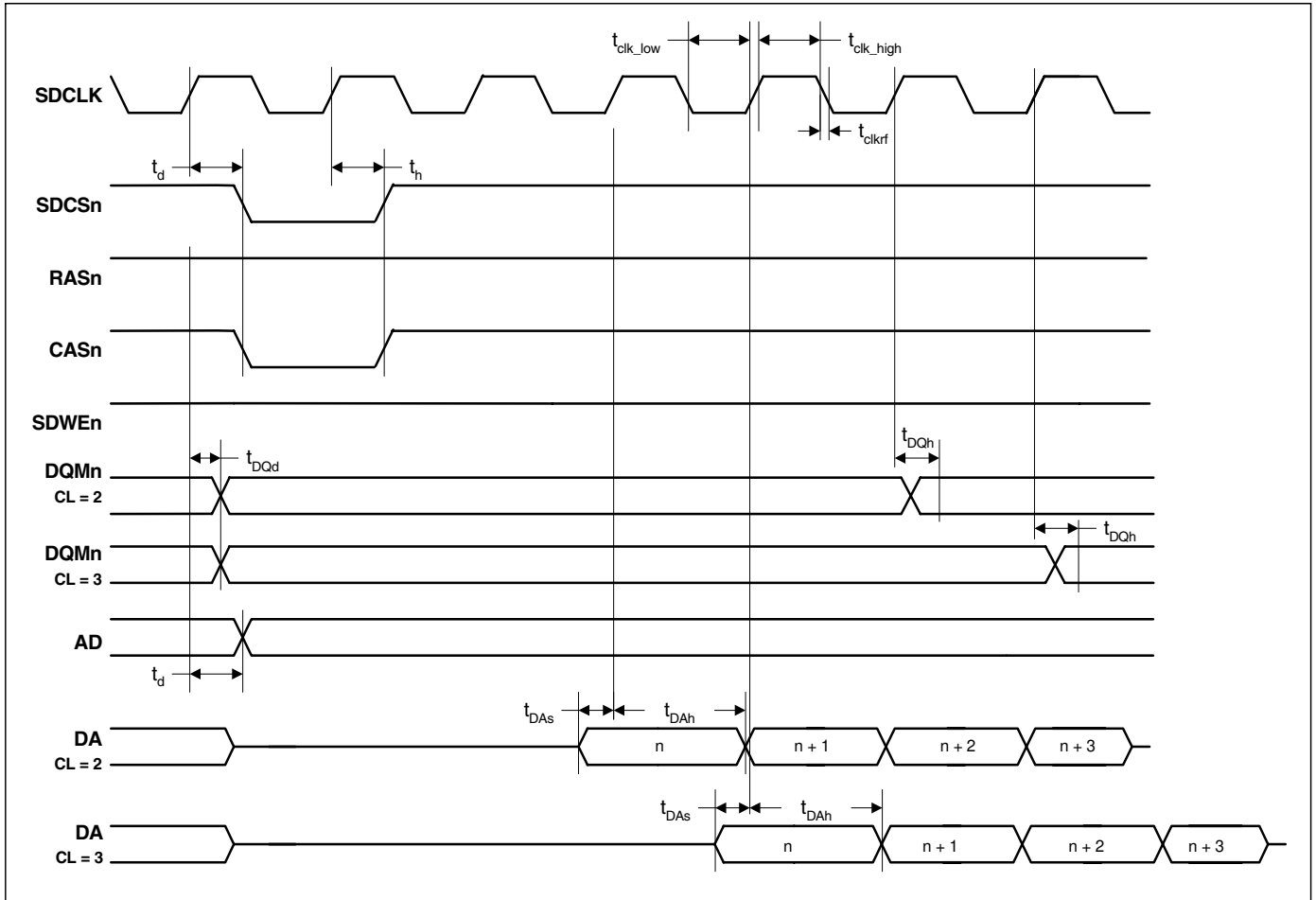


Figure 2. SDRAM Load Mode Register Cycle Timing Measurement

SDRAM Burst Read Cycle

Figure 3. SDRAM Burst Read Cycle Timing Measurement

SDRAM Burst Write Cycle

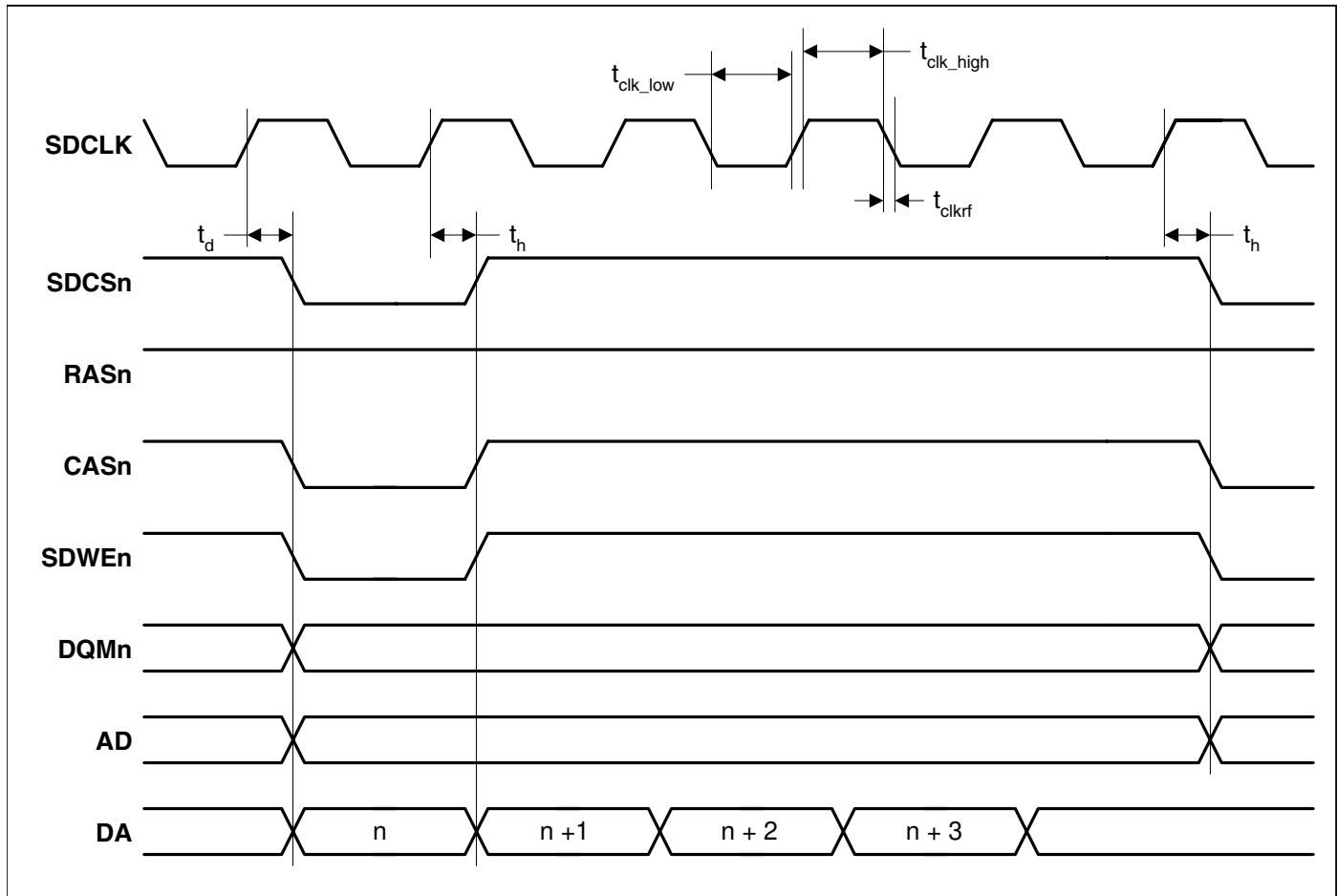
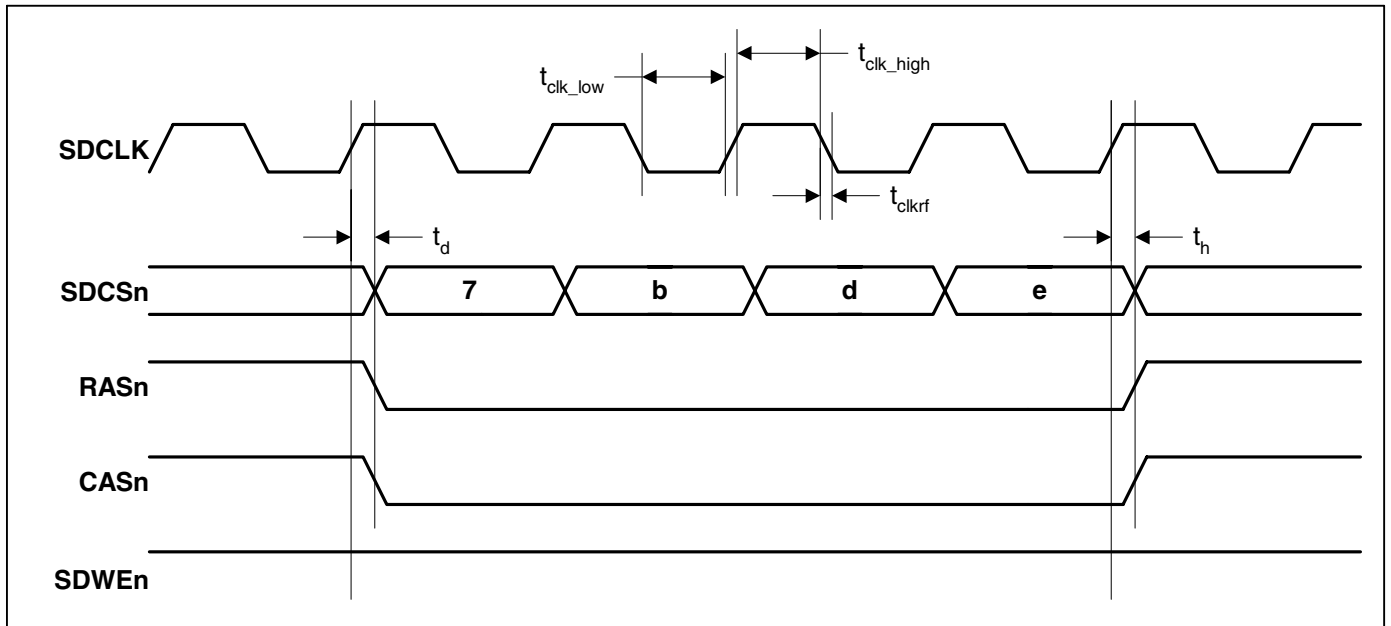


Figure 4. SDRAM Burst Write Cycle Timing Measurement

SDRAM Auto Refresh Cycle


Note: Chip select shown as bus to illustrate multiple devices being put into auto refresh in one access

Figure 5. SDRAM Auto Refresh Cycle Timing Measurement

Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

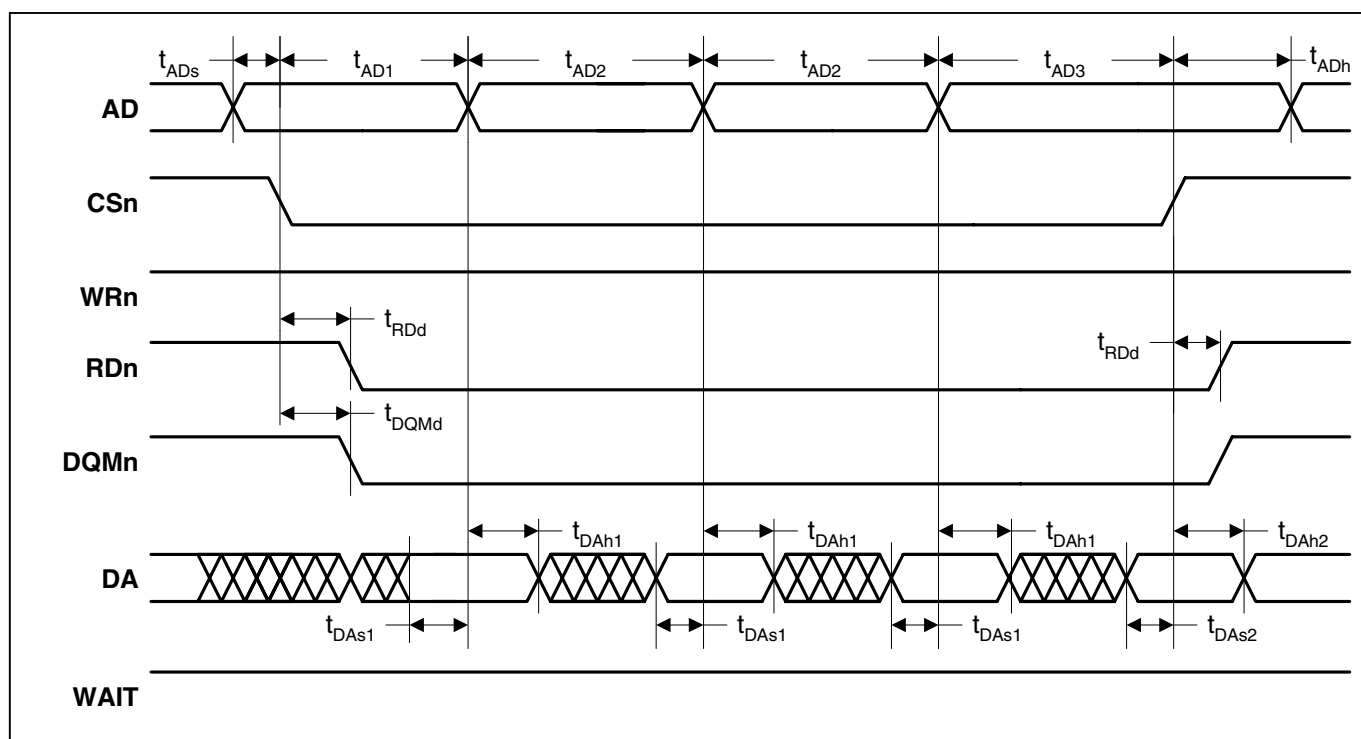
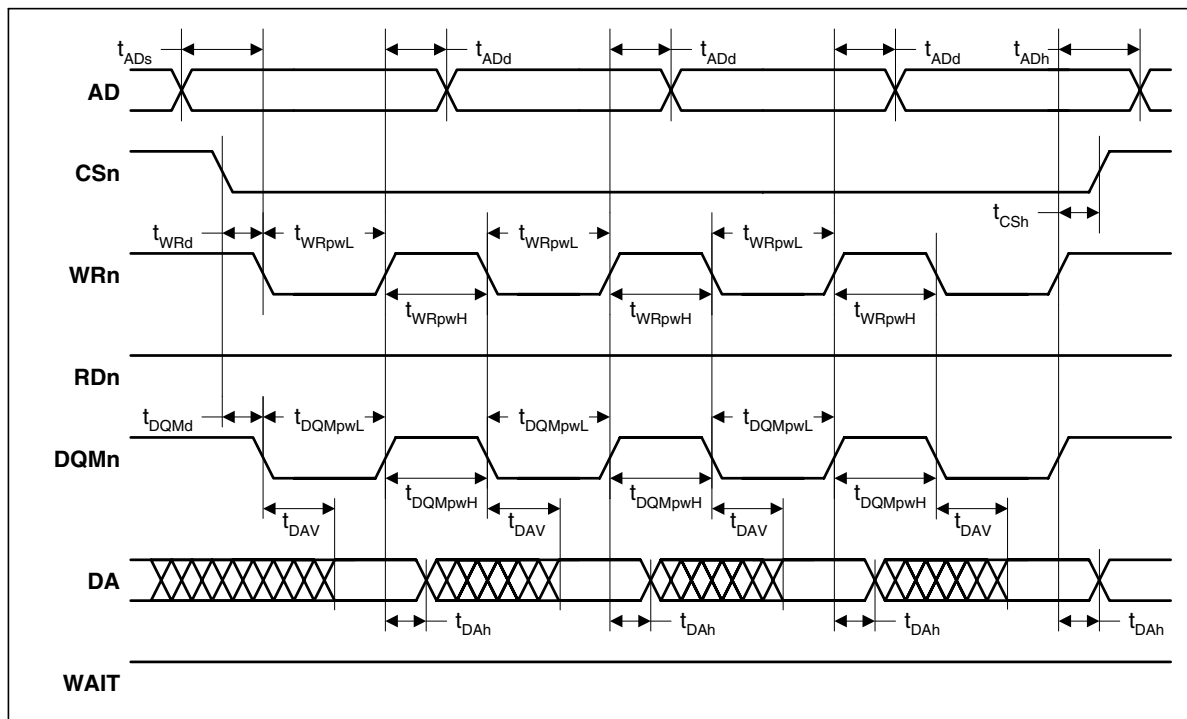


Figure 6. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns


Figure 7. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

Static Memory 32-bit Read on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to AD transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd2}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwl}	-	$t_{HCLK} \times ((2 \times WST1) + 3)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

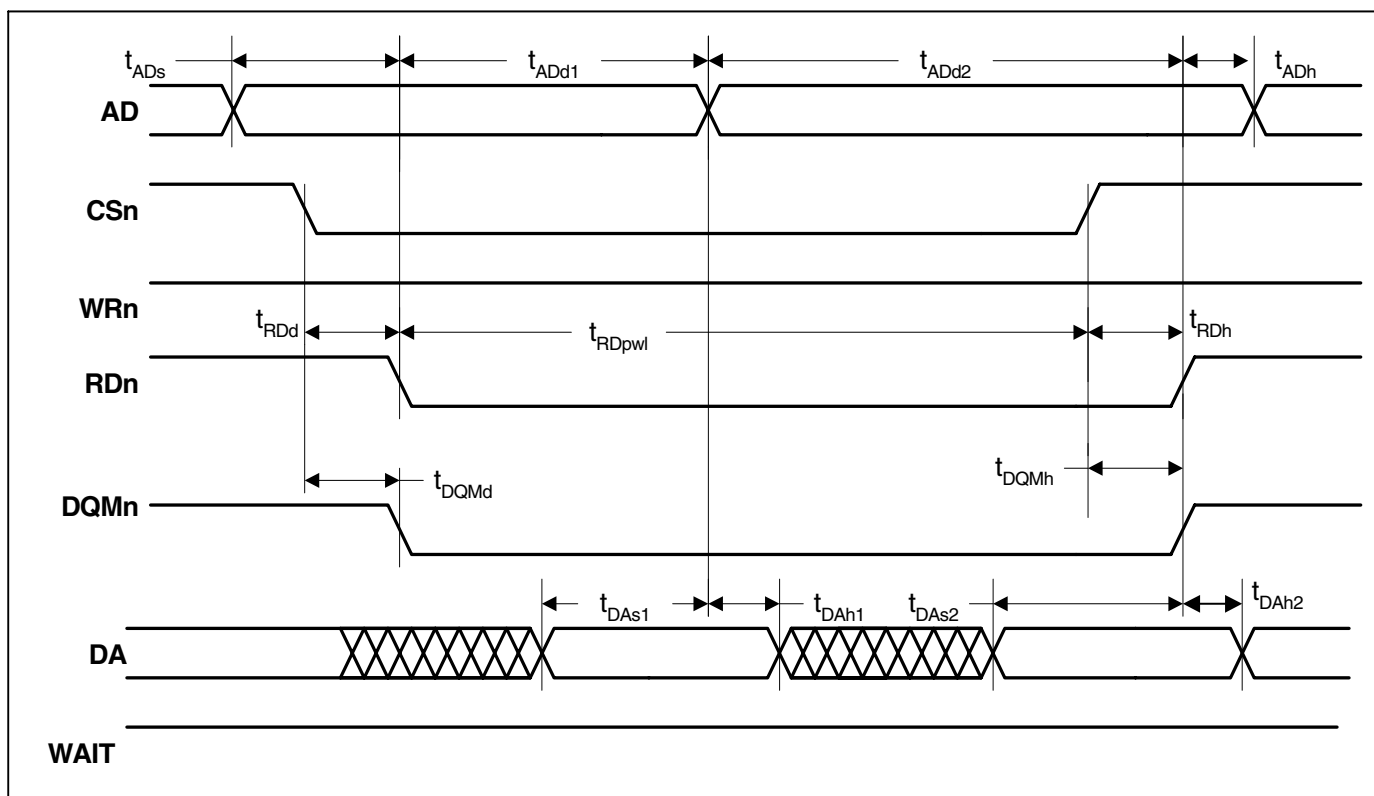
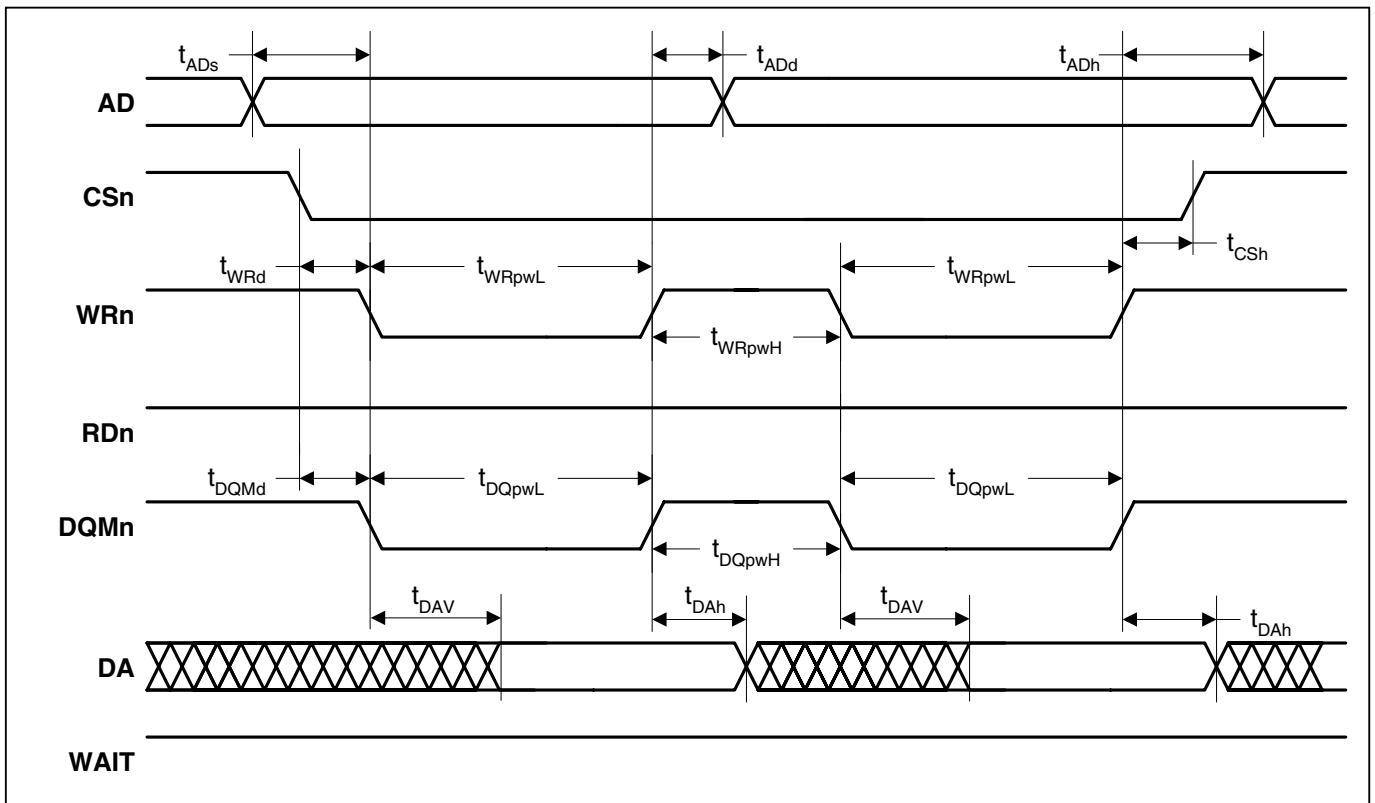


Figure 8. Static Memory Multiple Word Read 16-bit Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSH}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns


Figure 9. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

Static Memory Burst Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to Address 1 transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{ADd2}	-	$t_{HCLK} \times (WST2 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to CSn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

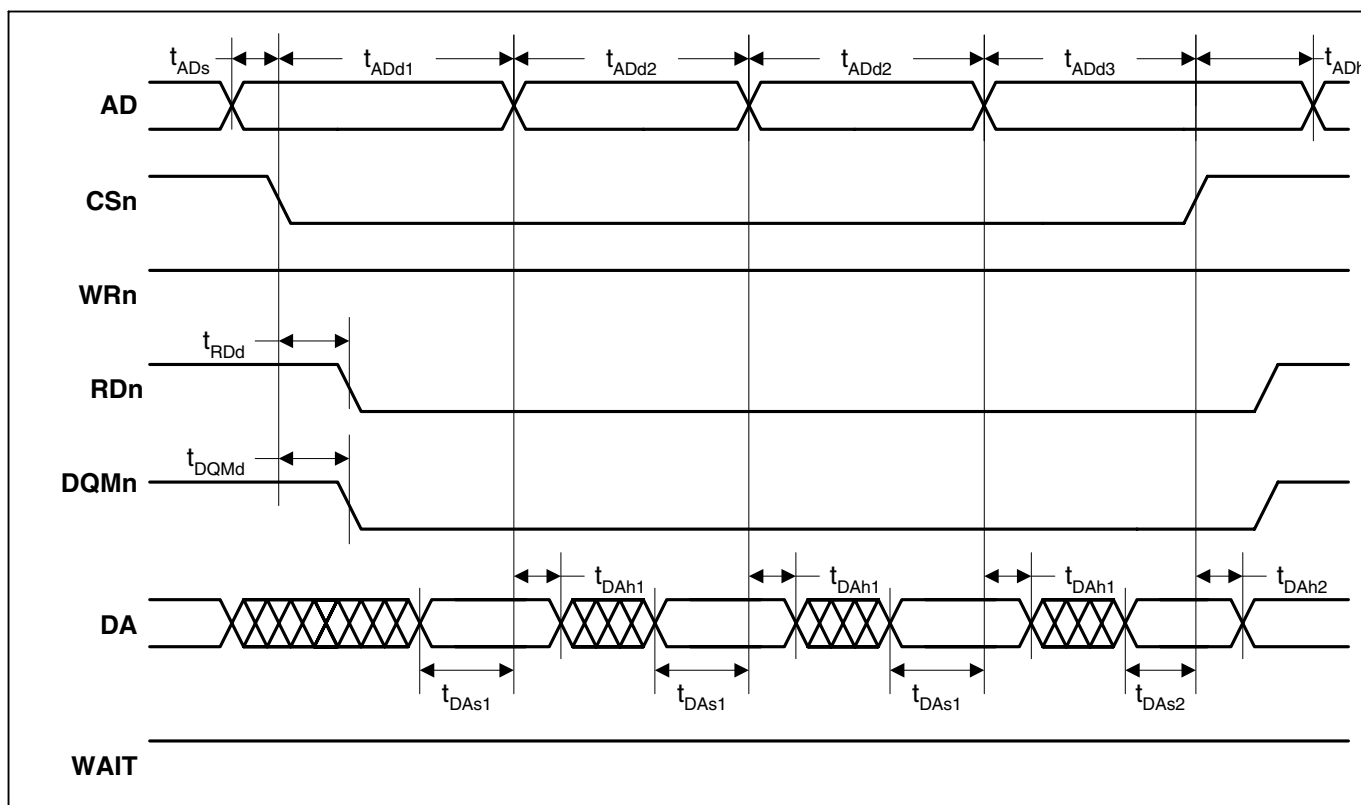


Figure 10. Static Memory Burst Read Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSH}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpWL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpWH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpWL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpWH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

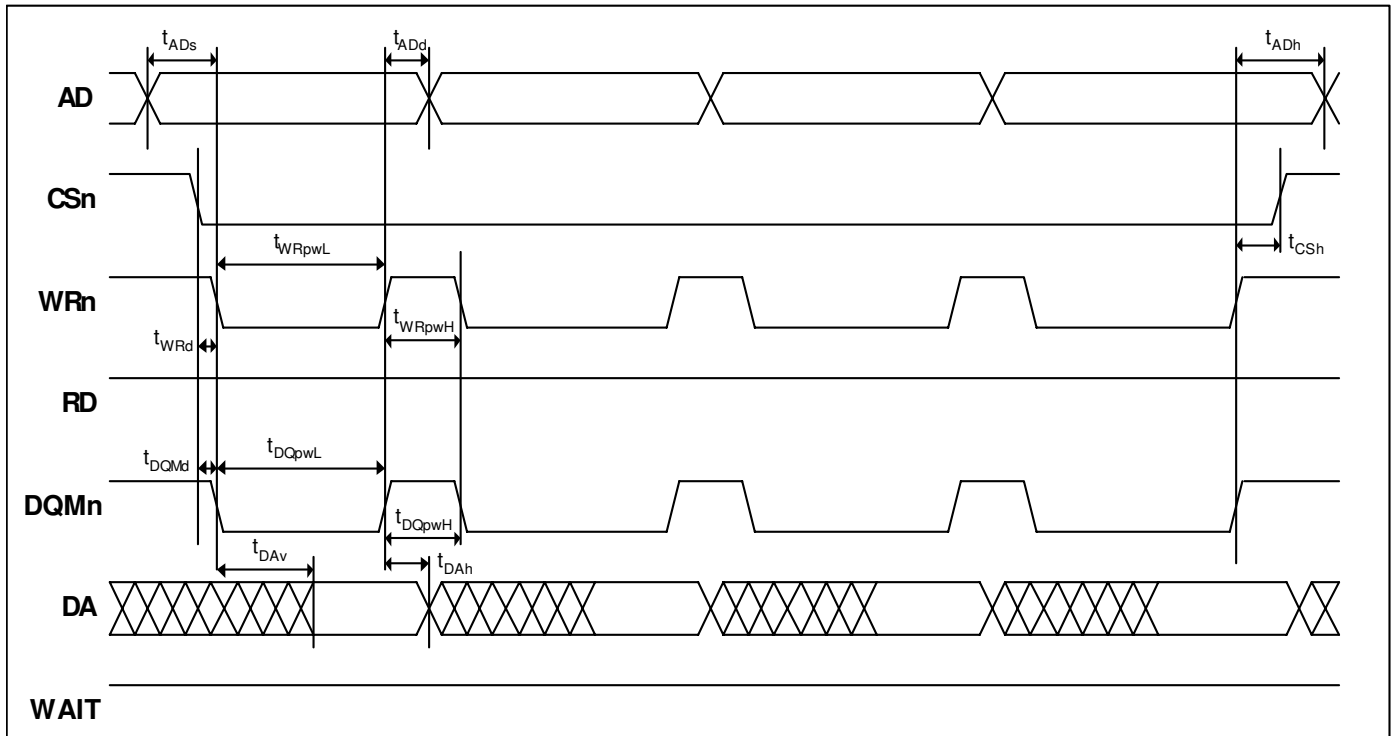


Figure 11. Static Memory Burst Write Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

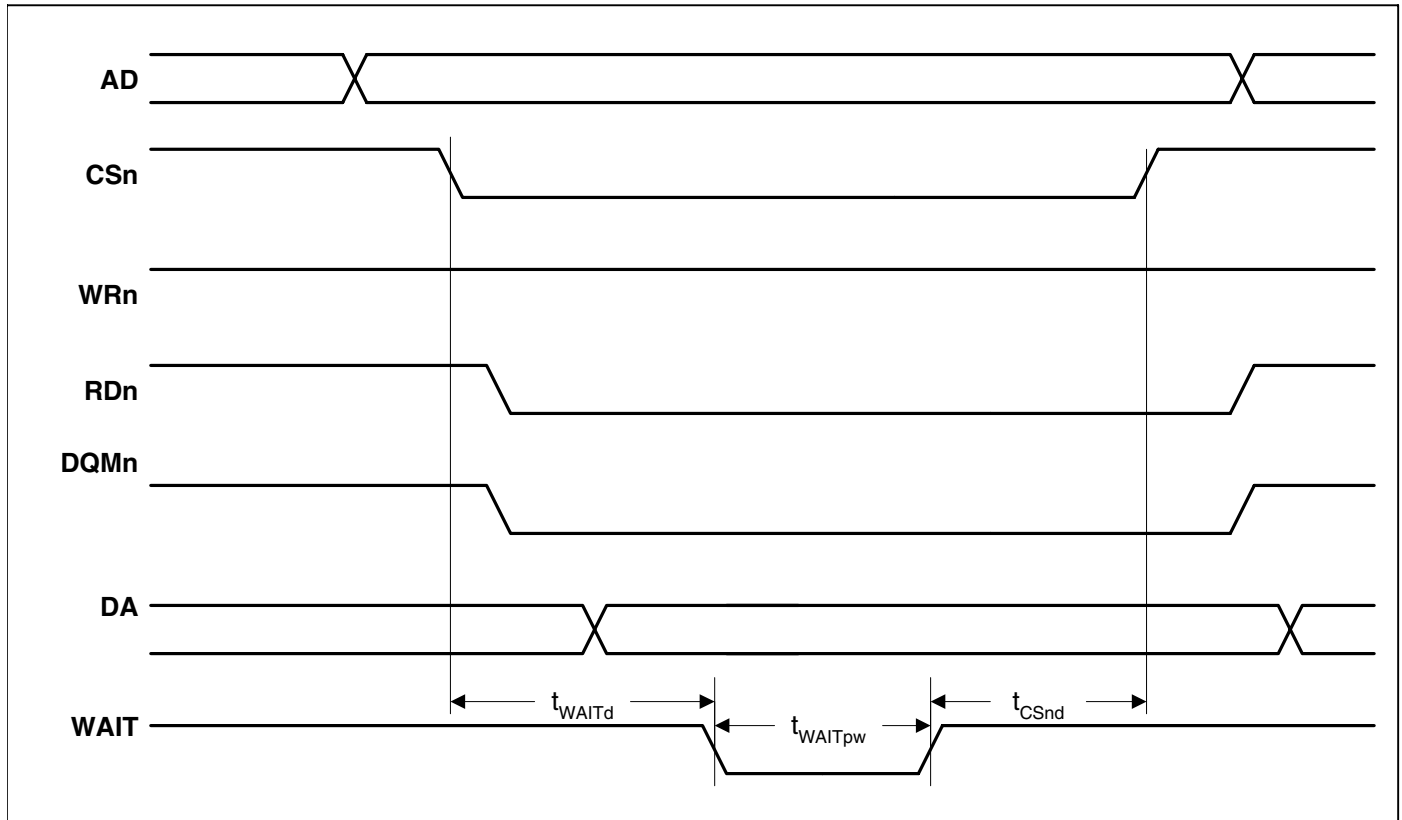
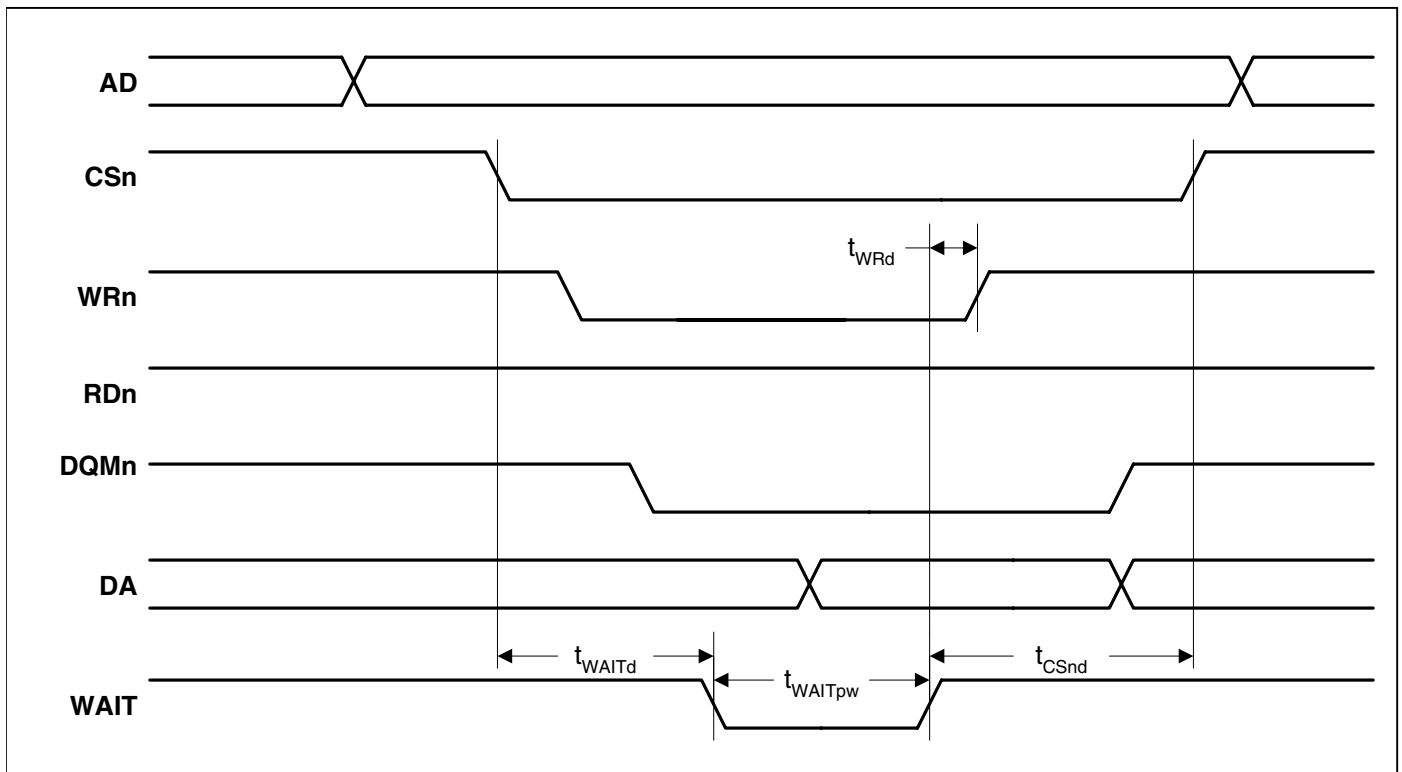


Figure 12. Static Memory Single Read Wait Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns


Figure 13. Static Memory Single Write Wait Cycle Timing Measurement