Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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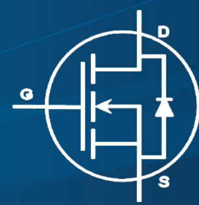
EPC2015C – Enhancement Mode Power Transistor

V_{DSS} , 40 V
$R_{DS(on)}$, 4 mΩ
I_D , 53 A

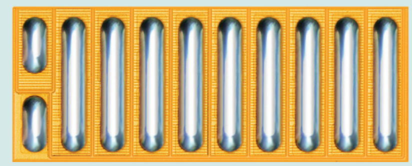


EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous (T_A = 25˚C, $R_{\Theta JA}$ = 6˚C/W)	53	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	235	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	



EPC2015C eGaN® FETs are supplied only in passivated die form with solder bars
Die size: 4.1 mm x 1.6 mm

Applications
- Industrial Automation
- Synchronous Rectification
- Class-D Audio

Benefits
- Ultra High Efficiency
- Ultra Low Switching and Conduction Losses
- Zero Q_{RR}
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2015C.aspx

Static Characteristics (T_J = 25˚C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 500 µA	40			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 32 V, V_{GS} = 0 V		200	400	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		1	7	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		200	400	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 9 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 33 A		3.2	4	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

All measurements were done with substrate shorted to source.

Thermal Characteristics

		TYP	UNIT
$R_{\Theta JC}$	Thermal Resistance, Junction to Case	0.8	˚C/W
$R_{\Theta JB}$	Thermal Resistance, Junction to Board	1.7	˚C/W
$R_{\Theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	54	˚C/W

Note 1: $R_{\Theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J = 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V		980	1180	pF
C_{RSS}	Reverse Transfer Capacitance			18		
C_{OSS}	Output Capacitance			710	1070	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 20 V, V_{GS} = 0 V		870		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			940		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 5 V, I_D = 33 A		8.7	11.2	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 20 V, I_D = 33 A		2.7		
Q_{GD}	Gate-to-Drain Charge			1.2		
$Q_{G(TH)}$	Gate Charge at Threshold			1.9		
Q_{OSS}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		19	29	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

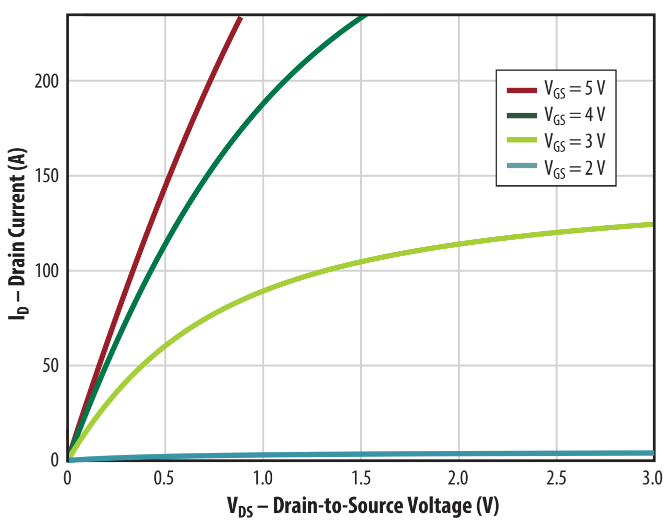


Figure 2: Transfer Characteristics

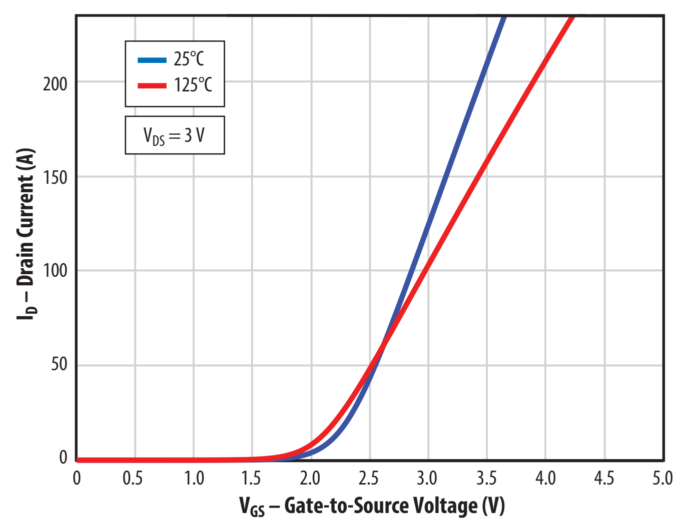


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

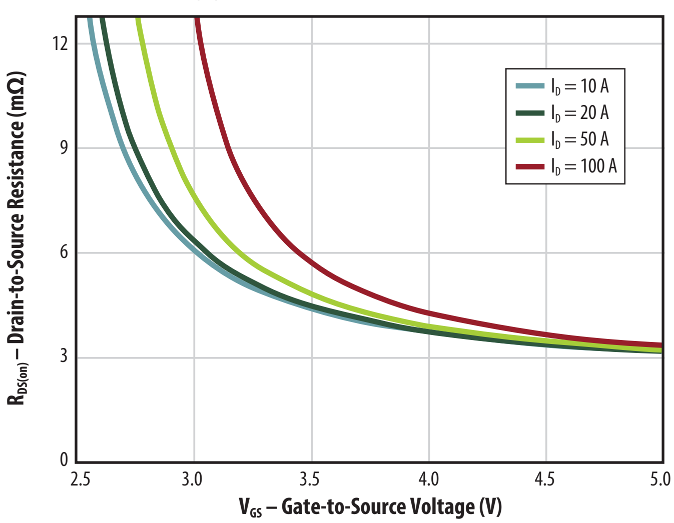


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

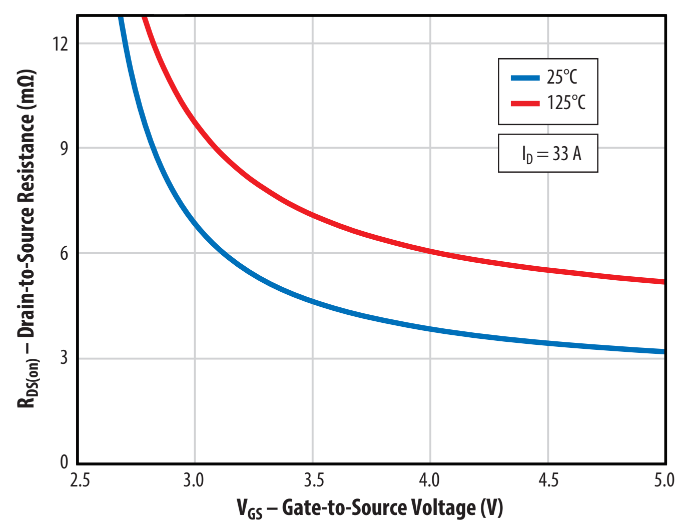


Figure 5a: Capacitance (Linear Scale)

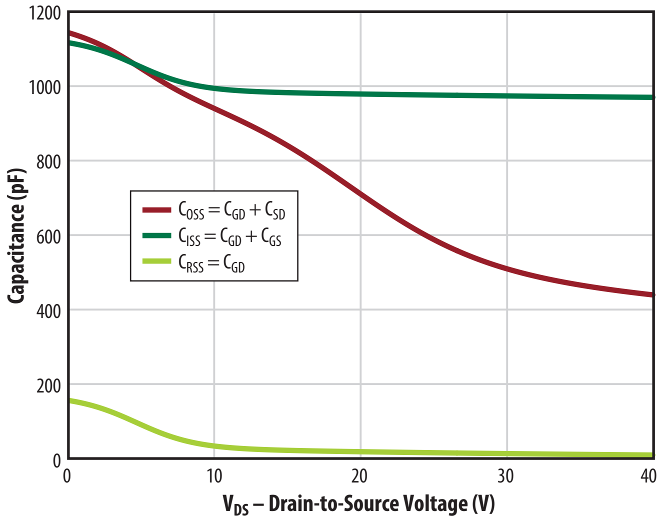


Figure 5b: Capacitance (Log Scale)

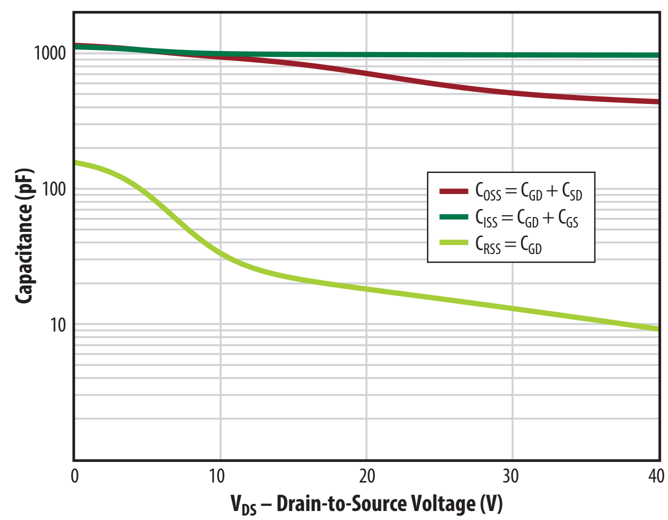


Figure 6: Gate Charge

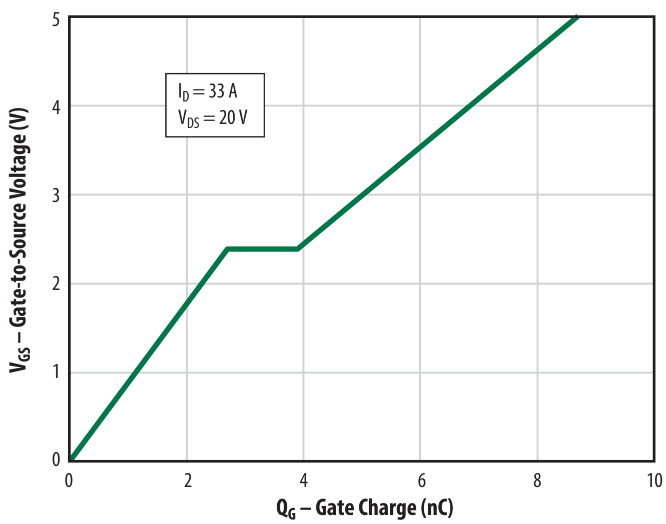


Figure 7: Reverse Drain-Source Characteristics

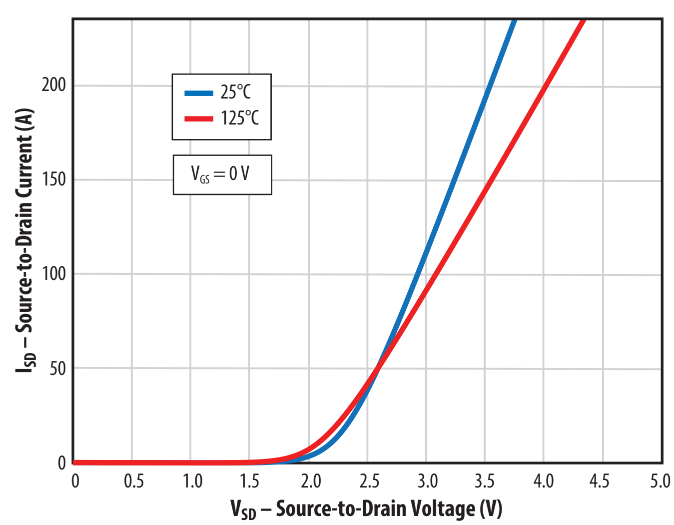


Figure 8: Normalized On-State Resistance vs. Temperature

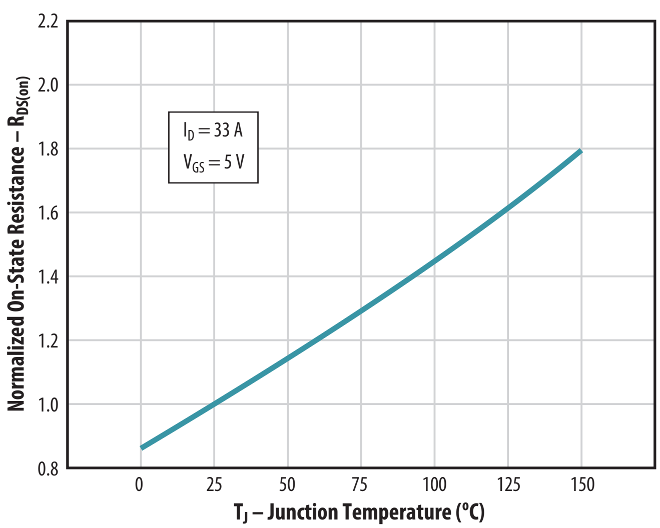
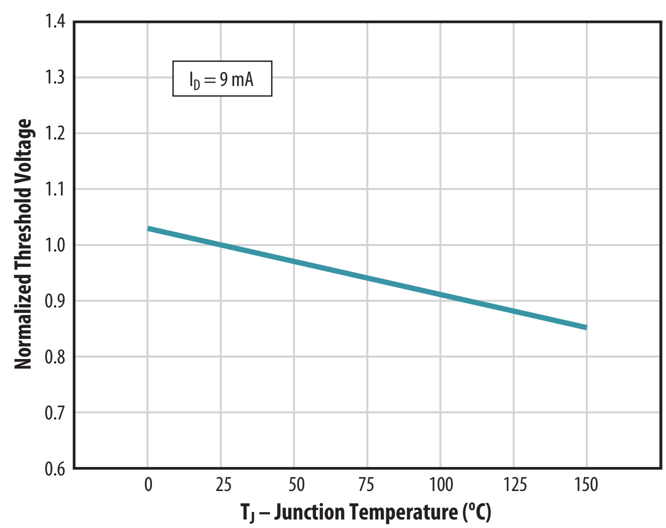


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shortened to source.

Figure 10: Gate Leakage Current

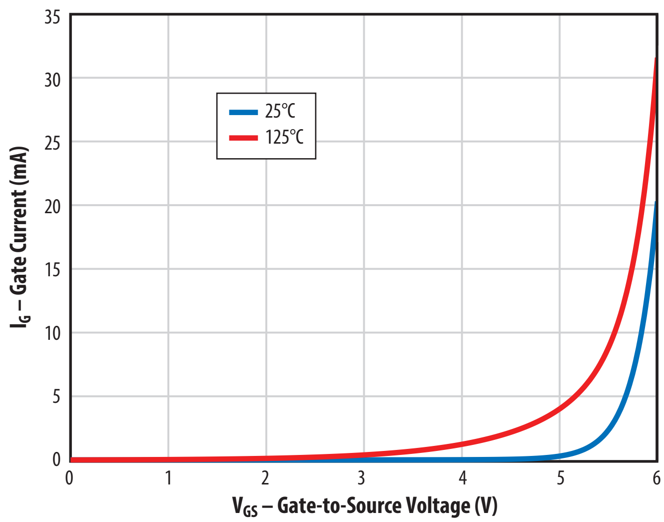
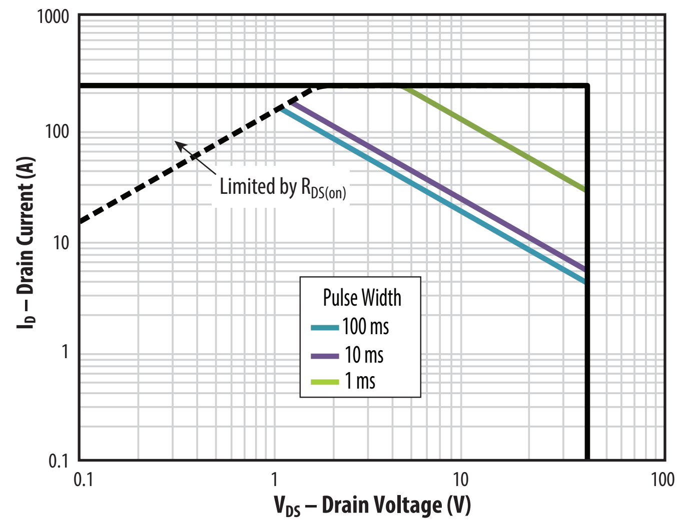


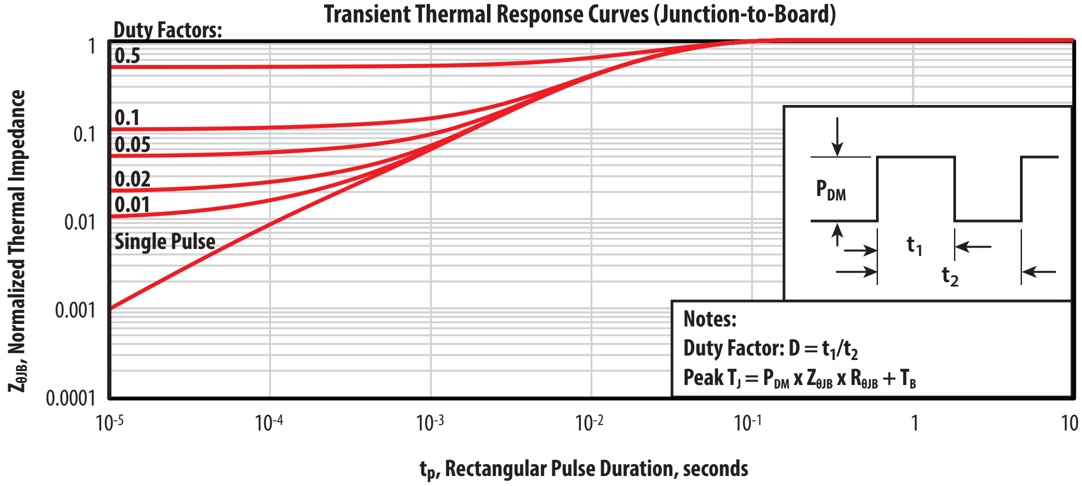
Figure 11: Safe Operating Area



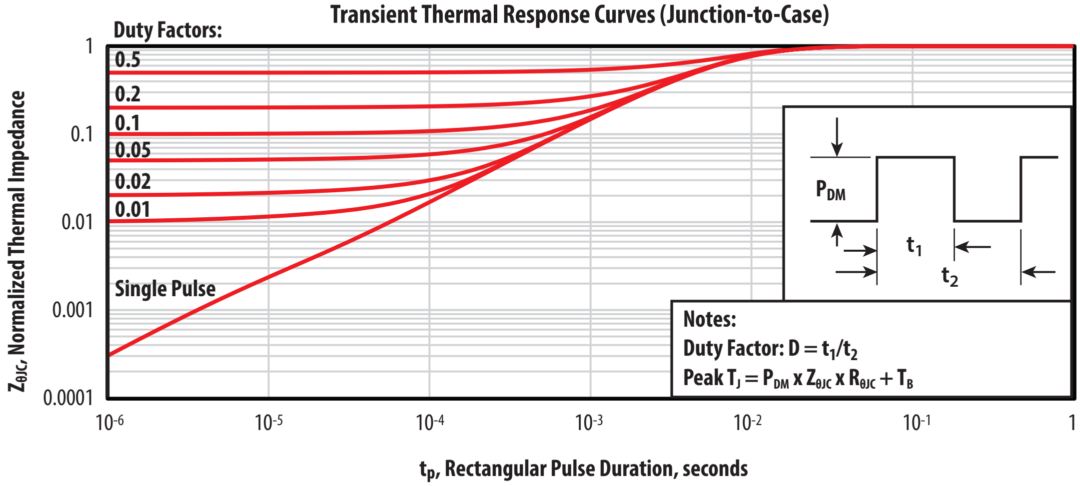
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Transient Thermal Response Curves

Transient Thermal Response Curves (Junction-to-Board)

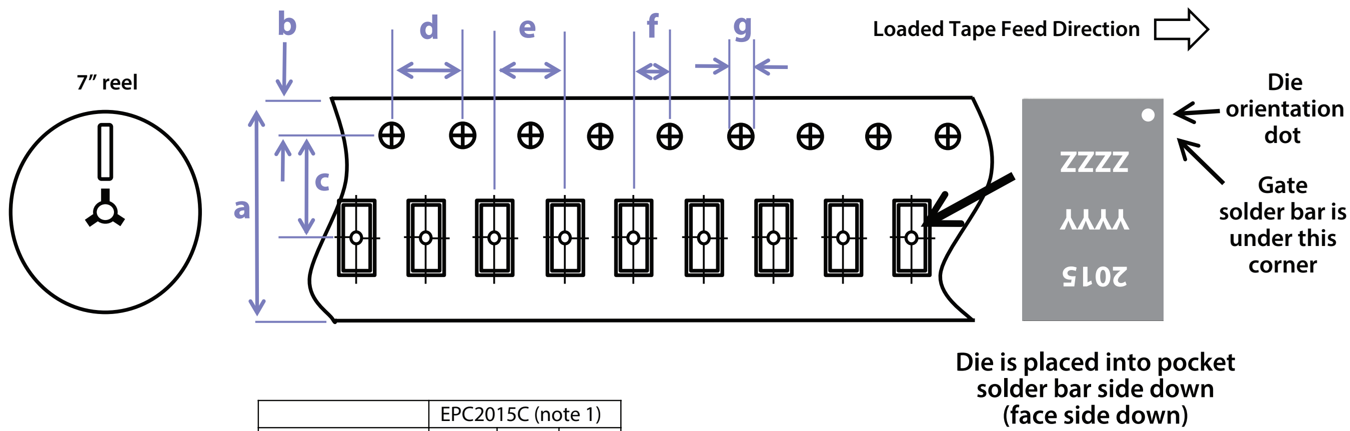


Transient Thermal Response Curves (Junction-to-Case)



TAPE AND REEL CONFIGURATION

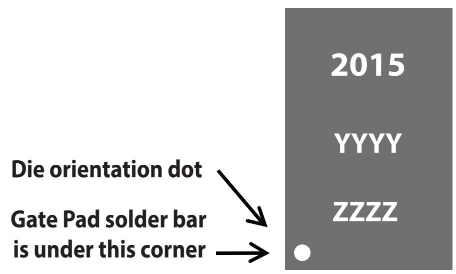
4mm pitch, 12mm wide tape on 7" reel



	EPC2015C (note 1)		
Dimension (mm)	target	min	max
a	12.0	11.7	12.3
b	1.75	1.65	1.85
c (note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

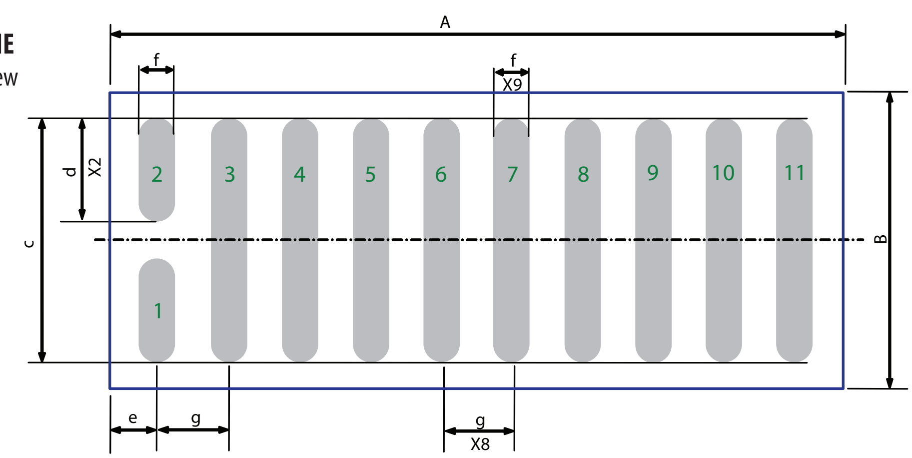
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2015C	2015	YYYY	ZZZZ

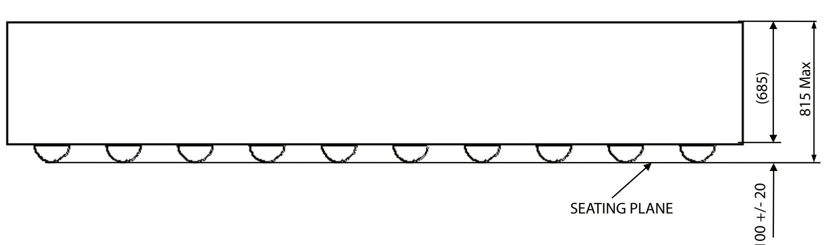
DIE OUTLINE

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

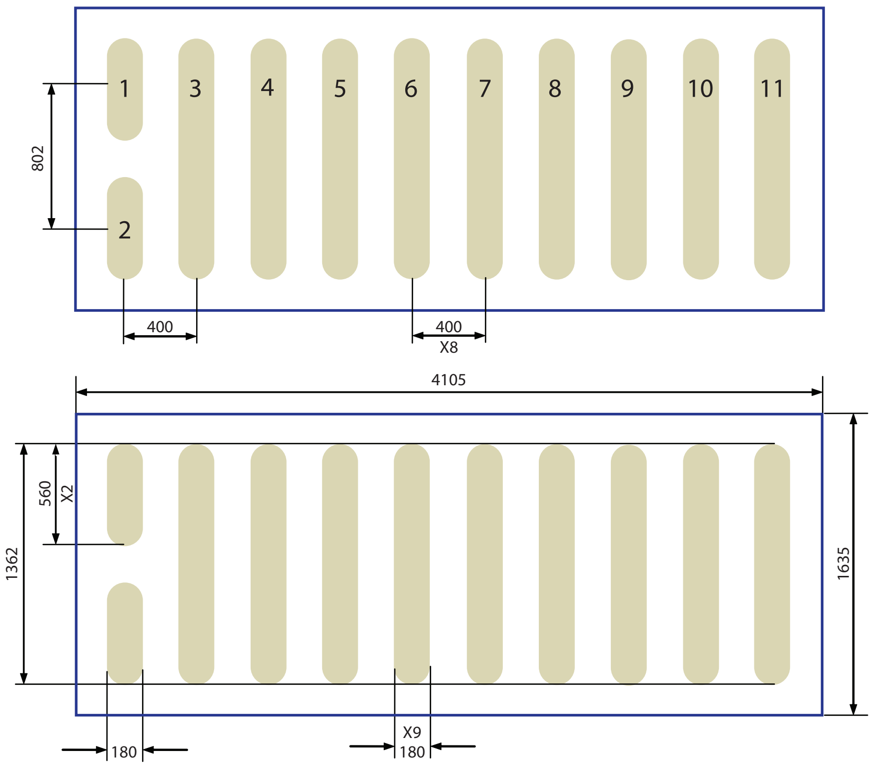
Side View



RECOMMENDED LAND PATTERN

(measurements in µm)

The land pattern is solder mask defined.



Pad no. 1 is Gate;

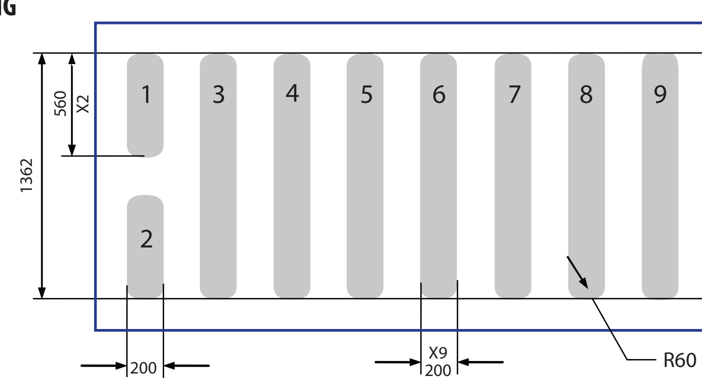
Pads no. 3, 5, 7, 9, 11 are Drain;

Pads no. 4, 6, 8, 10 are Source;

Pad no. 2 is Substrate.

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx