Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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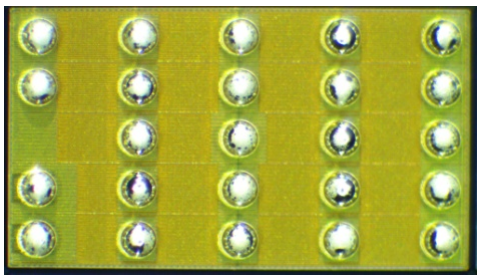
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

EPC2030 – Enhancement Mode Power Transistor
Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS}, 40 V
- Maximum $R_{DS(on)}$, 2.4 mΩ
- I_D, 31 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2030 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 2.6 mm x 4.6 mm

Applications:

- High Frequency DC-DC Conversion
- Motor Drive
- Industrial Automation
- Synchronous Rectification
- Inrush Protection
- Point-of-Load (POL) Converters

MAXIMUM RATINGS

Parameter		Value
V_{DS}	Maximum Drain – Source Voltage	40 V
V_{GS}	Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
I_D	Continuous Drain Current, (T_A = 25 °C, $R_{\theta JA}$ = 30 °C/W)	31 A
	Maximum Pulsed Drain Current, 25 °C, T_{pulse} = 300 µs	495 A
T_J	Optimum Temperature Range	-40 °C < T_J < 150 °C

STATIC CHARACTERISTICS

Parameter		Conditions	Value
I_{DSS}	Maximum Drain – Source Leakage	V_{DS} = 32 V, V_{GS} = 0 V	0.9 mA
$R_{DS(on)}$	Maximum Drain-Source On Resistance	V_{GS} = 5 V, I_D = 30 A	2.4 mΩ
	Typical Drain-Source On Resistance	V_{GS} = 5 V, I_D = 30 A	1.8 mΩ
$V_{GS(th)}$	Gate – Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 16 mA	0.8 V < $V_{GS(TH)}$ < 2.5 V
I_{GSS}	Gate – Source Maximum Positive Leakage	V_{GS} = 5 V	9 mA
	Gate – Source Maximum Negative Leakage	V_{GS} = -4 V	-0.9 mA

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source

DYNAMIC CHARACTERISTICS

Parameter		Conditions	Typical Value
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V	1900 pF
C_{OSS}	Output Capacitance		1500 pF
C_{RSS}	Reverse Transfer Capacitance		70 pF
R_G	Gate Resistance		0.4 Ω
Q_G	Total Gate Charge	V_{DS} = 20 V, I_D = 30 A, V_{GS} = 5 V	18 nC
Q_{GS}	Gate to Source Charge	V_{DS} = 20 V, I_D = 30 A	5.2 nC
Q_{GD}	Gate to Drain Charge		3.4 nC
$Q_{G(th)}$	Gate Charge at Threshold		3.5 nC
Q_{OSS}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V	41 nC
Q_{RR}	Source-Drain Recovery Charge		0

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source

THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	3.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	45	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Figure 1: Typical Output Characteristics at 25°C

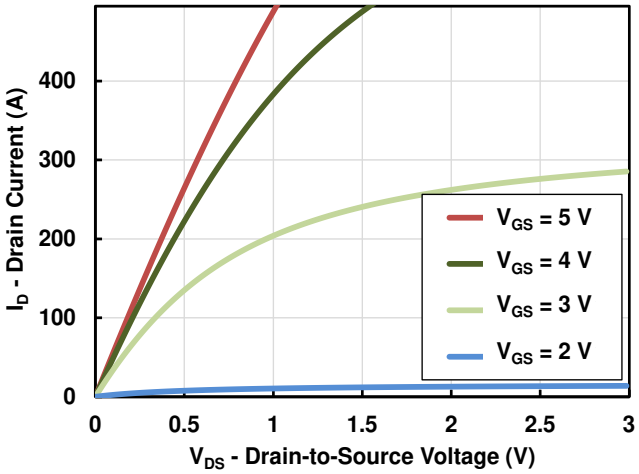


Figure 2: Transfer Characteristics

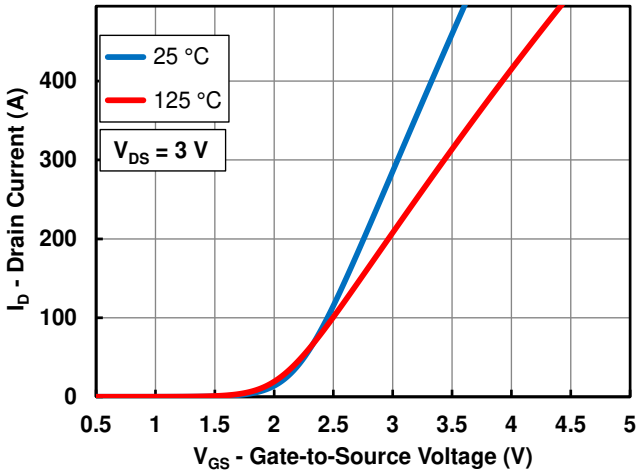


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

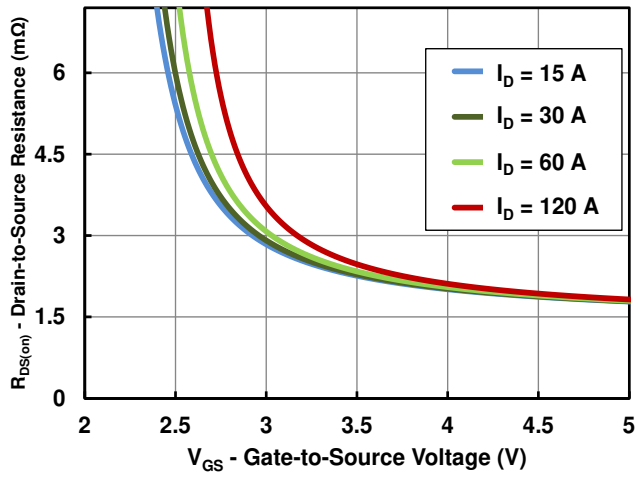


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Drain Temperatures

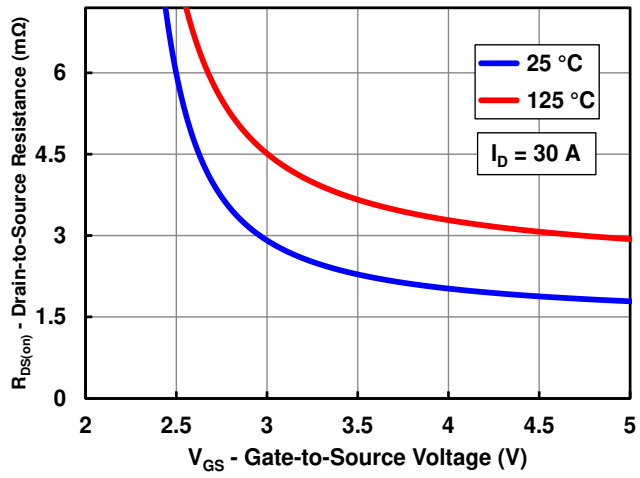


Figure 5a: Capacitance (Linear Scale)

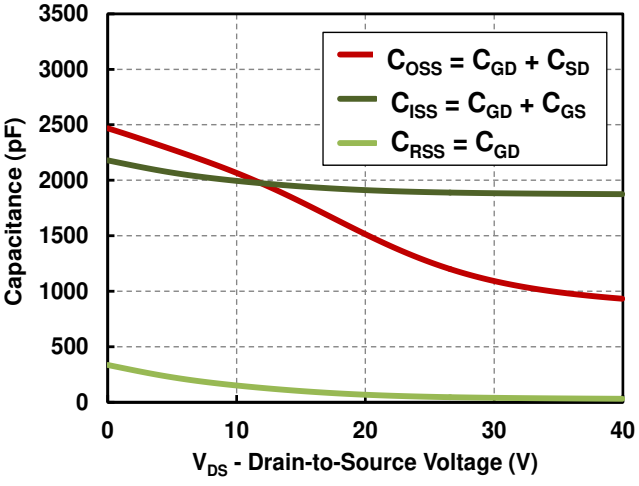


Figure 5b: Capacitance (Log Scale)

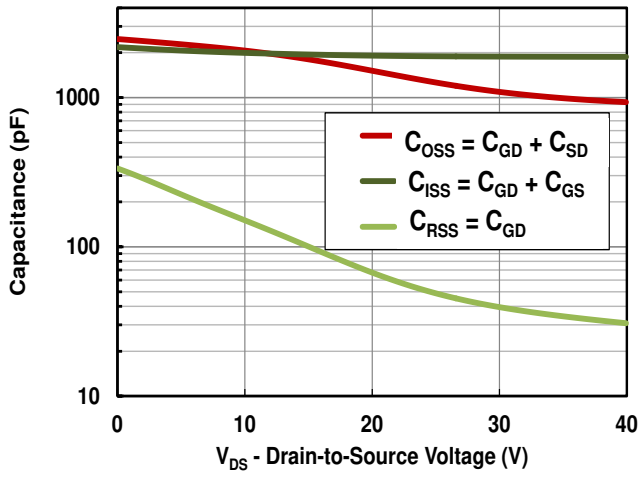


Figure 6: Gate Charge

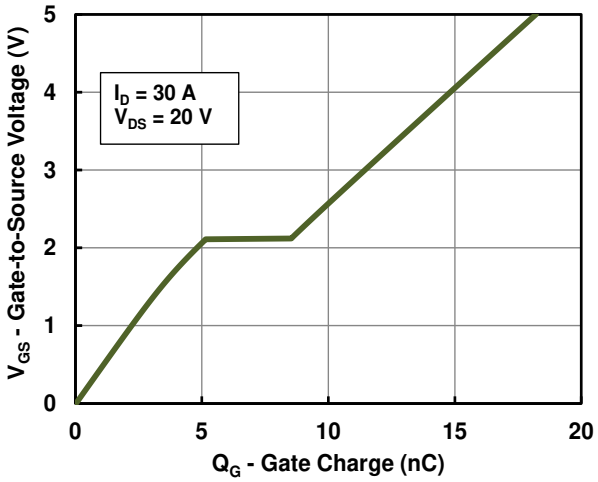


Figure 7: Reverse Drain-Source Characteristics

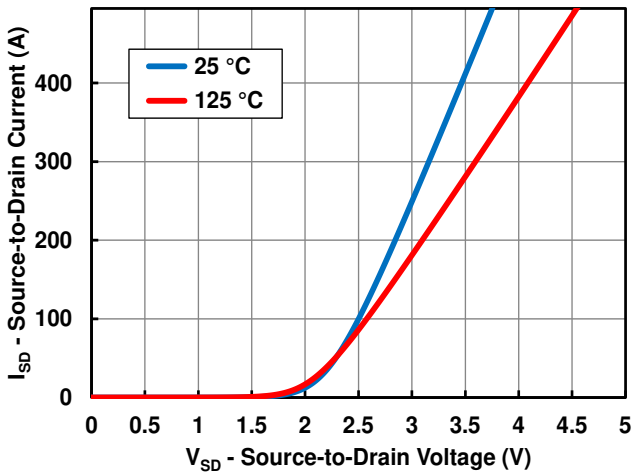


Figure 8: Normalized On Resistance vs. Temperature

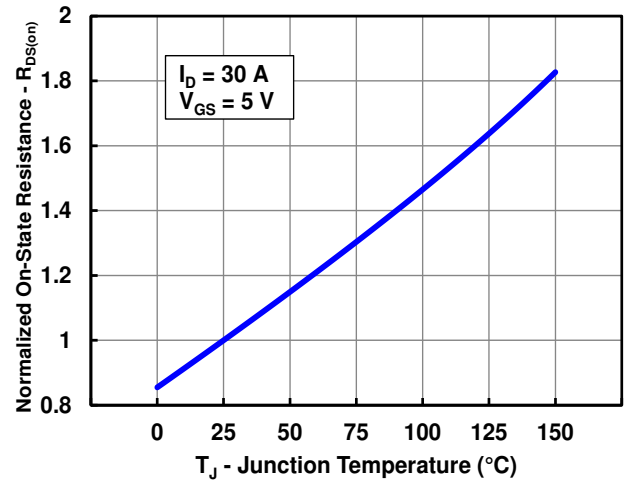


Figure 9: Normalized Threshold Voltage vs. Temperature

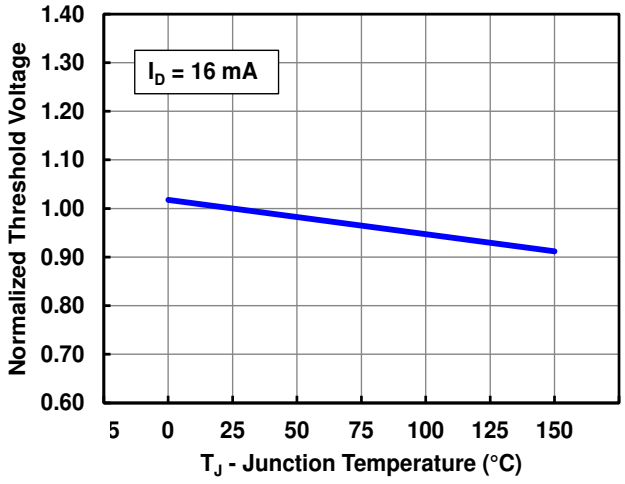
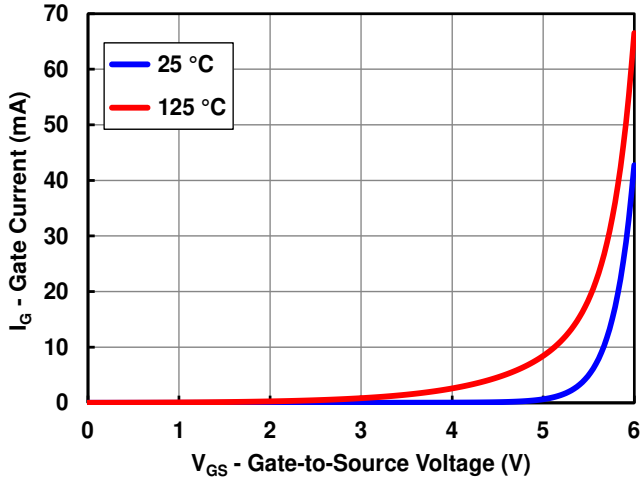


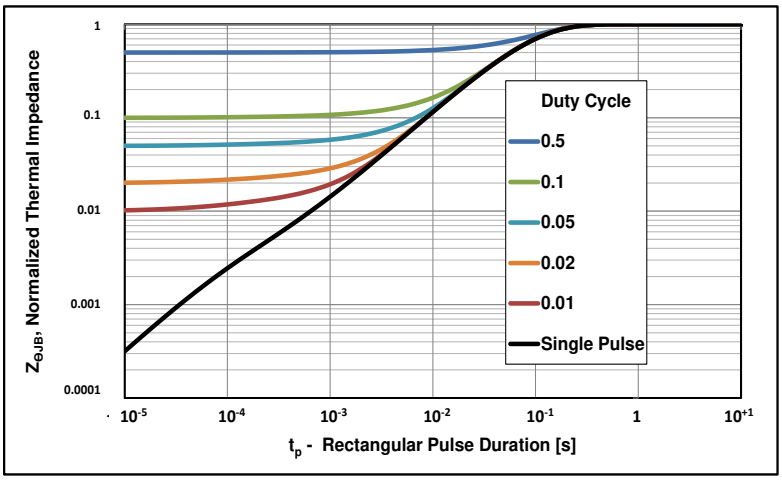
Figure 10: Gate Current

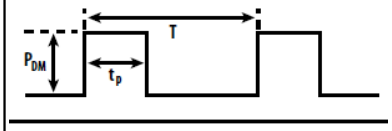


All measurements were done with substrate shorted to source

Figure 11: Transient Thermal Response Curves

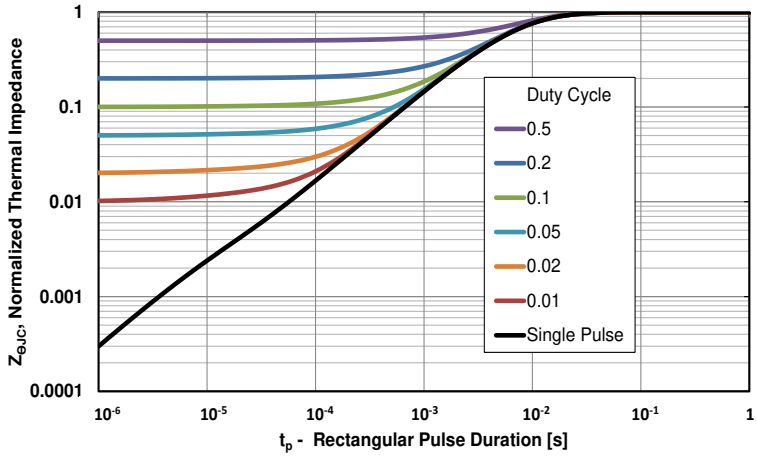
Junction-to-Board

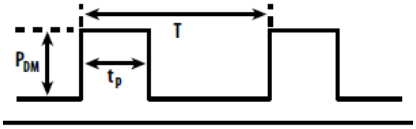




Notes:
Duty Factor = t_p/T
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

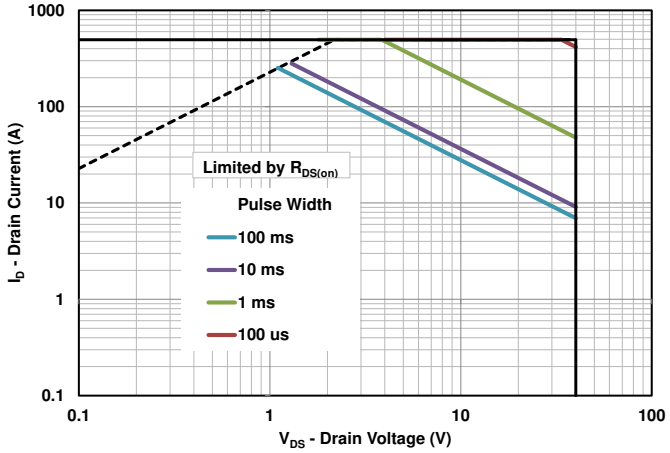
Junction-to-Case





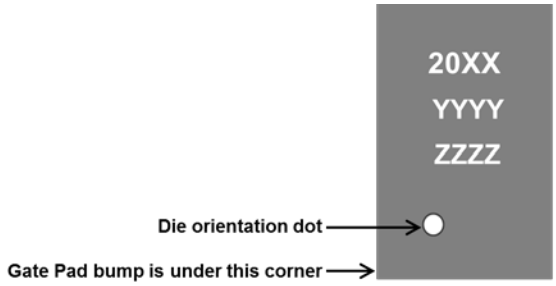
Notes:
Duty Factor = t_p/T
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25˚C, Single Pulse

DIE MARKINGS

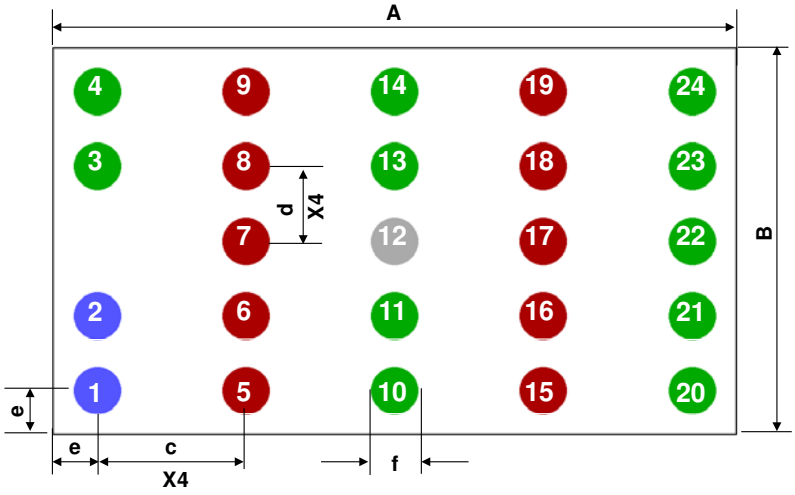


Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2030ENGR	20XX	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View

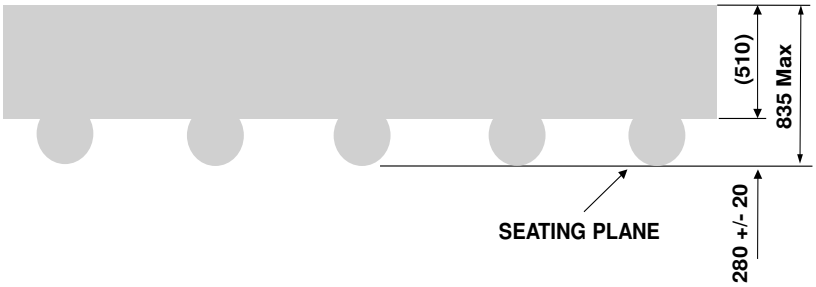
All measurements in micrometers (µm)



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4570	4600	4630
B	2570	2600	2630
c	1000	1000	1000
d	500	500	500
e	285	300	315
f	332	369	406

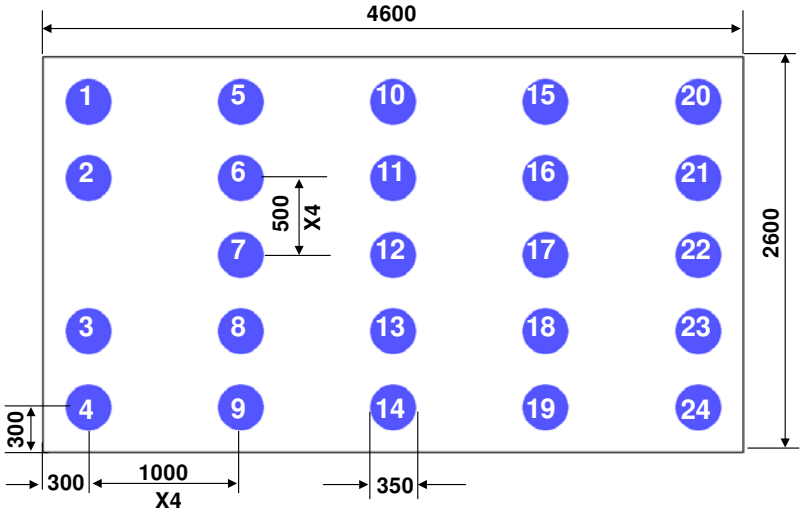
Pads 1 and 2 are Gate;
Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;
Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;
Pad 12 is Substrate.

Side View



RECOMMENDED LAND PATTERN

(*Units in µm)*

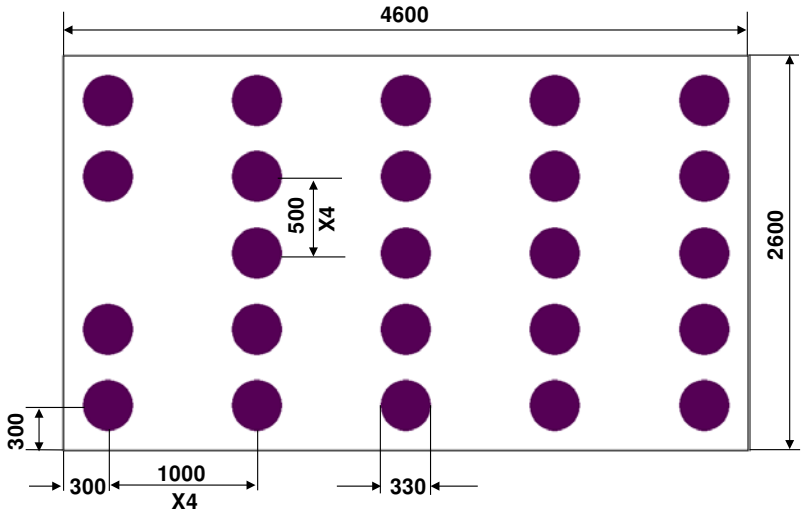


Pads 1 and 2 are Gate;
Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;
Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;
Pad 12 is Substrate.

Land pattern is solder mask defined
Solder mask opening is 350 µm
It is recommended to have on-Cu trace PCB vias
It is recommended to connect the substrate pin to source pin on the PCB in most high frequency switching applications

RECOMMENDED STENCIL

(*Units in µm)*



Recommended stencil should be 4mil (100 µm) thick, must be laser cut, openings per drawing.

For assembly recommendations please visit www.epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised December, 2015