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EPC2110 – Dual Common-Source Enhancement-Mode GaN Power Transistor

V_{DS} , 120 V
$R_{DS(on)}$, 110 mΩ
I_D , 3.4 A

EFFICIENT POWER CONVERSION

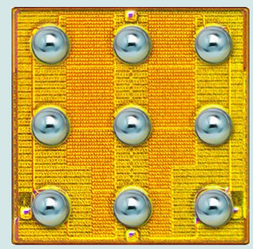
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings of Q1 & Q2			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	120	V
I_D	Continuous (T_A = 25°C, $R_{θJA}$ = 52°C/W)	3.4	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	20	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	–4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics of Q1 & Q2			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	3	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	25	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details



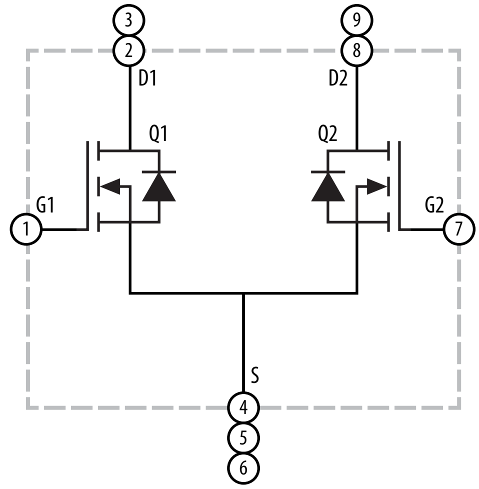
EPC2110 eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 1.35 mm x 1.35 mm

Applications
- Ultra High Frequency DC-DC Conversion
- Wireless Power Transfer
- Synchronous Rectification

Benefits
- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNFETsandICs/EPC2110.aspx

Static Characteristics of Q1 & Q2 (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.3 mA	120			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 96 V, V_{GS} = 0 V		0.01	0.25	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.05	1	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.01	0.25	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.7 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 4 A		80	110	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.9		V



EPC2110 – Detailed Schematic

Note: The EPC2110 can be connected in parallel or used as independent FETs with common source.

Dynamic Characteristics of Q1 & Q2 (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 60 V, V_{GS} = 0 V		85	100	pF
C_{RSS}	Reverse Transfer Capacitance			1		
C_{OSS}	Output Capacitance			45	70	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 60 V, V_{GS} = 0 V		54		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			67		
R_G	Gate Resistance			0.6		Ω
Q_G	Total Gate Charge	V_{DS} = 60 V, V_{GS} = 5 V, I_D = 4 A		0.8	1.1	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 60 V, I_D = 4 A		0.25		
Q_{GD}	Gate to Drain Charge			0.18		
$Q_{G(TH)}$	Gate Charge at Threshold			0.16		
Q_{OSS}	Output Charge	V_{DS} = 60 V, V_{GS} = 0 V		4	6	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1 (Q1 & Q2): Typical Output Characteristics at 25°C

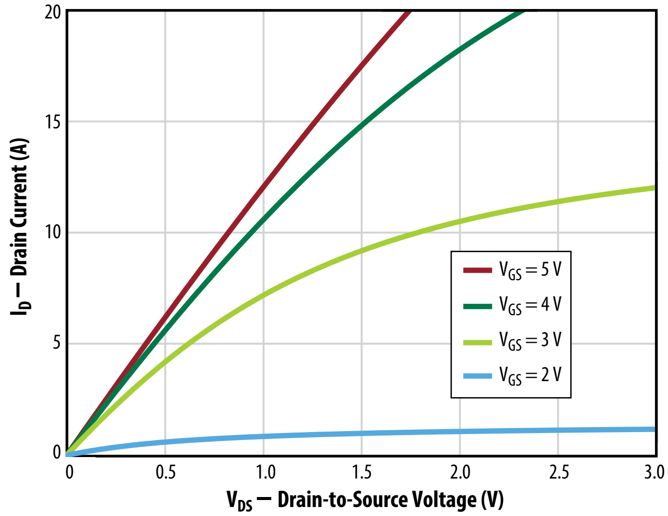


Figure 2 (Q1 & Q2): Transfer Characteristics

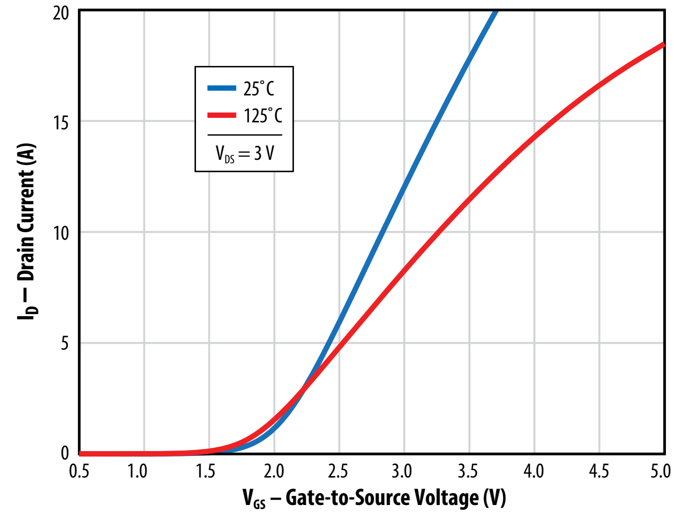


Figure 3 (Q1 & Q2): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

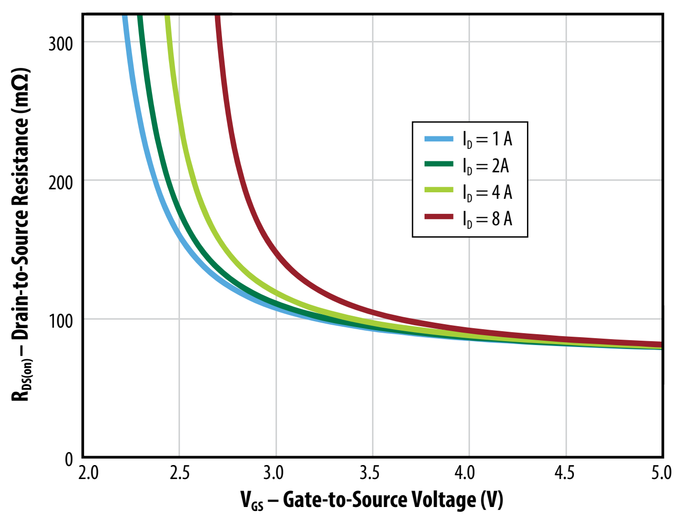


Figure 4 (Q1 & Q2): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

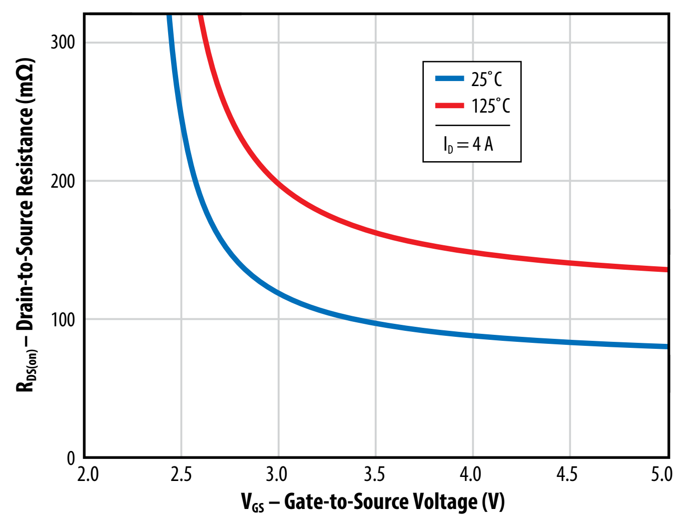


Figure 5a (Q1 & Q2): Capacitance (Linear Scale)

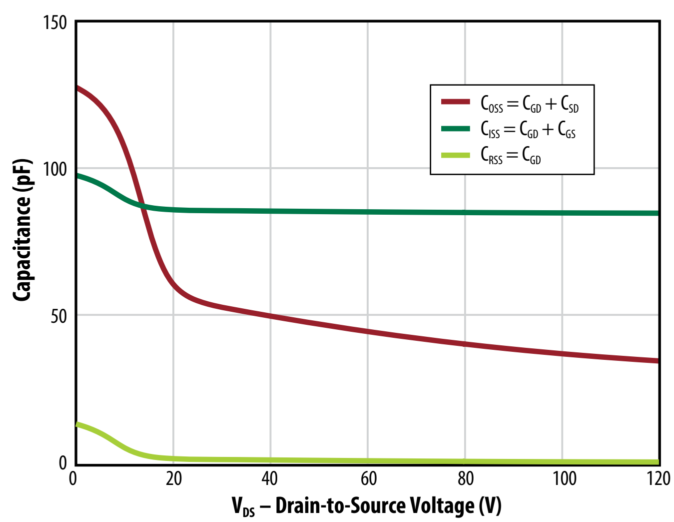


Figure 5b (Q1 & Q2): Capacitance (Log Scale)

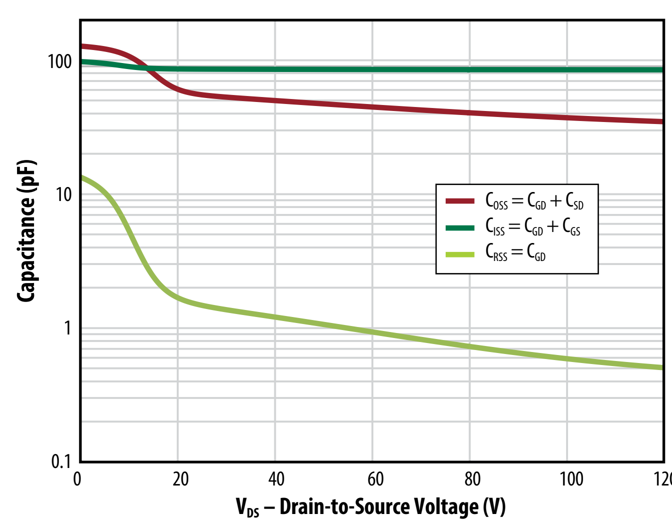


Figure 6 (Q1 & Q2): Output Charge and C_{OSS} Stored Energy

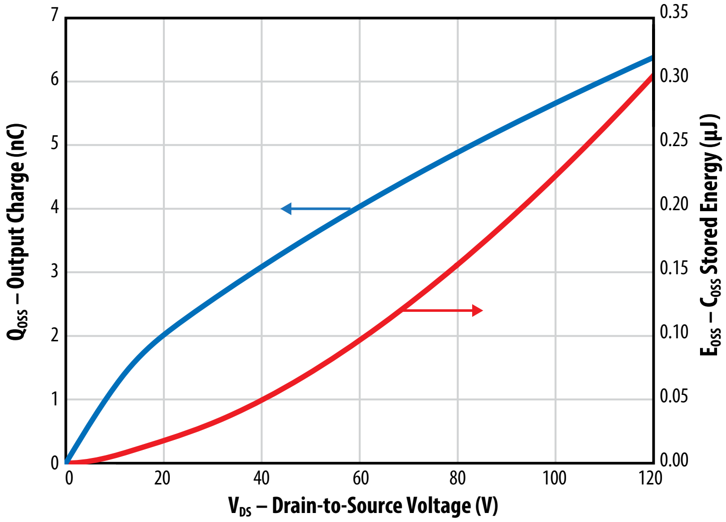


Figure 7 (Q1 & Q2): Gate Charge

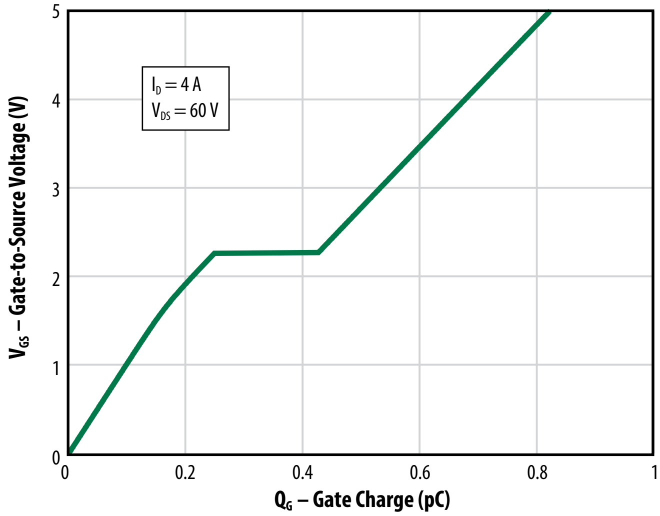


Figure 8: Reverse Drain-Source Characteristics

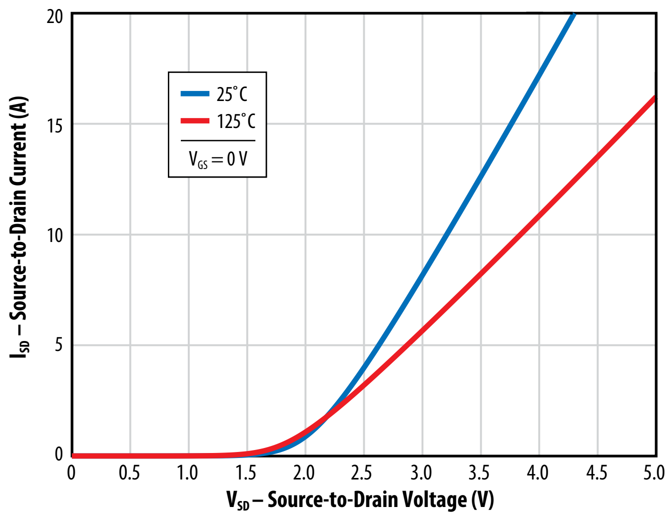


Figure 9 (Q1 & Q2):
Normalized On-State Resistance vs. Temperature

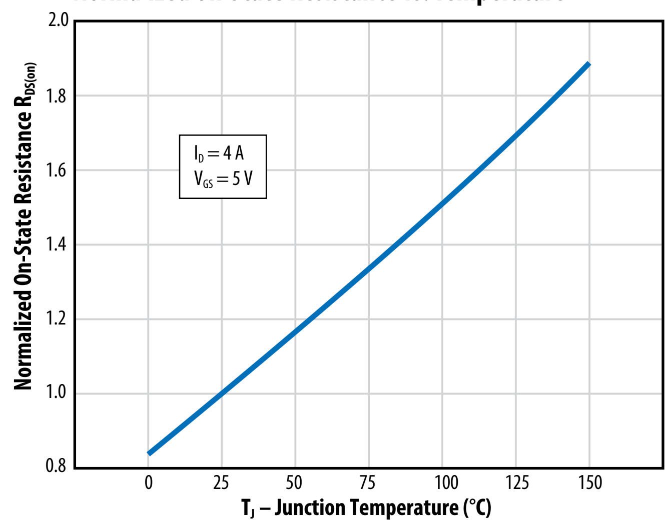


Figure 10 (Q1 & Q2):
Normalized Threshold Voltage vs. Temperature

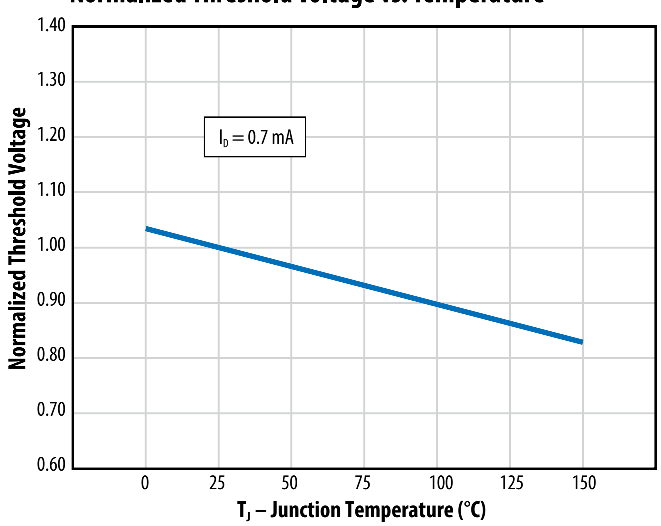


Figure 11a (Q1 & Q2): Transient Thermal Response Curves (Junction-to-Board)

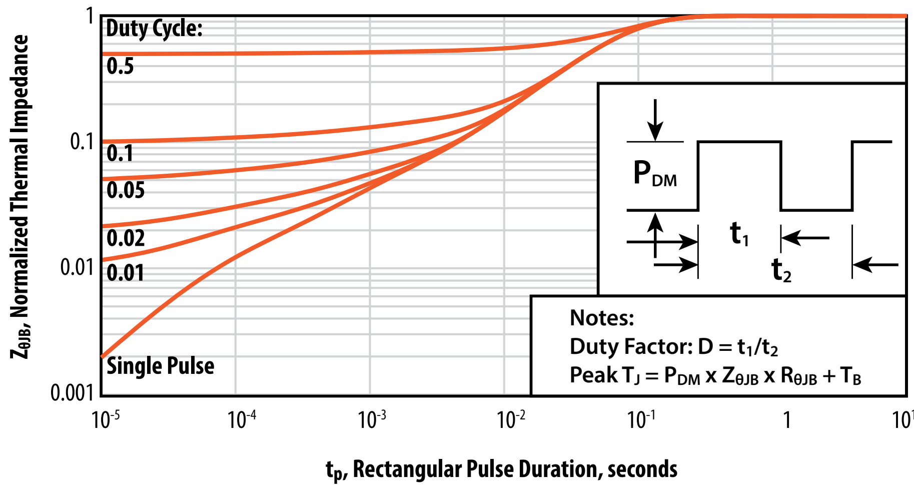


Figure 11b (Q1 & Q2): Transient Thermal Response Curves (Junction-to-Case)

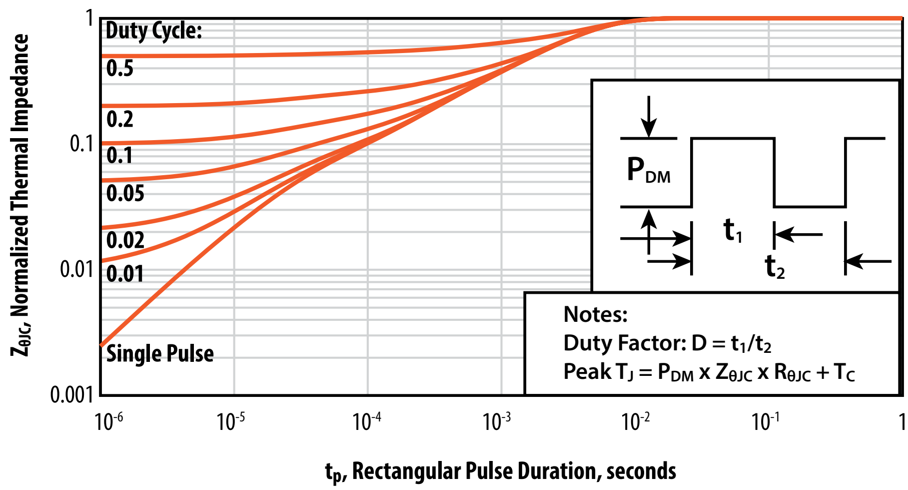
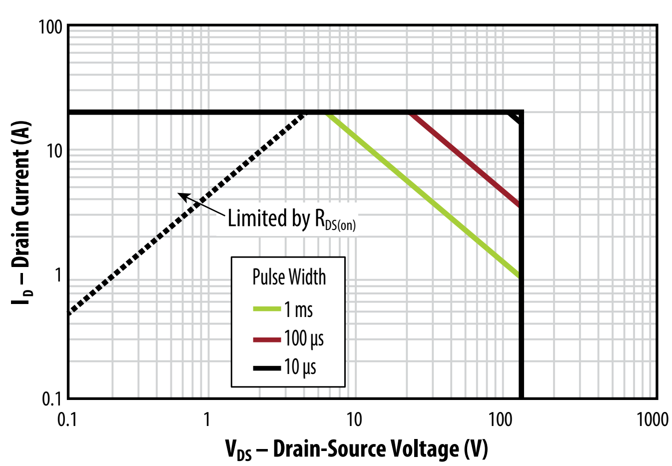


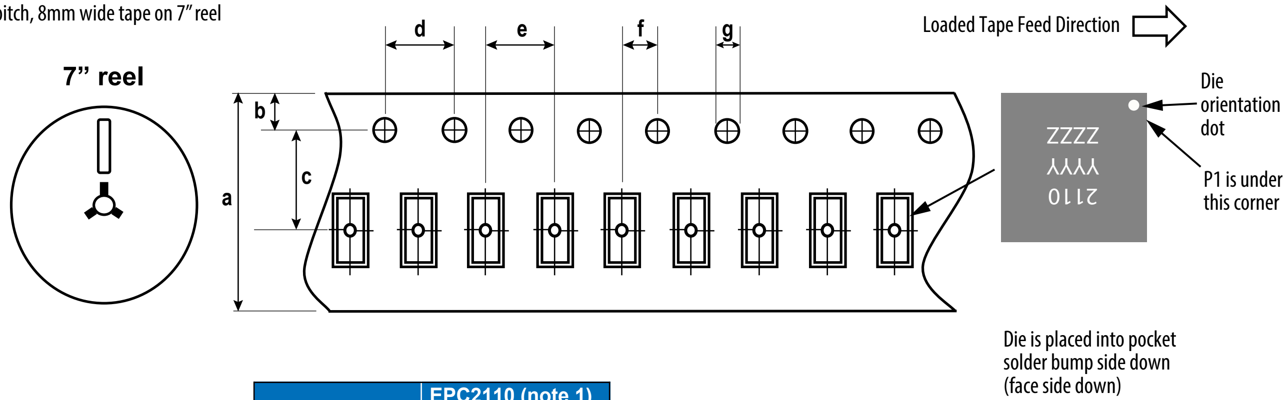
Figure 12 (Q1 & Q2): Safe Operating Area



T_J = Max rated, T_C = +25°C, Single pulse

TAPE AND REEL CONFIGURATION

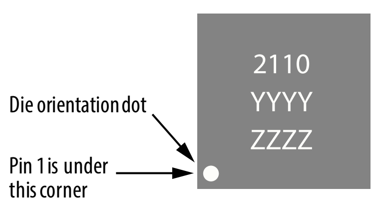
4mm pitch, 8mm wide tape on 7" reel



	EPC2110 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

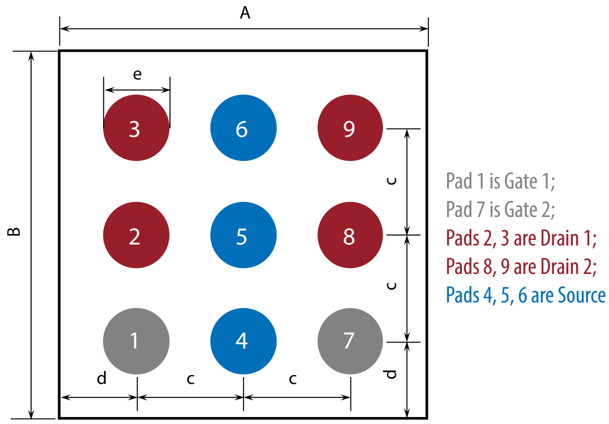
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2110	2110	YYYY	ZZZZ

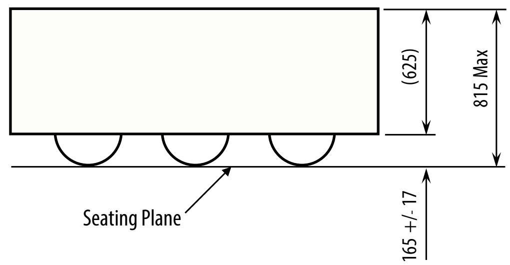
DIE OUTLINE

Solder Bump View



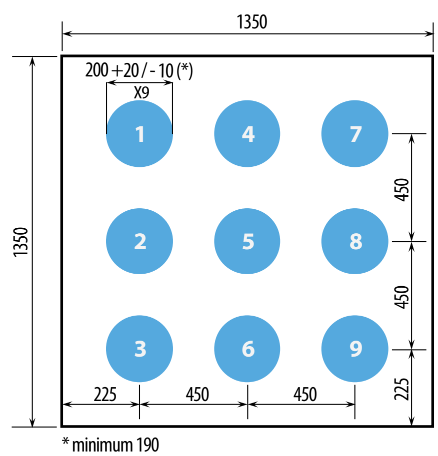
DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c	450	450	450
d	210	225	240
e	187	208	229

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)

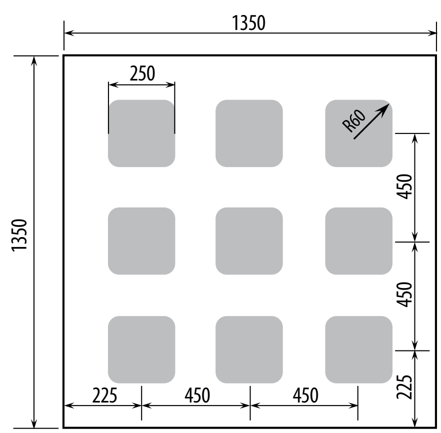


The land pattern is solder mask defined

Solder mask is 10 µm smaller per side than bump

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx