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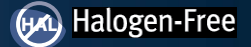


EPC2111 – Enhancement-Mode GaN Power Transistor Half-Bridge

V_{DS} , 30 V

$R_{DS(on)}$, 19 mΩ (Q1), 8 mΩ (Q2)

I_D , 16 A (Q1), 16 A (Q2)

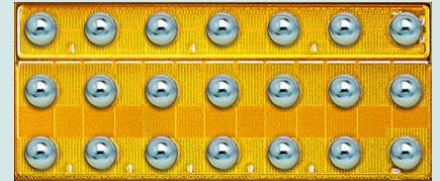


Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings				
DEVICE	PARAMETER		VALUE	UNIT
Q1	V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	36	
	I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 15^\circ\text{C/W}$)	16	A
		Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	50	
	V_{GS}	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	-4	
	T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150		
Q2	V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	36	
	I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 36^\circ\text{C/W}$)	16	A
		Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	140	
	V_{GS}	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	-4	
	T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150		

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	6.6	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	58	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details



EPC2111 eGaN® ICs are supplied only in passivated die form with solder bumps
Die Size: 3.5 mm x 1.5 mm

Applications

- High Frequency DC-DC
- Point-of-Load (POL) Converters

Benefits

- High Frequency Operation (up to 10 MHz)
- Low Inductance Package
- High Density Footprint

www.epc-co.com/epc/Products/eGaNfetsandICs/EPC2111.aspx

Static Characteristics

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 0.25 mA	30			V
	I _{DSS}	Drain-Source Leakage	V _{DS} = 24 V, V _{GS} = 0 V		0.002	0.15	mA
	I _{GSS}	Gate-to-Source Forward Leakage	V _{GS} = 5 V		0.004	2	mA
		Gate-to-Source Reverse Leakage	V _{GS} = -4 V		0.002	0.15	mA
	V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 2 mA	0.8	1.4	2.5	V
	R _{DS(on)}	Drain-Source On Resistance	V _{GS} = 5 V, I _D = 15 A		14	19	mΩ
	V _{SD}	Source-Drain Forward Voltage	I _S = 0.5 A, V _{GS} = 0 V		1.8		V
Q2	BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 0.4 mA	30			V
	I _{DSS}	Drain-Source Leakage	V _{DS} = 24 V, V _{GS} = 0 V		0.005	0.3	mA
	I _{GSS}	Gate-to-Source Forward Leakage	V _{GS} = 5 V		0.01	4.5	mA
		Gate-to-Source Reverse Leakage	V _{GS} = -4 V		0.005	0.3	mA
	V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 5 mA	0.8	1.4	2.5	V
	R _{DS(on)}	Drain-Source On Resistance	V _{GS} = 5 V, I _D = 15 A		6	8	mΩ
	V _{SD}	Source-Drain Forward Voltage	I _S = 0.5 A, V _{GS} = 0 V		1.8		V

Dynamic Characteristics

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	C _{ISS}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V		190	230	pF
	C _{RSS}	Reverse Transfer Capacitance			8		
	C _{OSS}	Output Capacitance			170	255	
	C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 15 V, V _{GS} = 0 V		204		pF
	C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			217		
	R _G	Gate Resistance			0.5		
	Q _G	Total Gate Charge	V _{DS} = 15 V, V _{GS} = 5 V, I _D = 15 A		1.7	2.2	nC
	Q _{GS}	Gate-to-Source Charge	V _{DS} = 15 V, I _D = 15 A		0.6		
	Q _{GD}	Gate-to-Drain Charge			0.3		
	Q _{G(TH)}	Gate Charge at Threshold			0.4		
	Q _{OSS}	Output Charge	V _{DS} = 15 V, V _{GS} = 0 V		3.3	5	
Q _{RR}	Source-Drain Recovery Charge			0			
Q2	C _{ISS}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V		495	595	pF
	C _{RSS}	Reverse Transfer Capacitance			21		
	C _{OSS}	Output Capacitance			490	735	
	C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 15 V, V _{GS} = 0 V		590		pF
	C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			637		
	R _G	Gate Resistance			0.4		
	Q _G	Total Gate Charge	V _{DS} = 15 V, V _{GS} = 5 V, I _D = 15 A		4.5	5.8	nC
	Q _{GS}	Gate-to-Source Charge	V _{DS} = 15 V, I _D = 15 A		1.4		
	Q _{GD}	Gate-to-Drain Charge			0.8		
	Q _{G(TH)}	Gate Charge at Threshold			1		
	Q _{OSS}	Output Charge	V _{DS} = 15 V, V _{GS} = 0 V		9.6	15	
Q _{RR}	Source-Drain Recovery Charge			0			

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1a (Q1): Typical Output Characteristics at 25°C

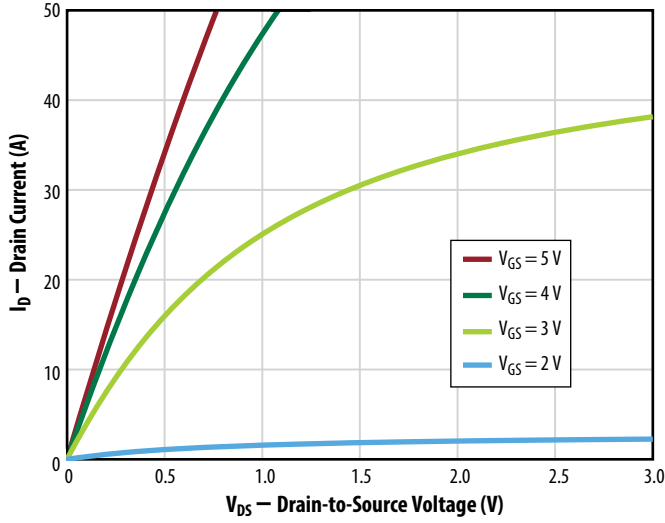


Figure 1b (Q2): Typical Output Characteristics at 25°C

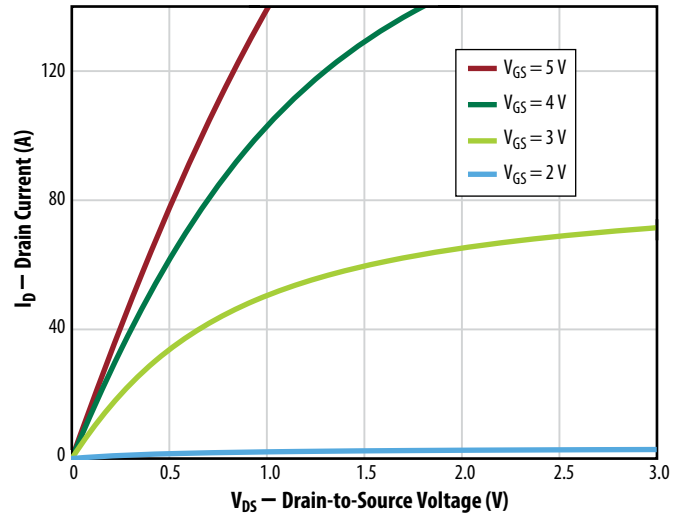


Figure 2a (Q1): Transfer Characteristics

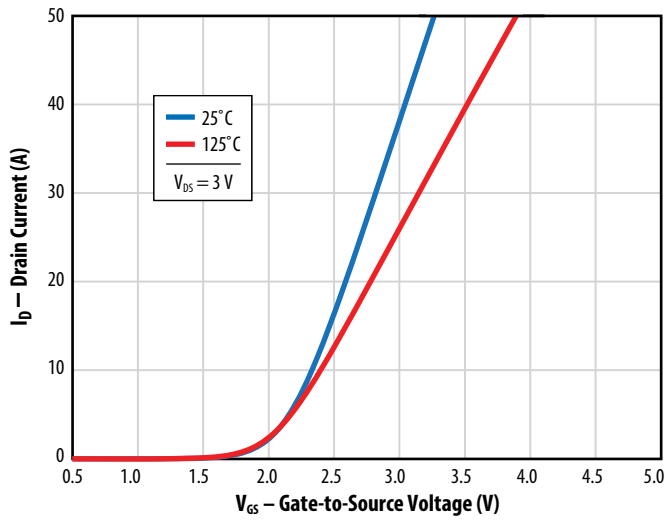


Figure 2b (Q2): Transfer Characteristics

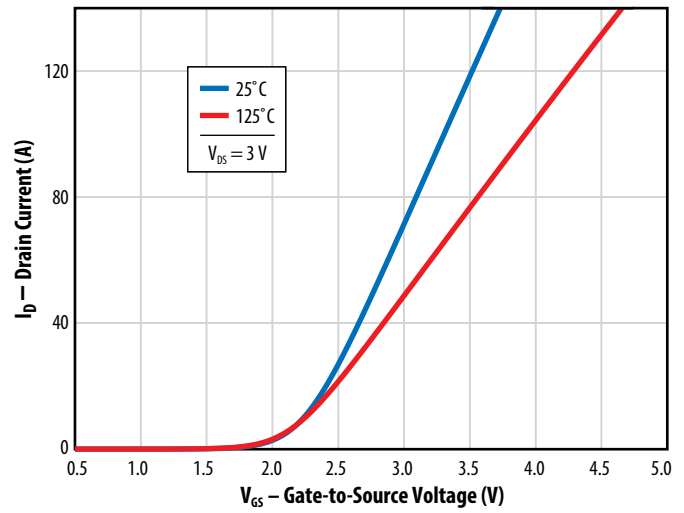


Figure 3a (Q1): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

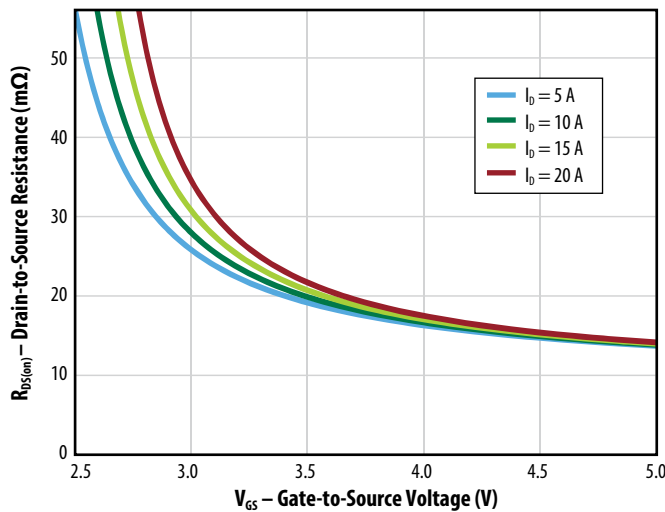


Figure 3b (Q2): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

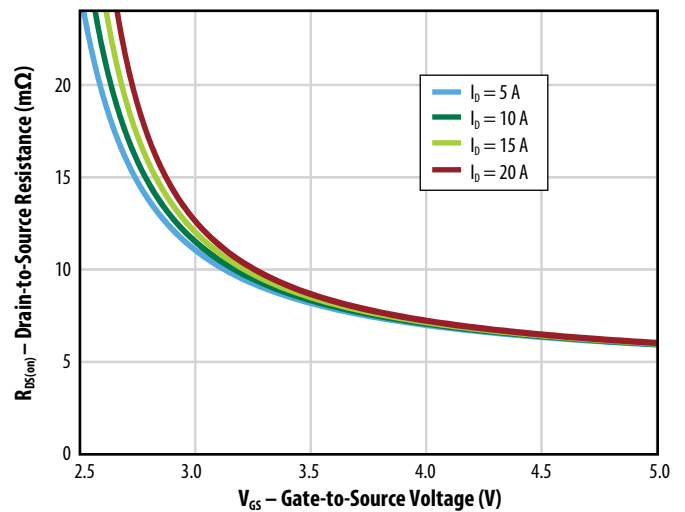


Figure 4a (Q1): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

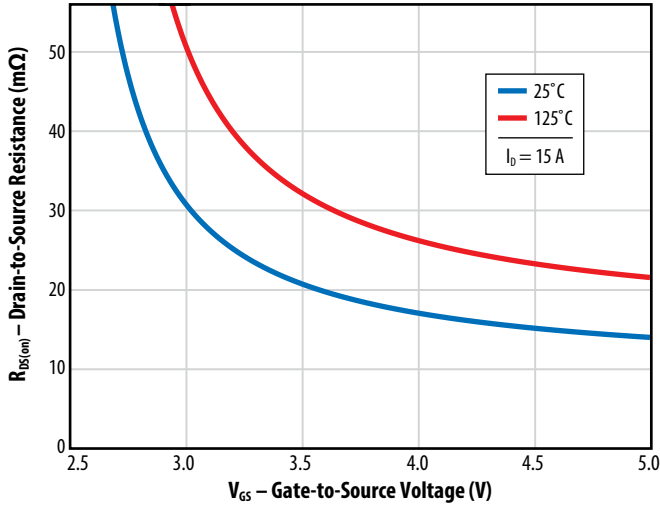


Figure 4b (Q2): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

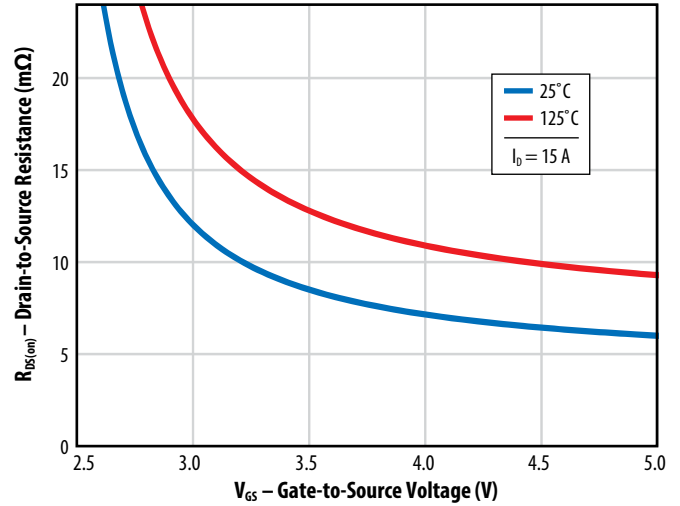


Figure 5a (Q1): Capacitance (Linear Scale)

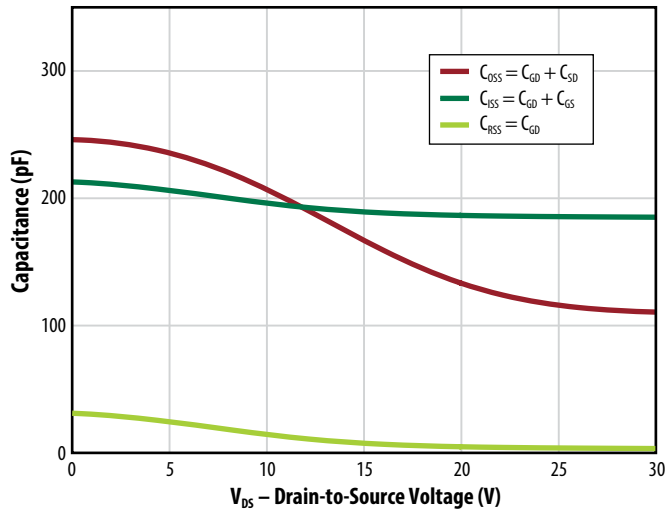


Figure 5b (Q2): Capacitance (Linear Scale)

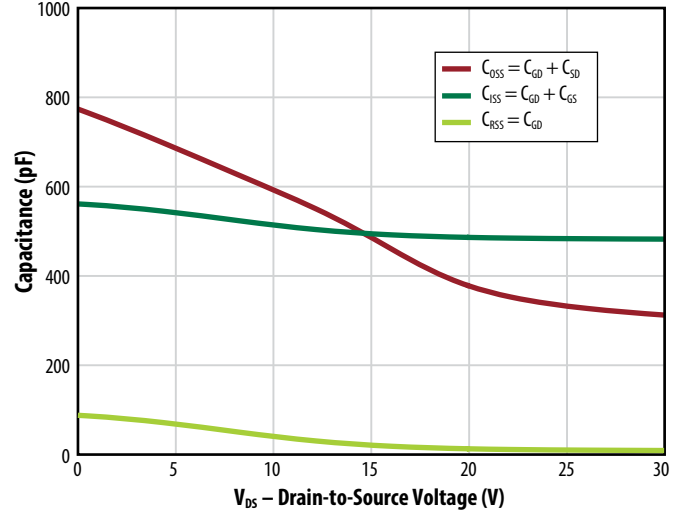


Figure 6a (Q1): Output Charge and C_{OSS} Stored Energy

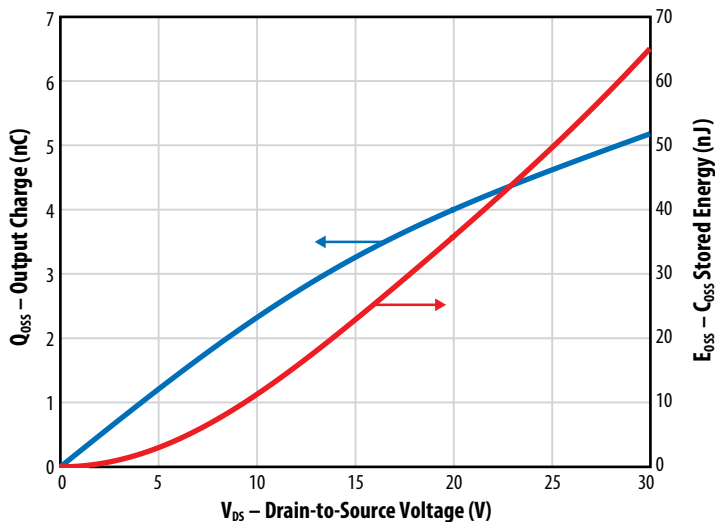


Figure 6b (Q2): Output Charge and C_{OSS} Stored Energy

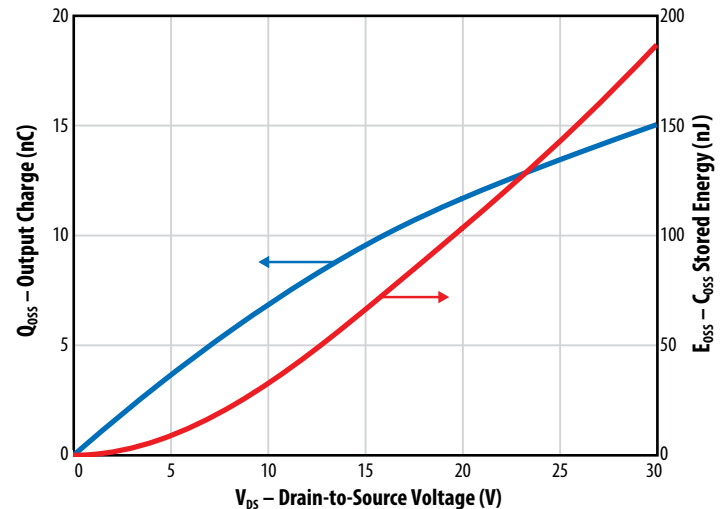


Figure 7a (Q1): Gate Charge

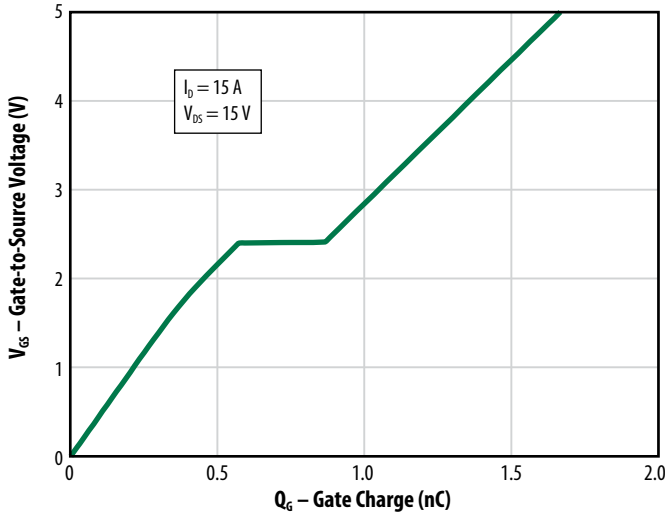


Figure 7b (Q2): Gate Charge

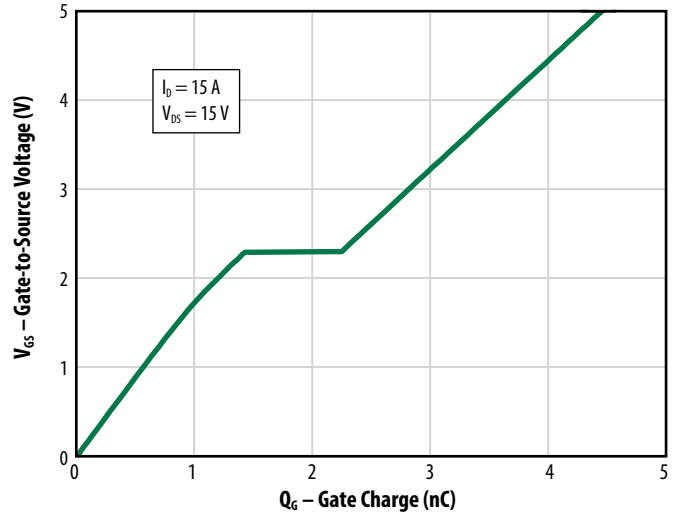


Figure 8a (Q1): Reverse Drain-Source Characteristics

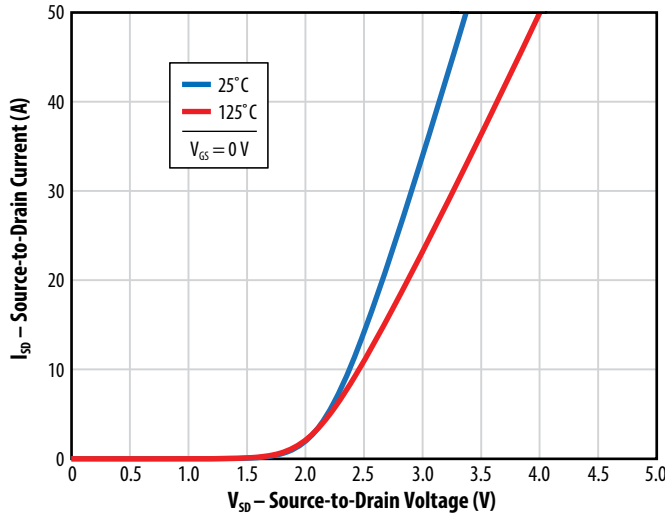


Figure 8b (Q2): Reverse Drain-Source Characteristics

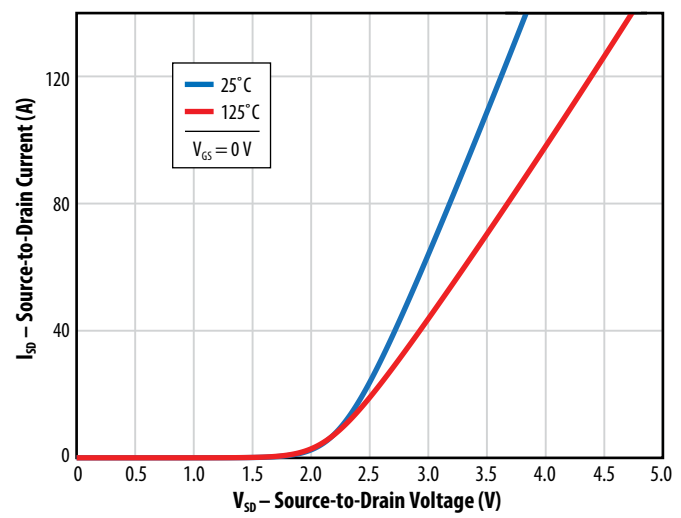


Figure 9a (Q1): Normalized On-State Resistance vs. Temperature

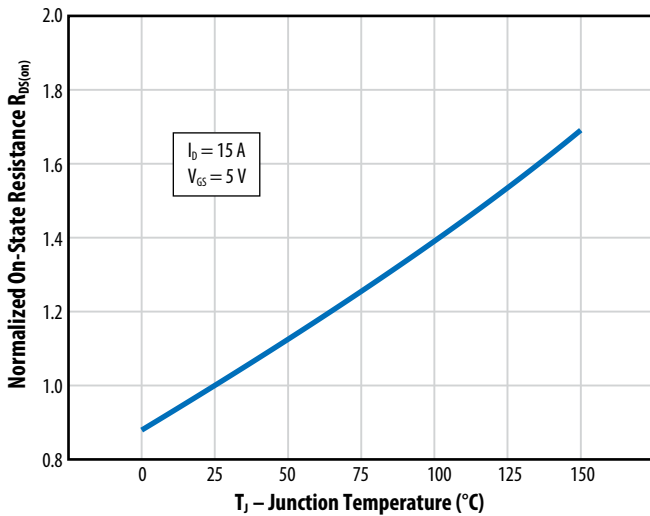


Figure 9b (Q2): Normalized On-State Resistance vs. Temperature

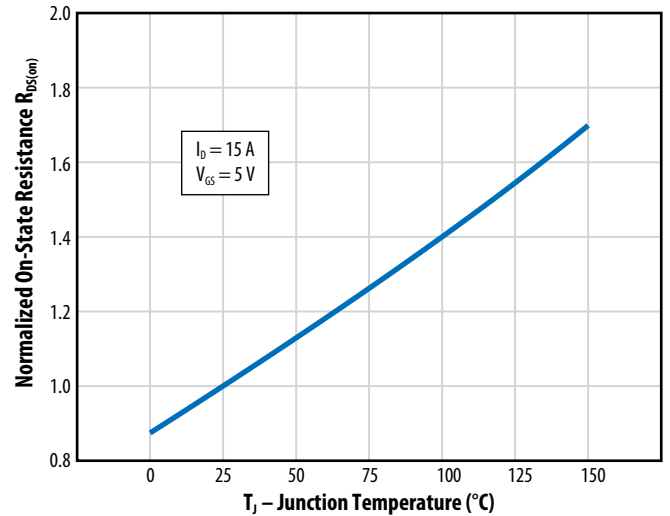


Figure 10a (Q1):
Normalized Threshold Voltage vs. Temperature

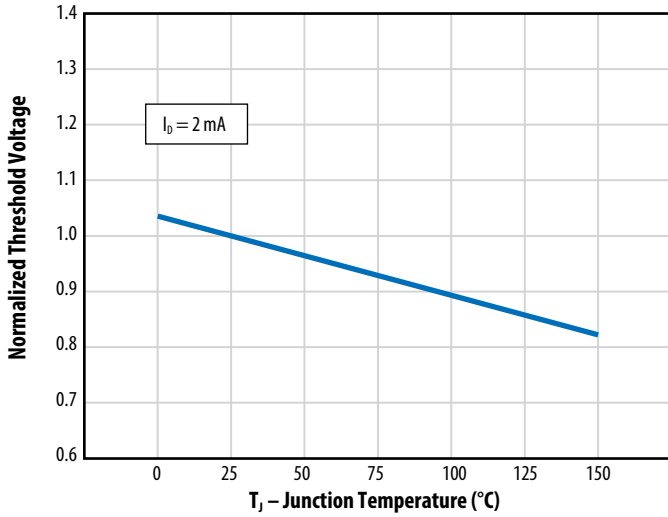


Figure 10b (Q2):
Normalized Threshold Voltage vs. Temperature

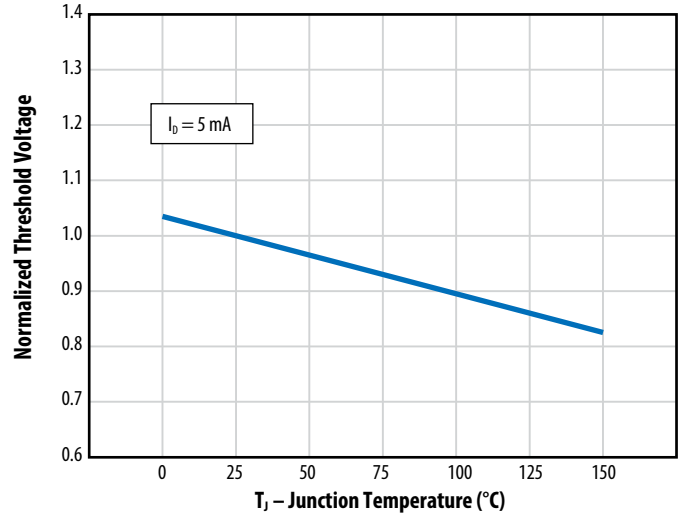


Figure 11a (Q1): Safe Operating Area

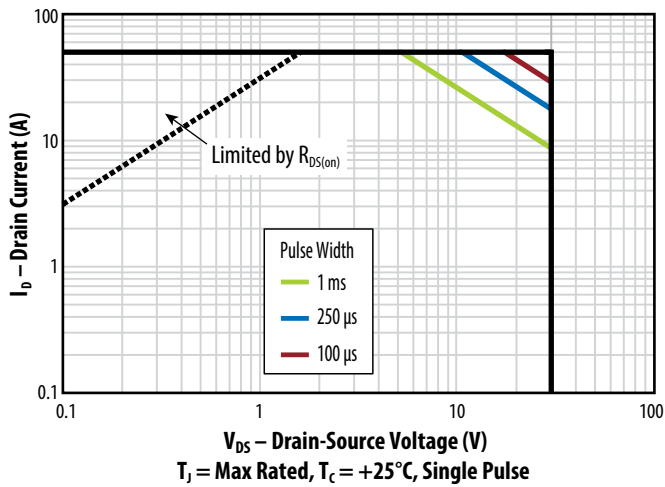


Figure 11b (Q2): Safe Operating Area

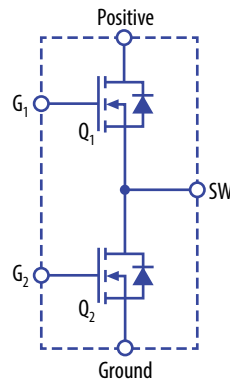
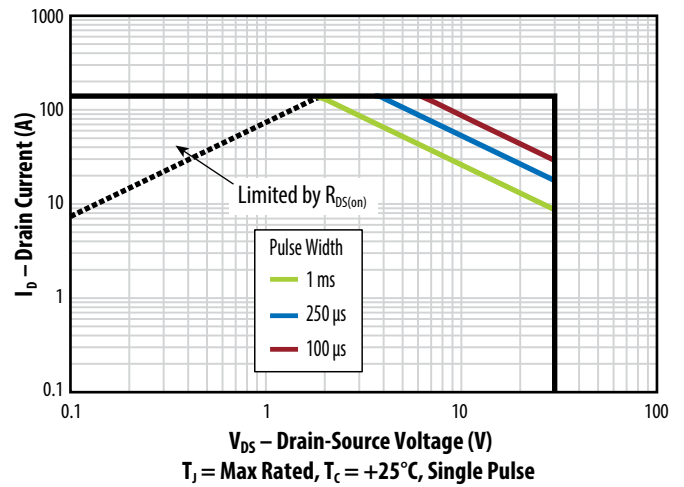


Figure 12
Typical Application Circuit

Figure 13a
Transient Thermal
Response Curves

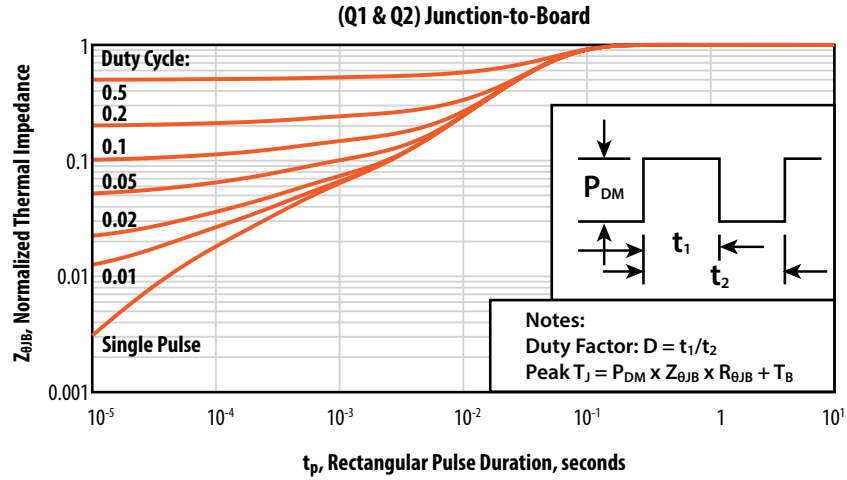
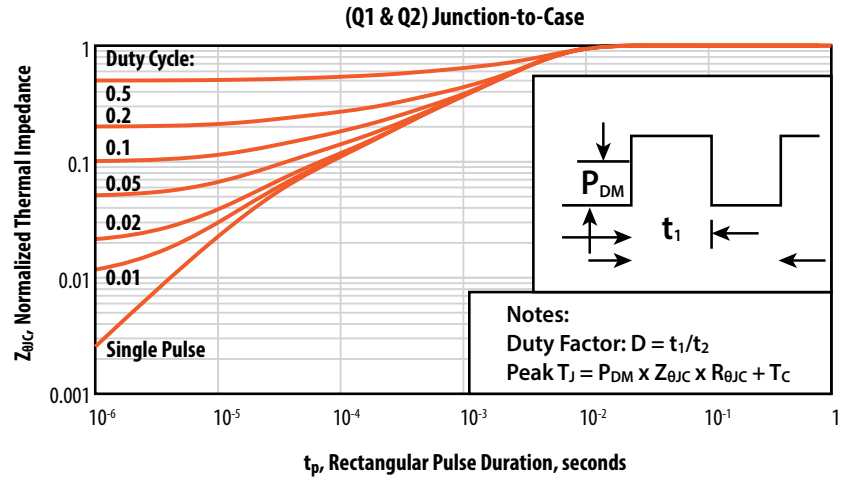
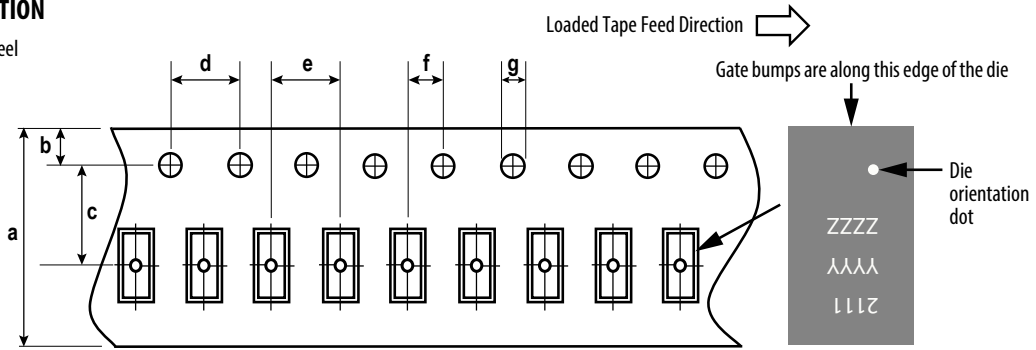
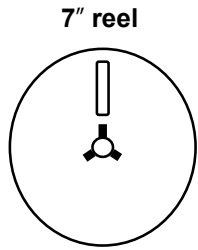


Figure 13b
Transient Thermal
Response Curves



TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

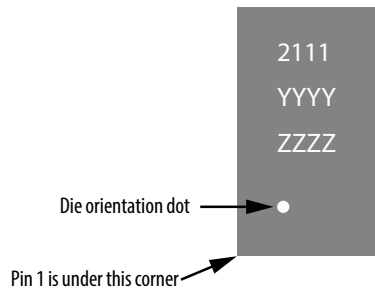


Gate bumps are along this edge of the die
 Die is placed into pocket solder ball side down (face side down)

EPC2111 (note 1)			
Dimension (mm)	target	min	max
a	12.00	11.70	12.30
b	1.75	1.65	1.85
c (see note)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

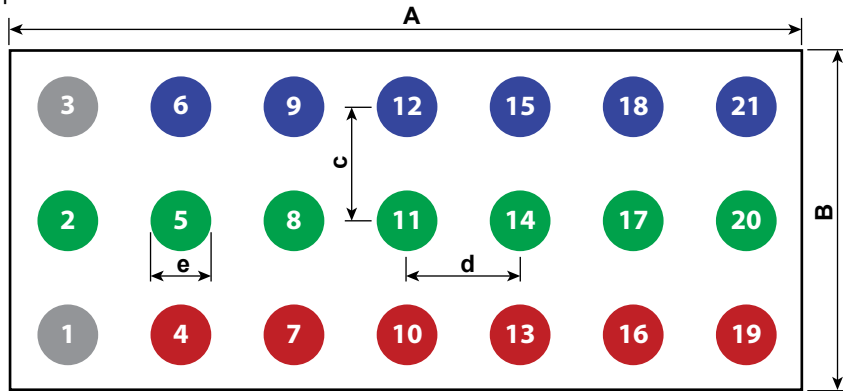
DIE MARKINGS



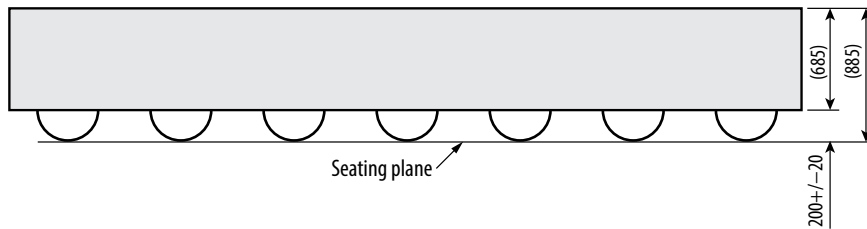
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2111	2111	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



Side View

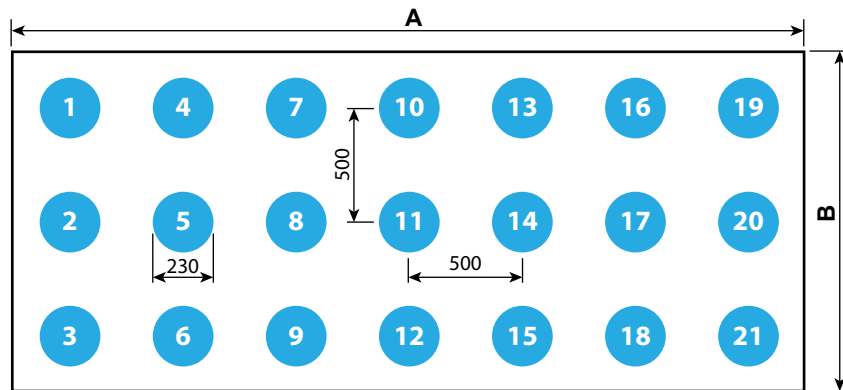


DIM	MIN	Nominal	MAX
A	3470	3500	3530
B	1470	1500	1530
c	500	500	500
d	500	500	500
e	238	264	290

Pad 1 is G1; Pad 3 is G2;
 Pads 4, 7, 10, 13, 16, 19 are V_{IN} ;
 Pads 2, 5, 8, 11, 14, 17, 20 are SN;
 Pads 6, 9, 12, 15, 18, 21 are GND

RECOMMENDED LAND PATTERN

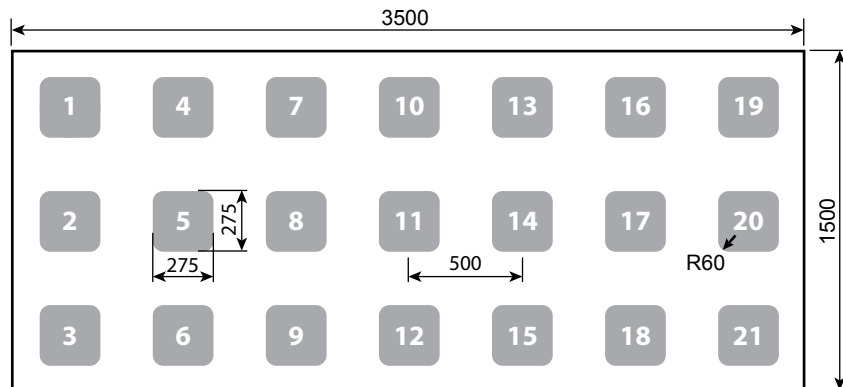
(measurements in μm)



The land pattern is solder mask defined.
 Solder mask is $10\ \mu\text{m}$ smaller per side than bump.

RECOMMENDED STENCIL DRAWING

(measurements in μm)



Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at:
<http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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 EPC Patent Listing: epc-co.com/epc/AboutEPC/Patents.aspx

Information subject to change without notice.

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