Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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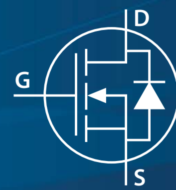
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

EPC2202 - Automotive 80 V (D-S) Enhancement Mode Power Transistor

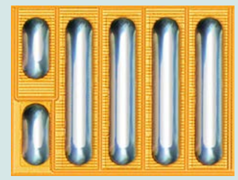
V_{DS} , 80 V
$R_{DS(on)}$, 17 mΩ
I_D , 18 A
AEC-Q101



EFFICIENT POWER CONVERSION

RoHS Pb | Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC2202 eGaN® FETs are supplied only in passivated die form with solder bars.
Die size: 2.1 mm x 1.6 mm

Applications

- LiDAR/Pulsed Power Applications
- High Power Density DC-DC Converters
- Class-D Audio
- High Intensity Headlamps

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2202.aspx

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
I_D	Continuous (T_A = 25°C, $R_{θJA}$= 12°C/W)	18	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	75	
V_{GS}	Gate-to-Source Voltage	5.75	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics

	PARAMETER	TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	2	°C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	4	
$R_{θJA}$	Thermal Resistance, Junction to Ambient (Note 1)	69	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	80			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 64 V, V_{GS} = 0 V		20	250	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	3	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.01	0.25	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{GS}, I_D = 3 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 11 A		12	17	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.8		V

All measurements were done with substrate shorted to source.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		345	415	pF
C_{RSS}	Reverse Transfer Capacitance			3		
C_{OSS}	Output Capacitance			230	345	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		279		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			352		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 11 A		3.2	4	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 11 A		1		
Q_{GD}	Gate-to-Drain Charge			0.55		
$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		18	27	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 62.5% BVDSS.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 62.5% BVDSS.

Figure 1: Typical Output Characteristics at 25°C

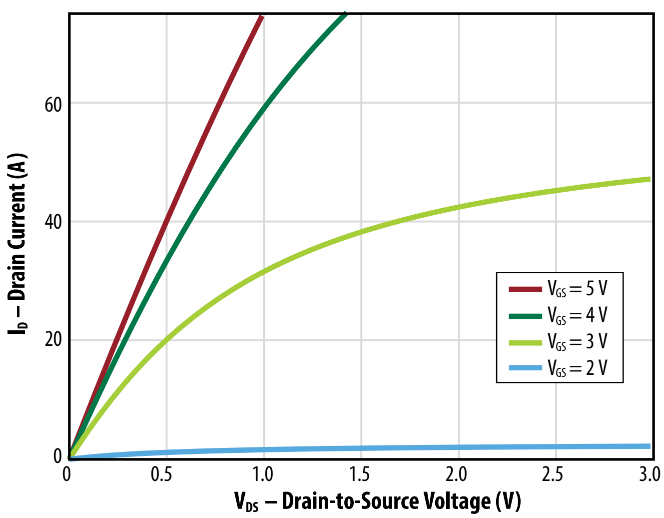


Figure 2: Transfer Characteristics

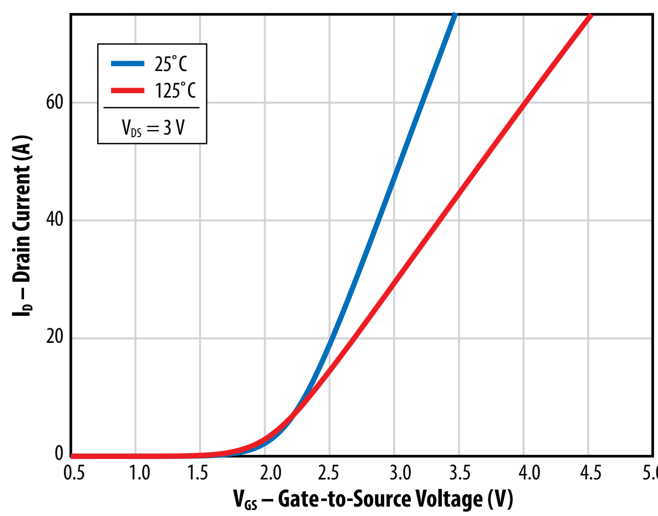


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Currents

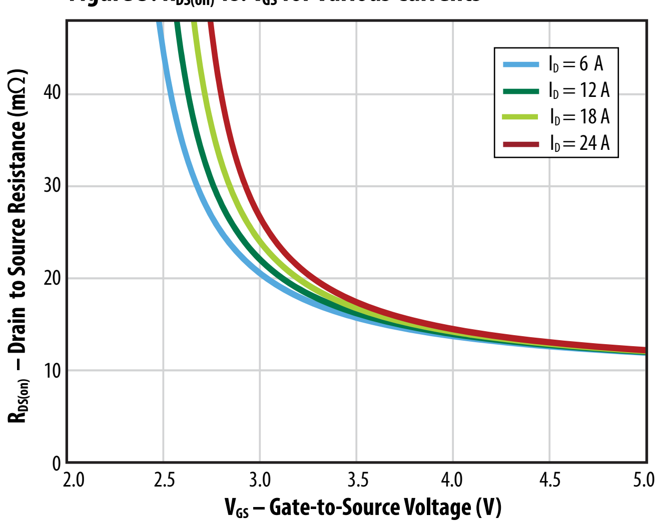


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

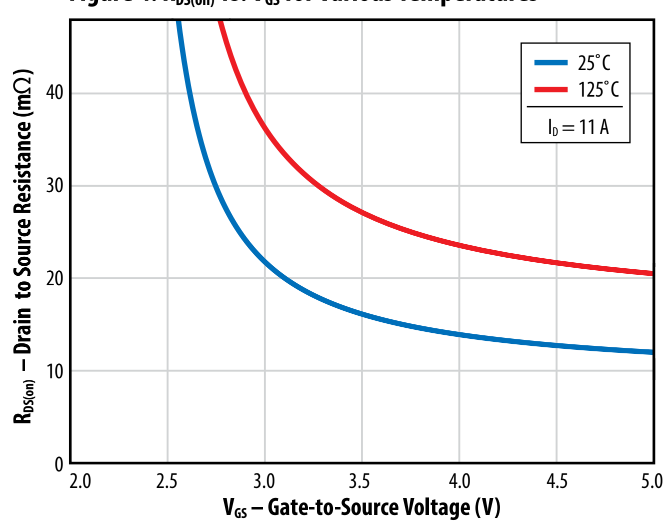


Figure 5a: Capacitance (Linear Scale)

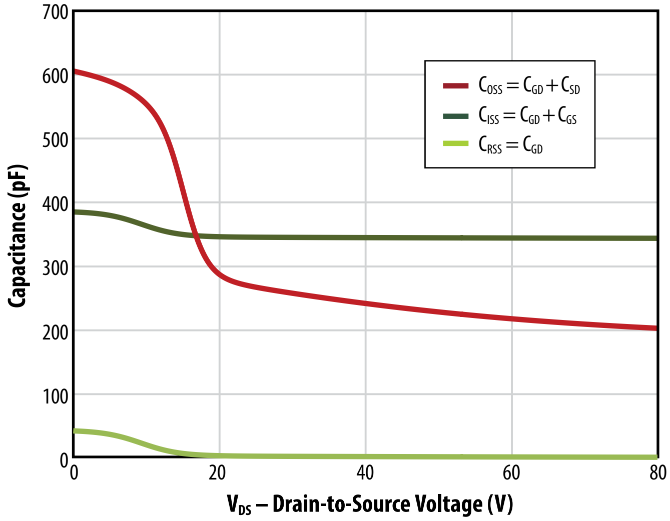


Figure 5b: Capacitance (Log Scale)

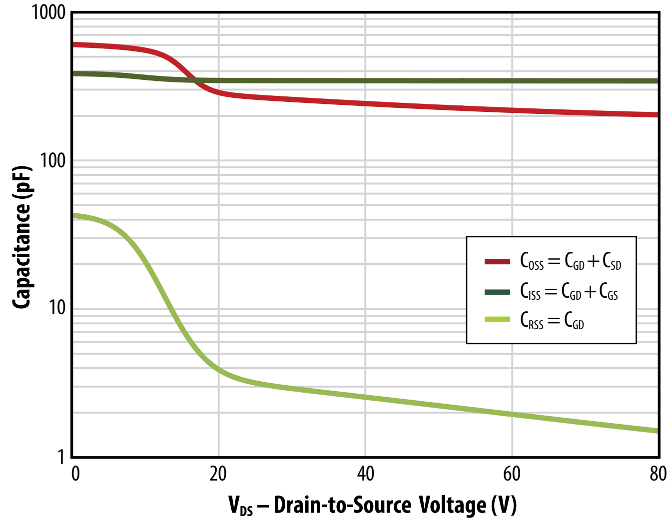


Figure 5c: Output Charge and C_{OSS} Stored Energy

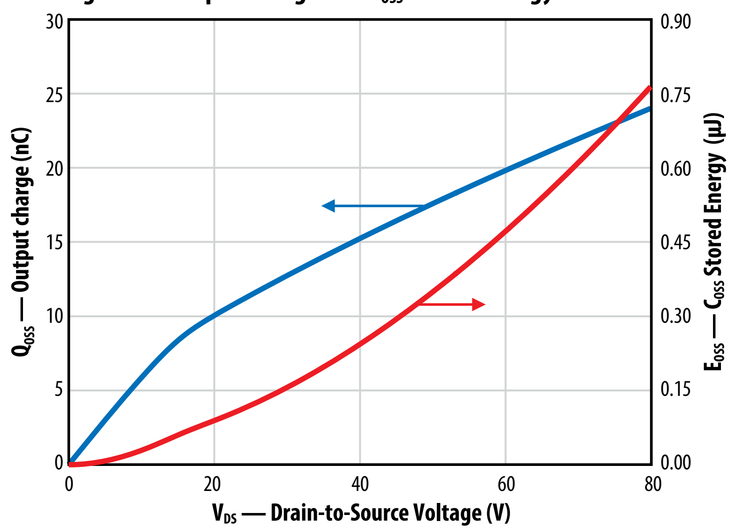


Figure 6: Gate Charge

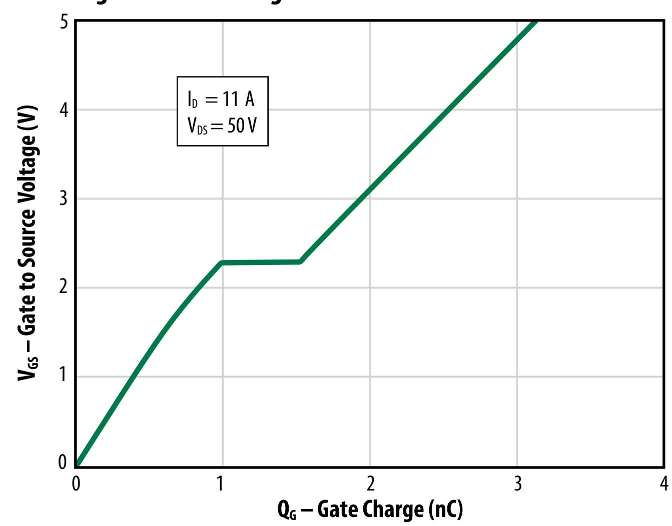


Figure 7: Reverse Drain-Source Characteristics

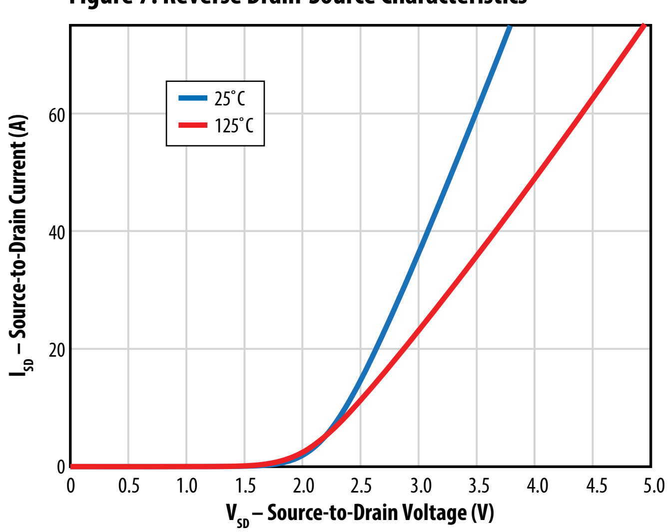


Figure 8: Normalized On-State Resistance vs. Temperature

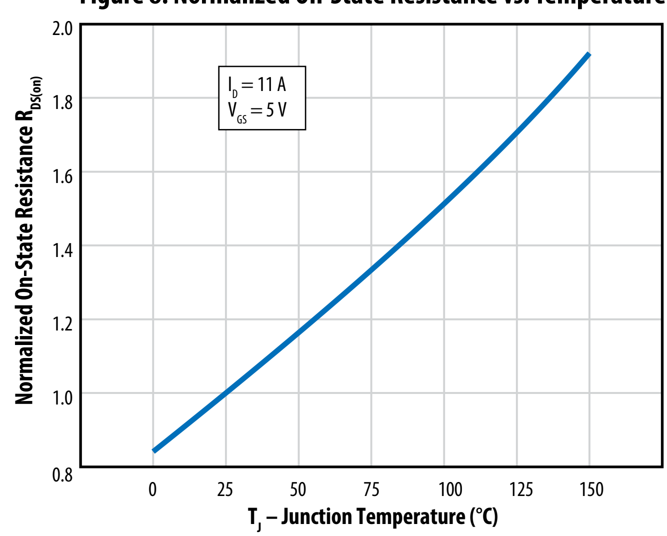


Figure 9: Normalized Threshold Voltage vs. Temperature

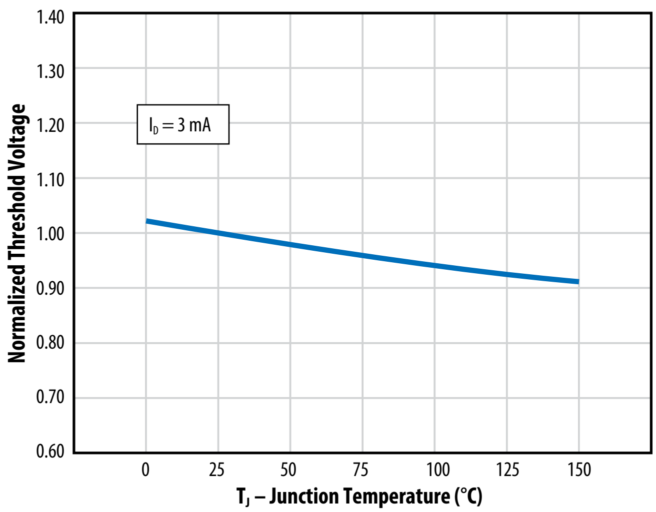


Figure 10: Transient Thermal Response Curves

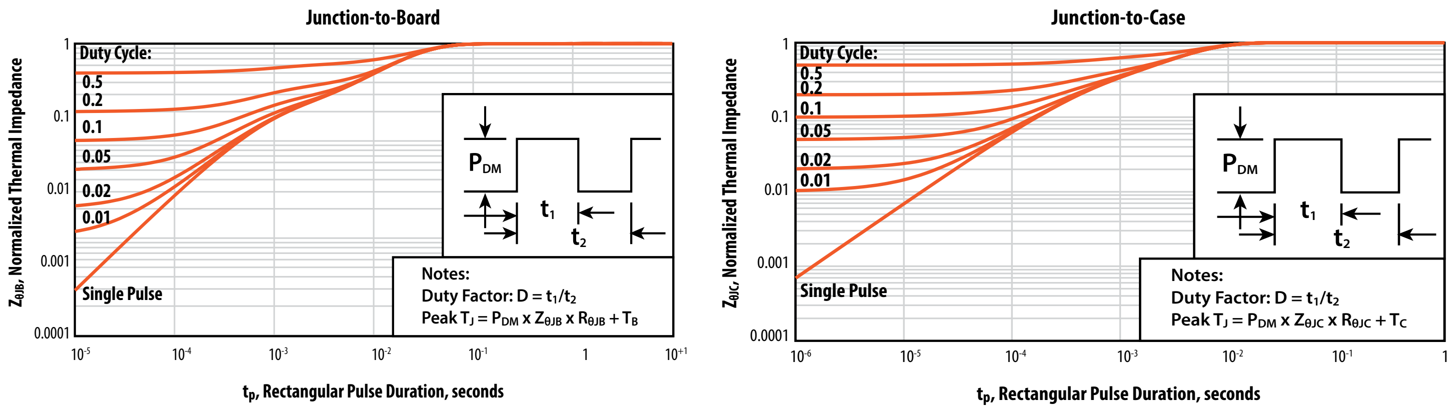
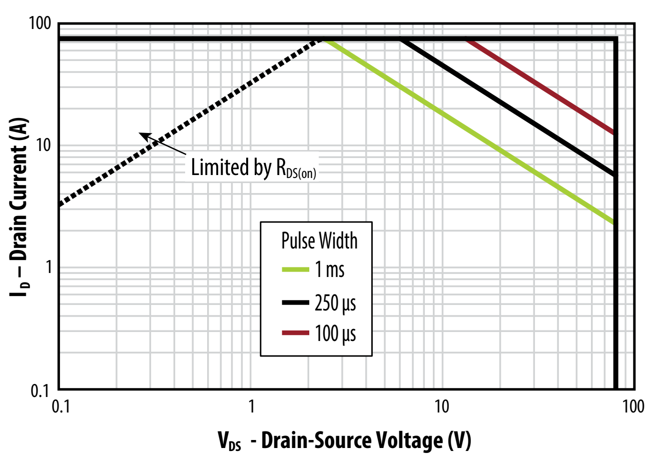
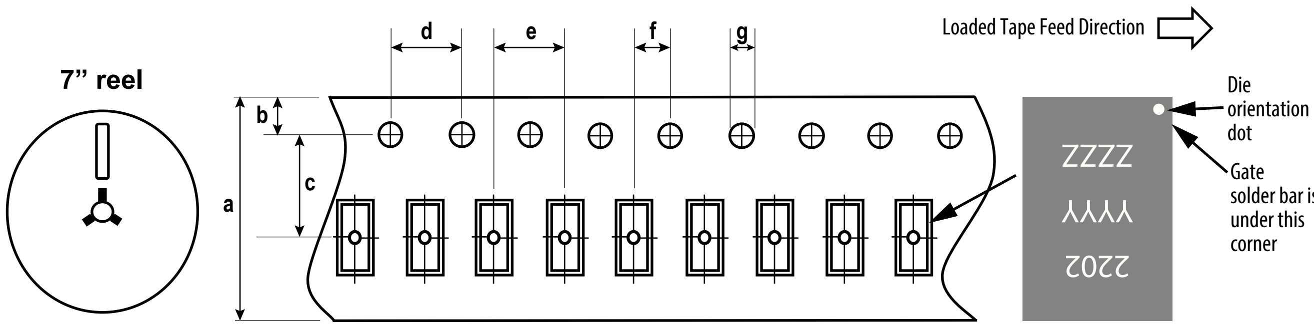


Figure 11: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

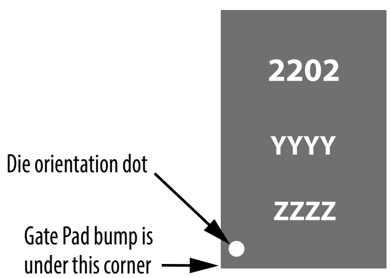


Die is placed into pocket solder bar side down (face side down)

	EPC2202 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

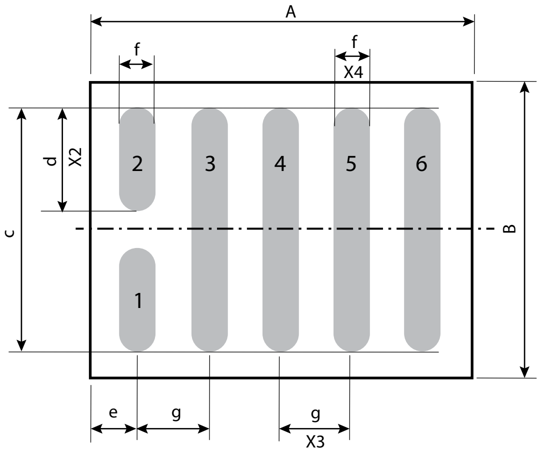
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2202	2202	YYYY	ZZZZ

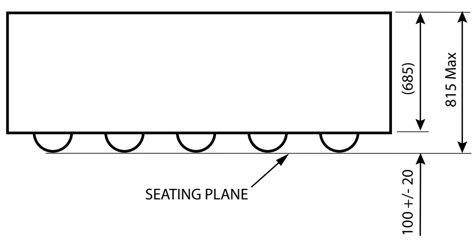
DIE OUTLINE

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2076	2106	2136
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

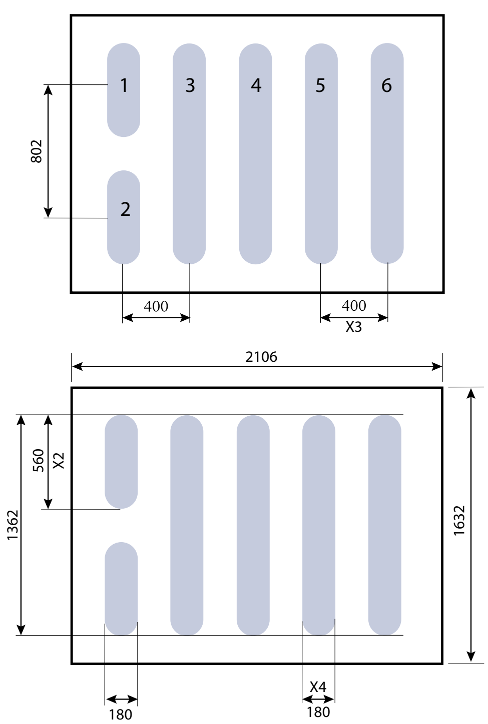
Side View



RECOMMENDED LAND PATTERN

(units in µm)

The land pattern is solder mask defined.



Pad no. 1 is Gate;

Pads no. 3, 5 are Drain;

Pads no. 4, 6 are Source;

Pad no. 2 is Substrate.

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Information subject to change without notice.

Revised April, 2018