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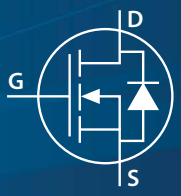
# EPC2203 – Automotive 80 V (D-S) Enhancement Mode Power Transistor

$V_{DS}$ , 80 V
$R_{DS(on)}$ , 80 mΩ
$I_D$ , 1.7 A
AEC-Q101




EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

| Maximum Ratings | | | |
|---|---|---|---|
| PARAMETER | | VALUE | UNIT |
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 80 | V |
| $I_D$ | Continuous ($T_A$ = 25°C, $R_{\theta JA}$ = 314°C/W) | 1.7 | A |
| | Pulsed (25°C, $T_{PULSE}$ = 300 µs) | 17 | |
| $V_{GS}$ | Gate-to-Source Voltage | 5.75 | V |
| | Gate-to-Source Voltage | -4 | |
| $T_J$ | Operating Temperature | –40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | –40 to 150 | |

| Thermal Characteristics | | | |
|---|---|---|---|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 6.5 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction to Board | 65 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1) | 100 | |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

EPC2203 eGaN® FETs are supplied only in passivated die form with solder bumps.
Die Size: 0.9 mm x 0.9 mm

**Applications**
- LiDAR/Pulsed Power Applications
- High Power Density DC-DC Converters
- Wireless Power
- Class-D Audio

**Benefits**
- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low $Q_G$
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2203.aspx

| Static Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 300 µA | 80 | | | V |
| $I_{DSS}$ | Drain-Source Leakage | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | | 5 | 250 | µA |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | $V_{GS}$ = 5 V | | 0.01 | 0.9 | mA |
| | Gate-to-Source Reverse Leakage | $V_{GS}$ = -4 V | | 2 | 250 | µA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 0.6 mA | 0.8 | 1.5 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS}$ = 5 V, $I_D$ = 1 A | | 53 | 80 | mΩ |
| $V_{SD}$ | Source-Drain Forward Voltage | $I_S$ = 0.35 A, $V_{GS}$ = 0 V | | 2.2 | | V |

All measurements were done with substrate shorted to source.

| Dynamic Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 73 | 88 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 0.5 | | |
| $C_{OSS}$ | Output Capacitance | | | 47 | 71 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS}$ = 0 to 50 V, $V_{GS}$ = 0 V | | 57 | | |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 72 | | |
| $R_G$ | Gate Resistance | | | 0.6 | | Ω |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 5 V, $I_D$ = 1 A | | 670 | 830 | pC |
| $Q_{GS}$ | Gate-to-Source Charge | $V_{DS}$ = 50 V, $I_D$ = 1 A | | 220 | | |
| $Q_{GD}$ | Gate-to-Drain Charge | | | 120 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 154 | | |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 3600 | 5400 | |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 62.5% BVDSS.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 62.5% BVDSS.

**Figure 1: Typical Output Characteristics at 25°C**

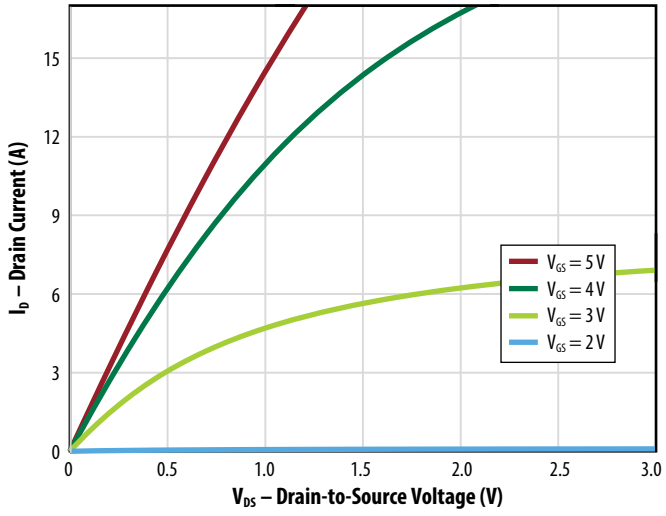



**Figure 2: Transfer Characteristics**

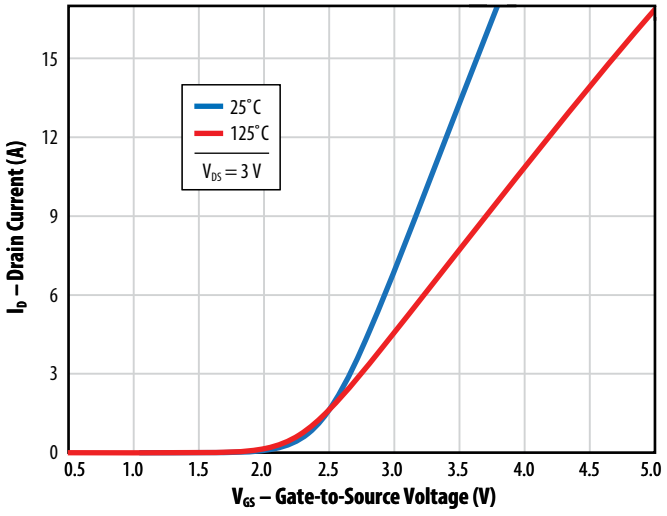



**Figure 3: $R_{DS(on)}$ vs. $V_{GS}$ for Various Drain Currents**

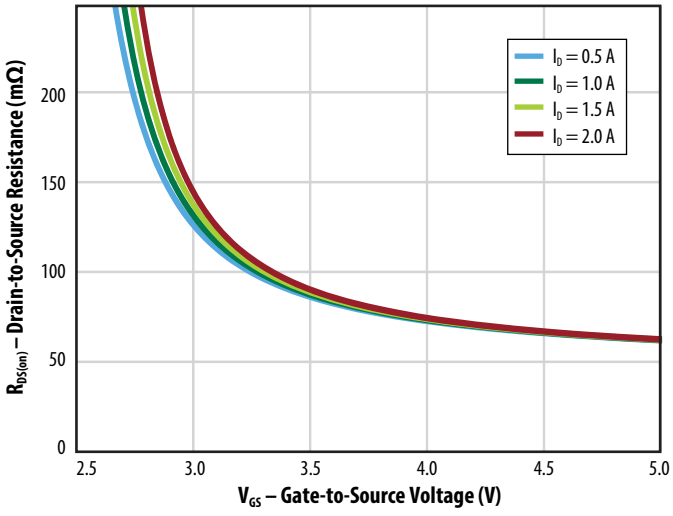



**Figure 4: $R_{DS(on)}$ vs. $V_{GS}$ for Various Temperatures**

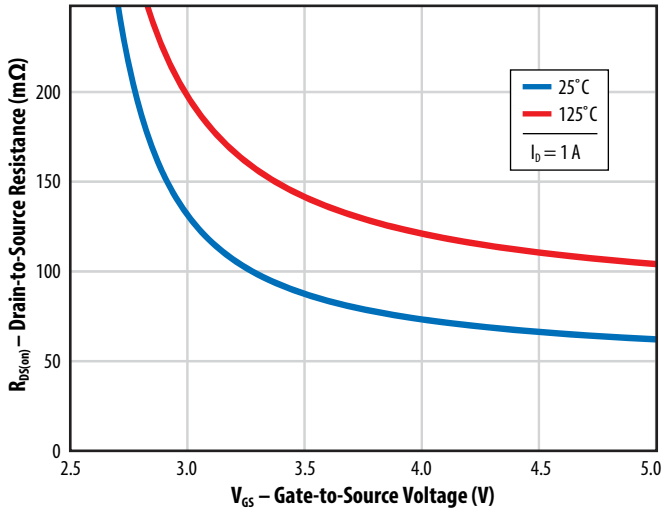


**Figure 5a: Capacitance (Linear Scale)**

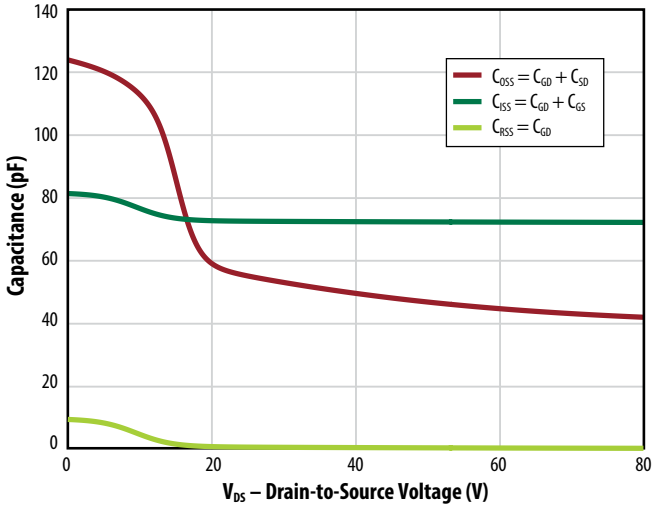



**Figure 5b: Capacitance (Log Scale)**

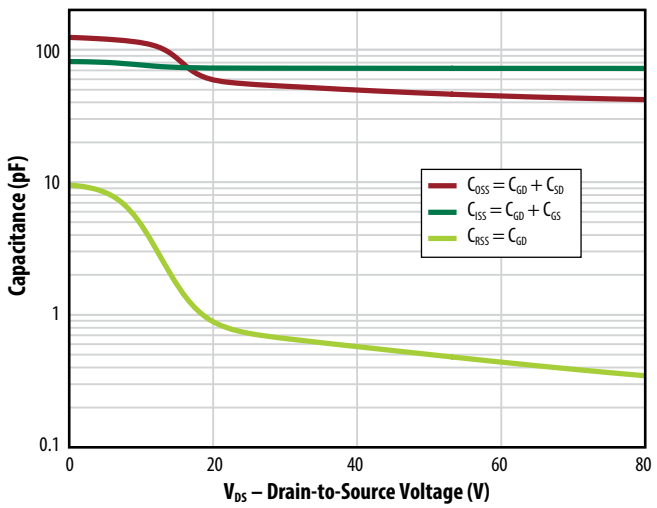



**Figure 5c: Output Charge and $C_{OSS}$ Stored Energy**

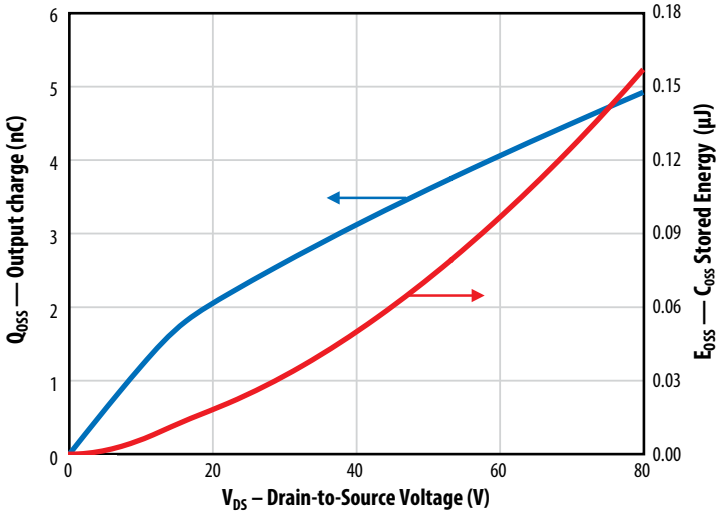



**Figure 6: Gate Charge**

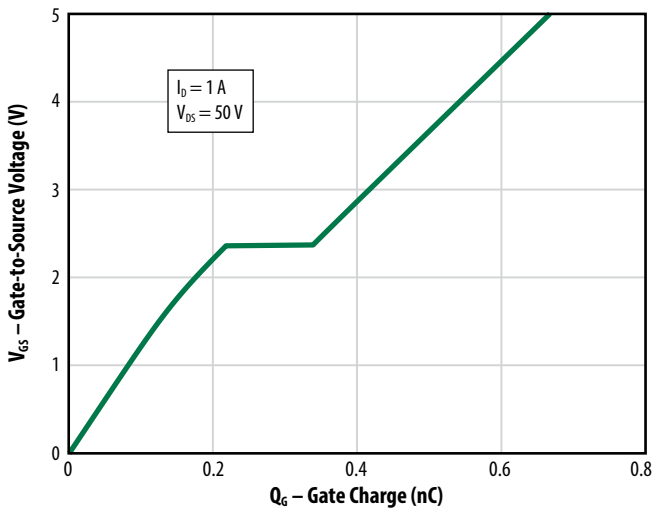



**Figure 7: Reverse Drain-Source Characteristics**

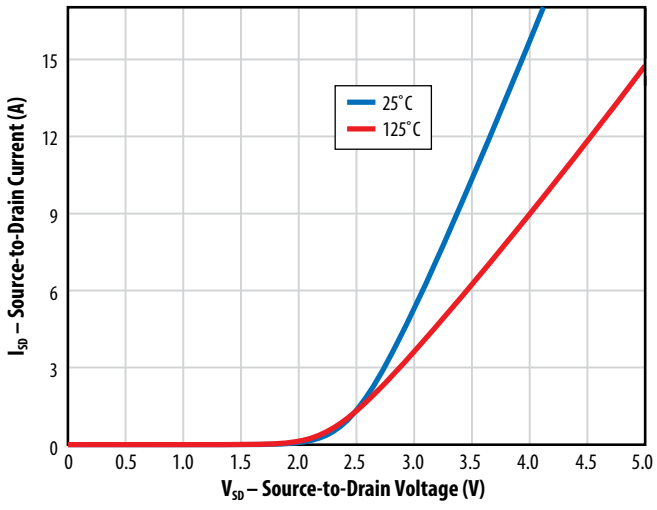
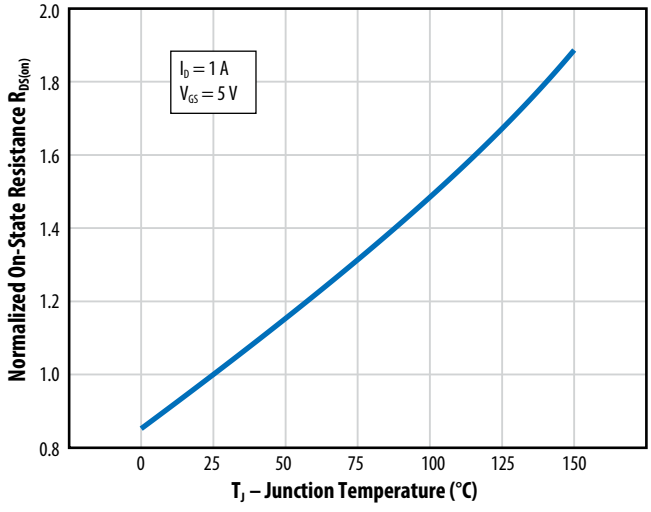



**Figure 8: Normalized On-State Resistance vs. Temperature**




All measurements were done with substrate shortened to source.

**Figure 9: Normalized Threshold Voltage vs. Temperature**

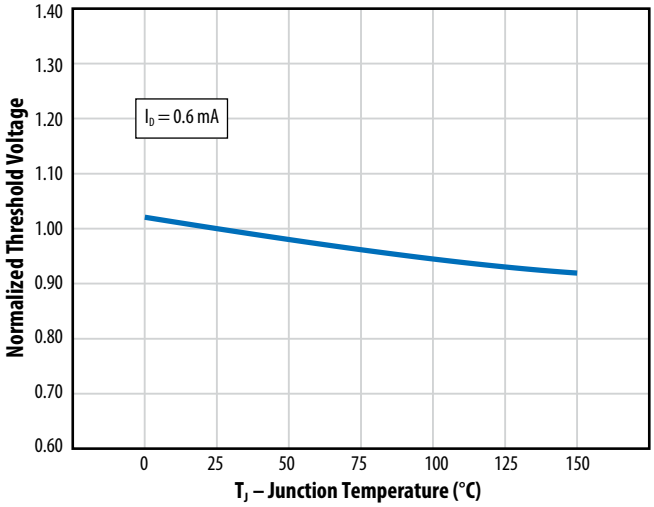



**Figure 10: Transient Thermal Response Curves**

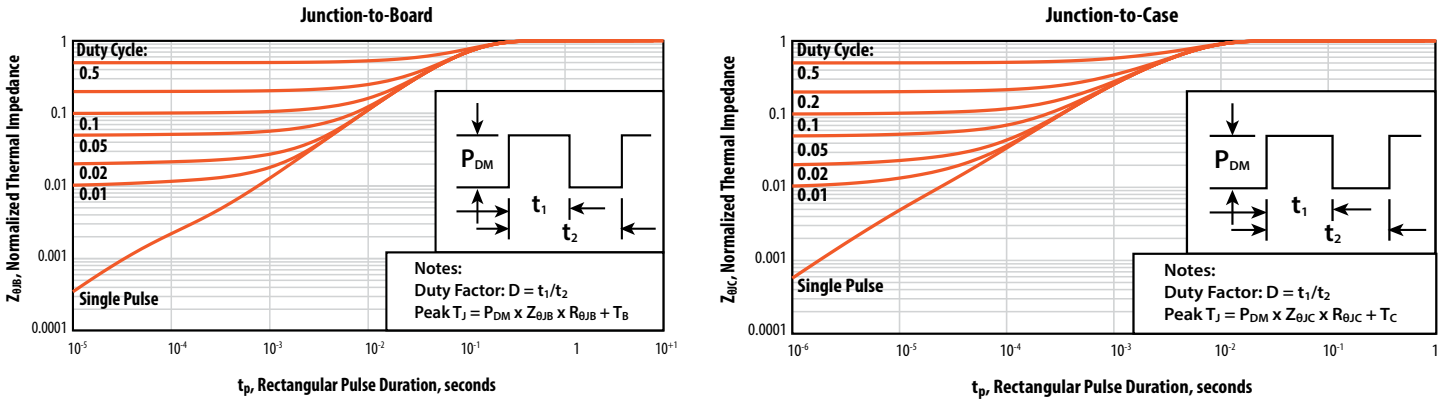
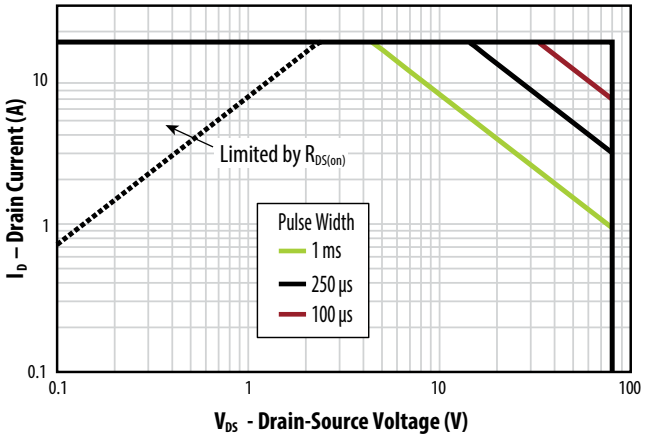
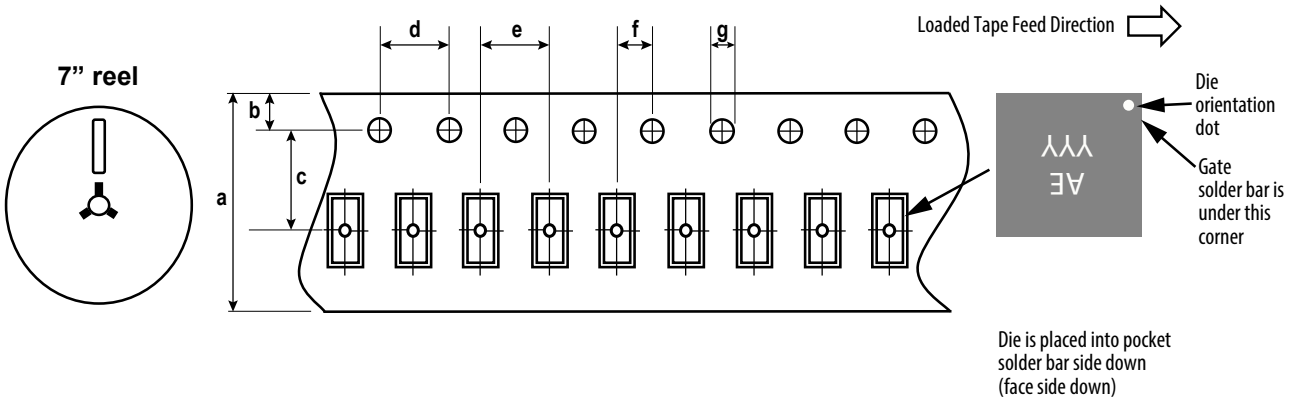



**Figure 11: Safe Operating Area**



## TAPE AND REEL CONFIGURATION

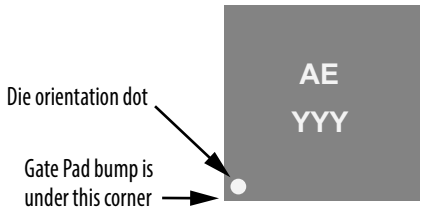
4mm pitch, 8mm wide tape on 7" reel




| | EPC2203 (note 1) | | |
|---|---|---|---|
| Dimension (mm) | target | min | max |
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (see note) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (see note) | 2.00 | 1.95 | 2.05 |
| g | 1.5 | 1.5 | 1.6 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

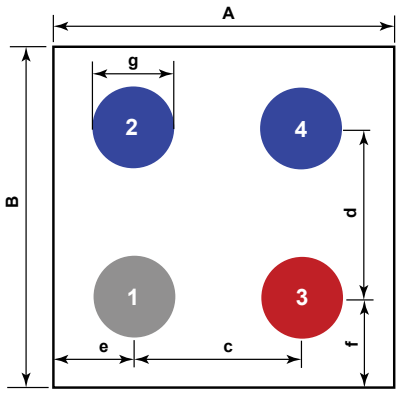
## DIE MARKINGS




| Part Number | Laser Markings | |
|---|---|---|
| | Part # Marking Line 1 | Lot_Date Code Marking line 2 |
| EPC2203 | AE | YYY |

## DIE OUTLINE

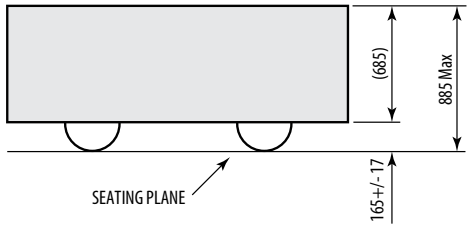
Solder Bump View




Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

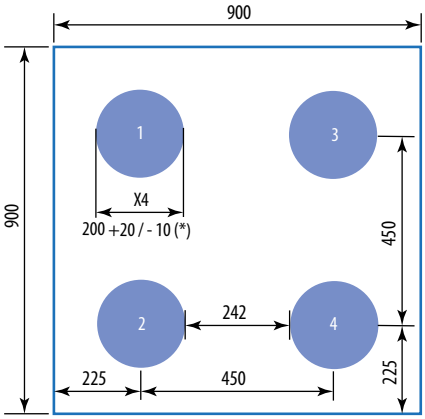
| DIM | MIN | Nominal | MAX |
|---|---|---|---|
| A | 870 | 900 | 930 |
| B | 870 | 900 | 930 |
| c | 450 | 450 | 450 |
| d | 450 | 450 | 450 |
| e | 210 | 225 | 240 |
| f | 210 | 225 | 240 |
| g | 187 | 208 | 229 |

Side View




## RECOMMENDED LAND PATTERN

*(measurements in µm)*




* minimum 190

The land pattern is solder mask defined
Solder mask is 10µm smaller per side than bump

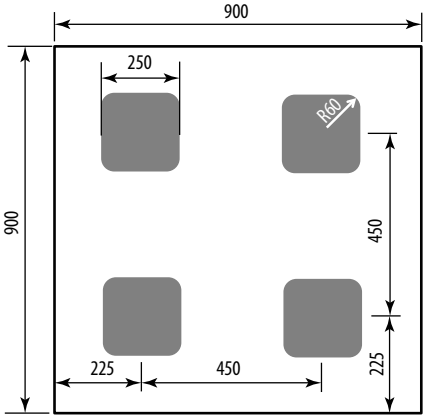
Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

## RECOMMENDED STENCIL DRAWING

*(measurements in µm)*




Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx