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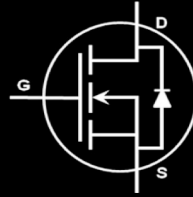
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



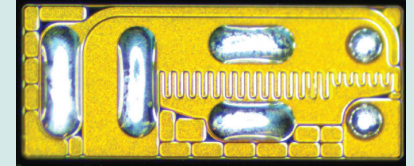
EPC8004 – Enhancement Mode Power Transistor

 $V_{DS}, 40\text{ V}$

New Product

 $R_{DS(on)}, 110\text{ m}\Omega$
 $I_D, 2.7\text{ A}$


Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC8004 eGaN FETs are supplied only in passivated die form with solder bars

Applications

- Ultra High Speed DC-DC Conversion
- RF Envelope Tracking
- Wireless Power Transfer
- Game Console and Industrial Movement Sensing (LiDAR)

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

| Maximum Ratings | | | |
|-----------------|---|------------|----|
| V_{DS} | Drain-to-Source Voltage (Continuous) | 40 | V |
| | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 125°C) | 48 | |
| I_D | Continuous ($T_A = 25^\circ\text{C}, \theta_{JA} = 87$) | 2.7 | A |
| | Pulsed ($25^\circ\text{C}, T_{Pulse} = 300\ \mu\text{s}$) | 7.5 | |
| V_{GS} | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| T_J | Operating Temperature | -40 to 150 | °C |
| T_{STG} | Storage Temperature | -40 to 150 | |

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|------------------------------|---|-----|-----|------|------------------|
| Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | | |
| BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0\text{ V}, I_D = 125\ \mu\text{A}$ | 40 | | V | |
| I_{DSS} | Drain Source Leakage | $V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}, T = 25^\circ\text{C}$ | | 50 | 100 | μA |
| I_{GSS} | Gate-Source Forward Leakage | $V_{GS} = 5\text{ V}$ | | 100 | 500 | μA |
| | Gate-Source Reverse Leakage | $V_{GS} = -4\text{ V}$ | | 50 | 100 | |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{GS} = V_{GS}, I_D = 0.25\text{ mA}$ | 0.8 | 1.4 | 2.5 | V |
| $R_{DS(ON)}$ | Drain-Source On Resistance | $V_{GS} = 5\text{ V}, I_D = 0.5\text{ A}$ | | 80 | 110 | $\text{m}\Omega$ |
| V_{SD} | Source-Drain Forward Voltage | $I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$ | | 2.2 | | V |

Specifications are with substrate shorted to source where applicable.

| Thermal Characteristics | | | |
|-------------------------|--|-----|------|
| | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 8.2 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction to Board | 16 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1) | 82 | °C/W |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------|-----|------|-----|------|
| Dynamic Characteristics (T_J = 25°C unless otherwise stated) | | | | | |
| C _{ISS} | Input Capacitance | | 45 | 52 | pF |
| C _{OSS} | Output Capacitance | | 23 | 34 | |
| C _{RSS} | Reverse Transfer Capacitance | | 0.8 | 1.3 | |
| R _G | Gate Resistance | | 0.34 | | Ω |
| Q _G | Total Gate Charge | | 370 | 450 | pC |
| Q _{GS} | Gate to Source Charge | | 120 | | |
| Q _{GD} | Gate to Drain Charge | | 47 | 80 | |
| Q _{G(TH)} | Gate Charge at Threshold | | 95 | | |
| Q _{OSS} | Output Charge | | 630 | 940 | |
| Q _{RR} | Source-Drain Recovery Charge | | 0 | | |

Specifications are with substrate shorted to source where applicable.

Figure 1: Typical Output Characteristics at 25°C

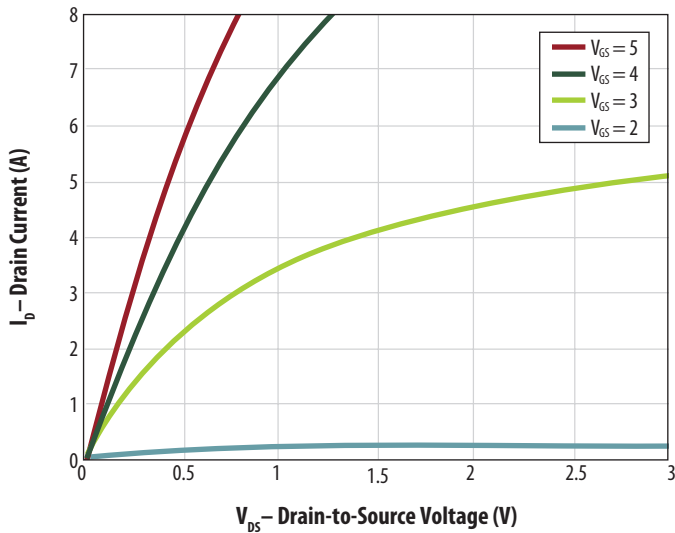


Figure 2: Transfer Characteristics

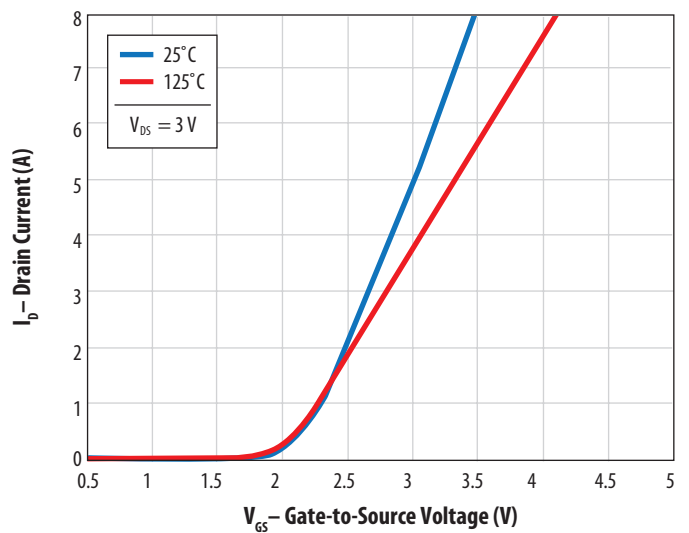


Figure 3: R_{DS(on)} vs V_{GS} for Various Drain Currents

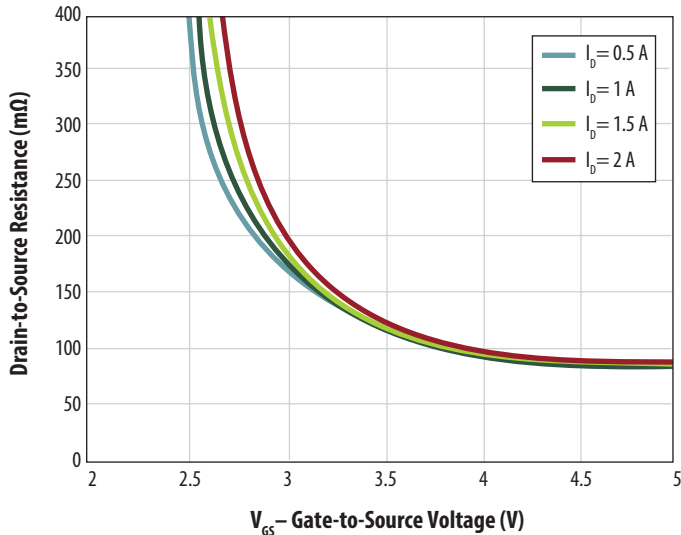


Figure 4: R_{DS(on)} vs V_{GS} for Various Temperatures

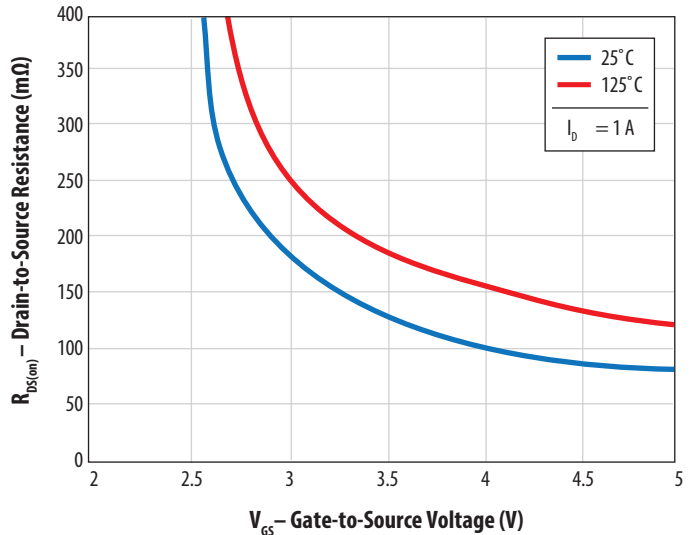


Figure 5: Capacitance (Linear Scale)

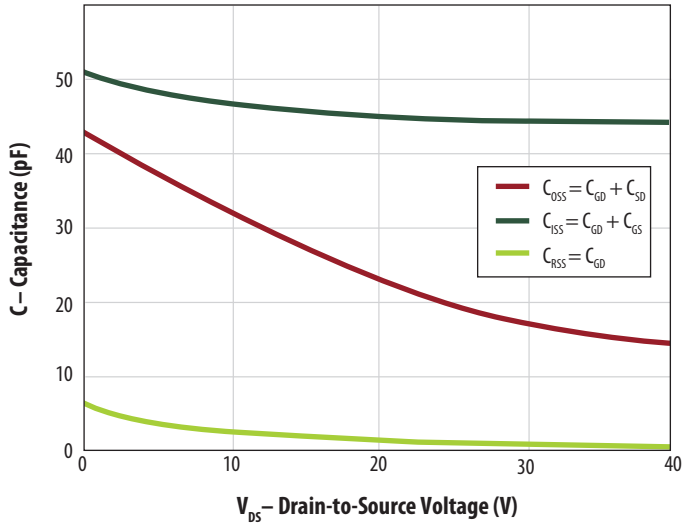


Figure 5A: Capacitance (Log Scale)

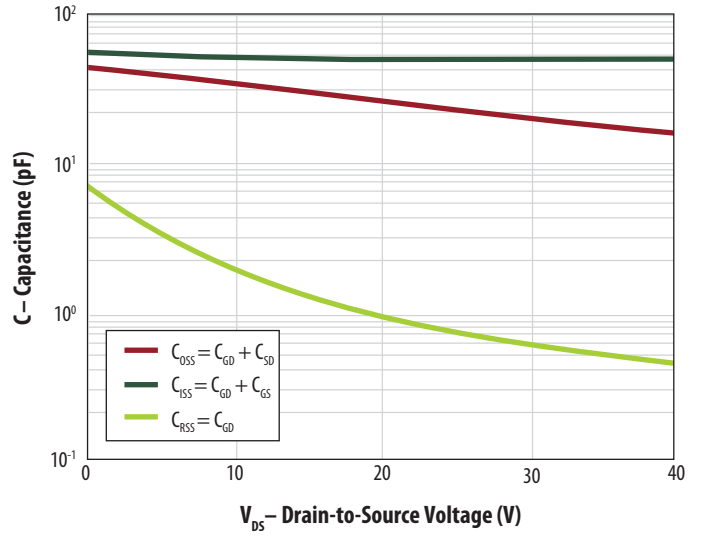


Figure 6: Gate Charge

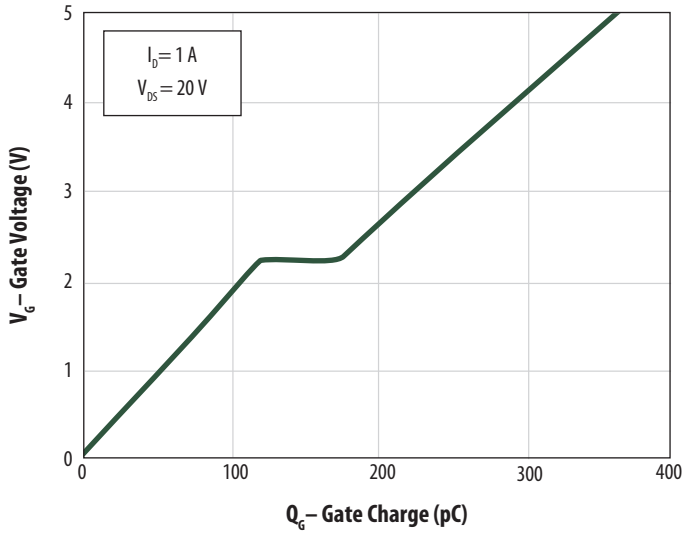


Figure 7: Reverse Drain-Source Characteristics

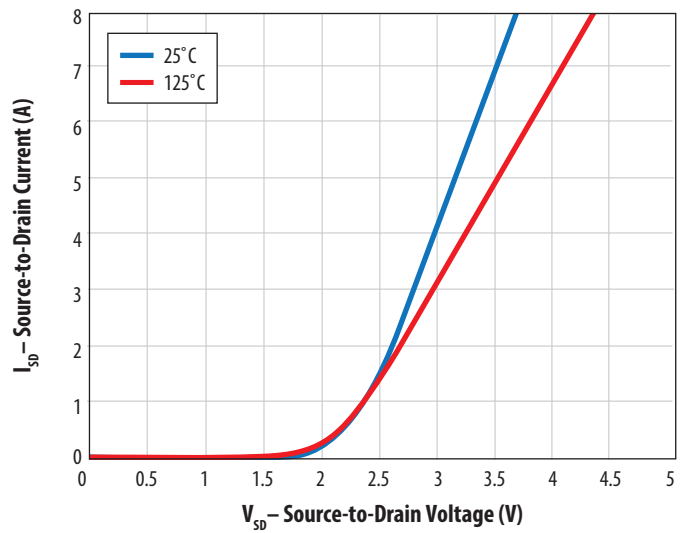


Figure 8: Normalized On Resistance vs Temperature

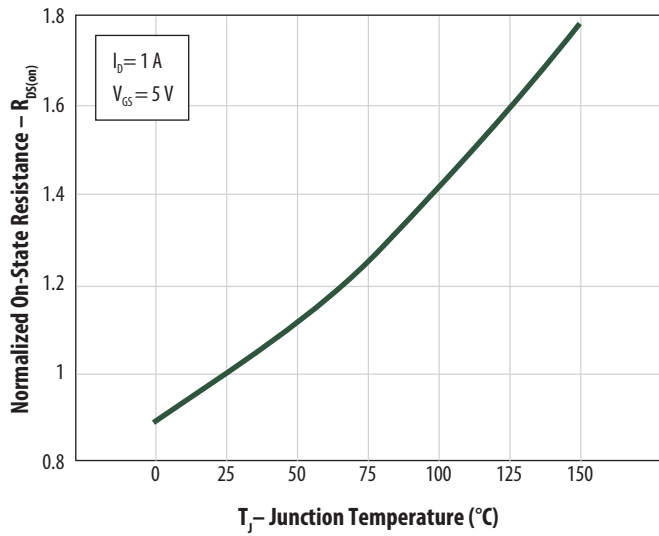


Figure 9: Normalized Threshold Voltage vs Temperature

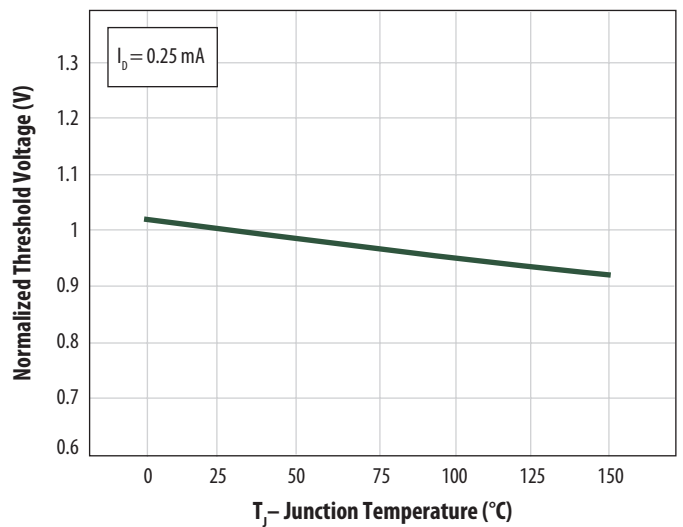
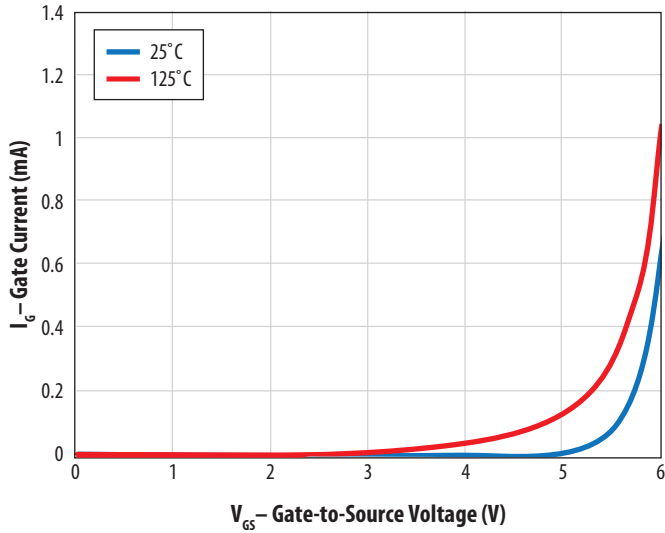


Figure 10: Gate Current



All measurements were done with substrate shortened to source.

Figure 12: Gain Chart

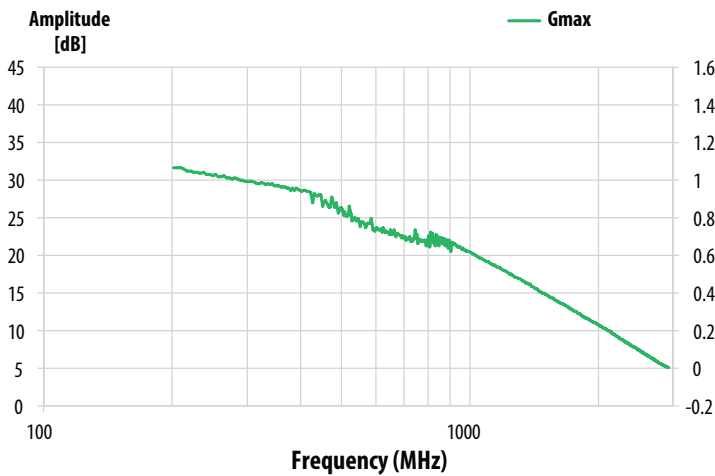


Figure 11: Smith Chart

S-Parameter Characteristics
 $V_{GSQ} = 1.38\text{ V}$, $V_{DSQ} = 20\text{ V}$, $I_{DQ} = 0.50\text{ A}$
 Pulsed Measurement, Heat-Sink Installed, $Z_0 = 50\ \Omega$

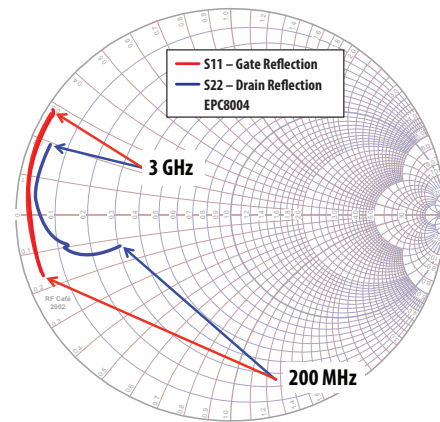


Figure 13: Device Reflection

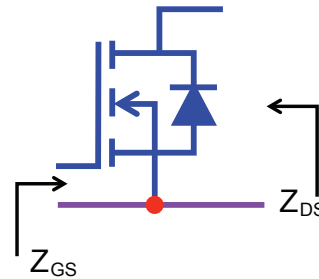
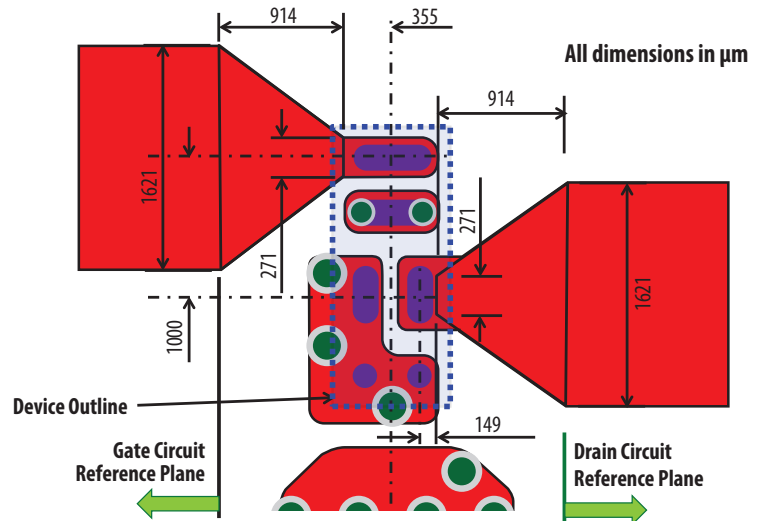


Figure 14: Taper and Reference Plane details – Device Connection

Micro-Strip design: 2-layer
 1/2 oz (17.5 μm) thick copper
 30 mil thick R04350 substrate



| Frequency [MHz] | Gate (Z_{GS}) [Ω] | Drain (Z_{DS}) [Ω] |
|-----------------|--------------------------------|---------------------------------|
| 200 | $2.00 - j8.07$ | $15.27 - j6.36$ |
| 500 | $1.74 - j2.18$ | $10.78 - j7.01$ |
| 1000 | $1.41 + j1.60$ | $5.98 - j4.42$ |
| 1200 | $1.30 + j3.20$ | $4.52 - j3.07$ |
| 1500 | $1.11 + j4.75$ | $3.19 - j0.98$ |
| 2000 | $0.84 + j8.32$ | $2.14 + j3.07$ |
| 2400 | $0.70 + j10.24$ | $1.95 + j5.86$ |
| 3000 | $0.65 + j14.17$ | $2.17 + j10.24$ |

S-Parameter Table - Download S-parameter files at www.epc-co.com

Figure 15: Transient Thermal Response Curves

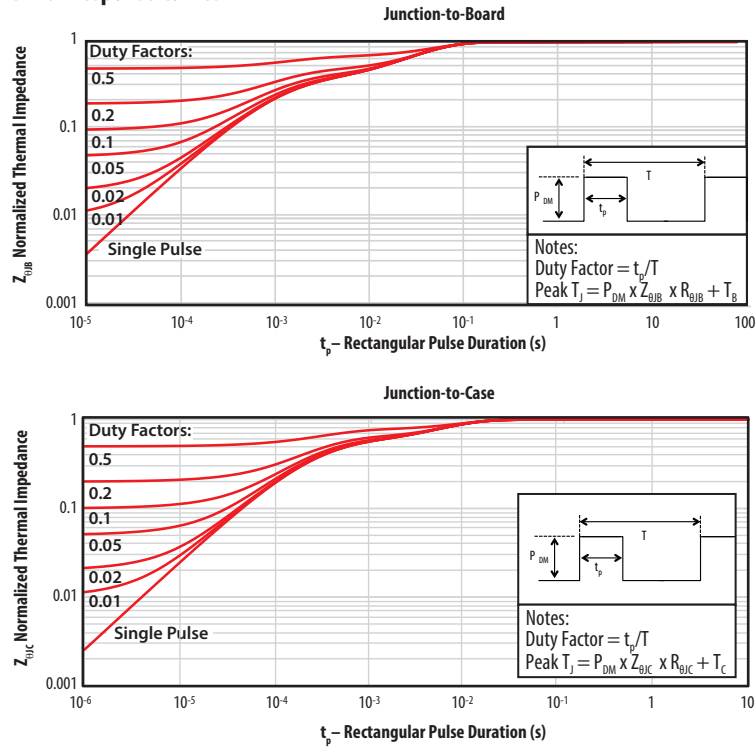
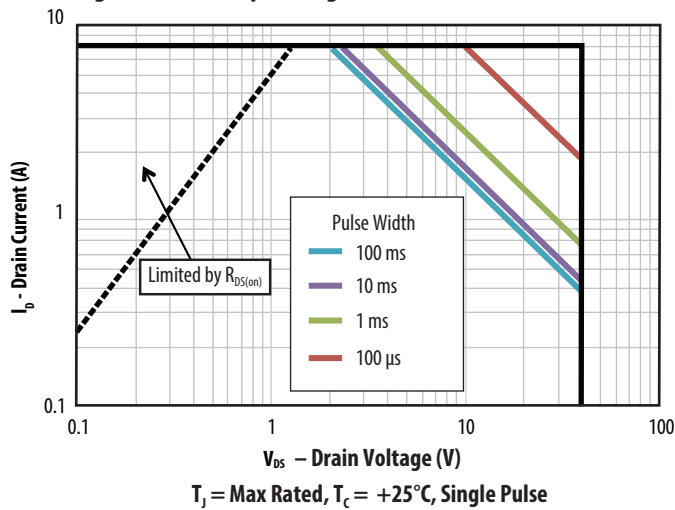


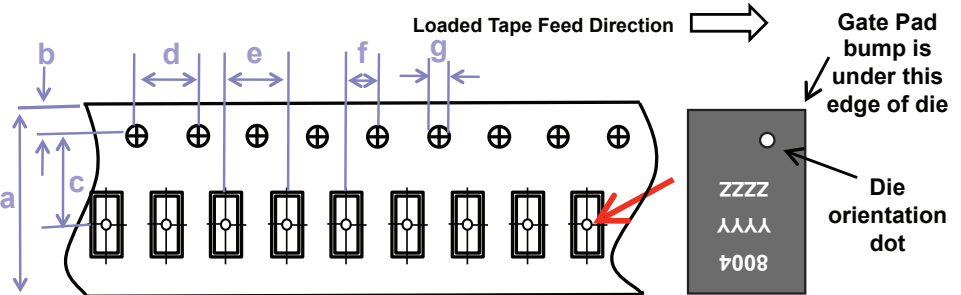
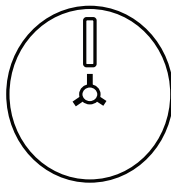
Figure 16: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

7" reel



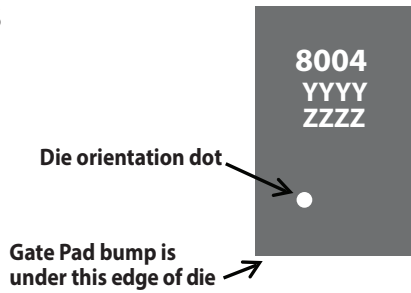
| Dimension (mm) | EPC8004 (Note 1) | | |
|----------------|------------------|------|------|
| | target | min | max |
| a | 8 | 7.9 | 8.3 |
| b | 1.75 | 1.65 | 1.85 |
| c (see note 2) | 3.5 | 3.45 | 3.55 |
| d | 4 | 3.9 | 4.1 |
| e | 4 | 3.9 | 4.1 |
| f (see note 2) | 2 | 1.95 | 2.05 |
| g | 1.5 | 1.5 | 1.6 |

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

Die is placed into pocket bump side down (face side down)

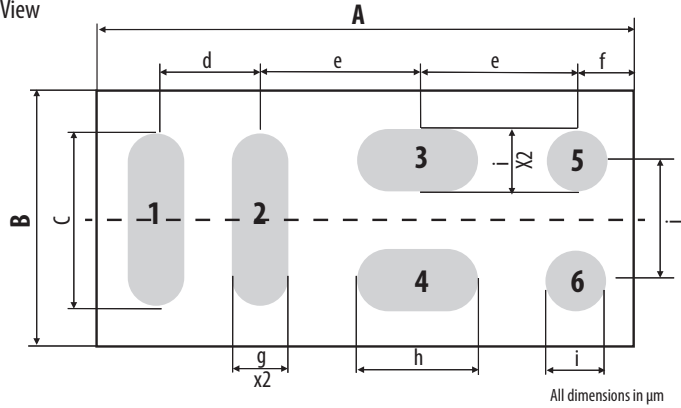
DIE MARKINGS



| Part Number | Laser Markings | | |
|-------------|--------------------------|---------------------------------|---------------------------------|
| | Part # Marking Line 1 | Lot_Date Code Marking line 2 | Lot_Date Code Marking Line 3 |
| EPC8004 | 8004 | YYYY | ZZZZ |

DIE OUTLINE

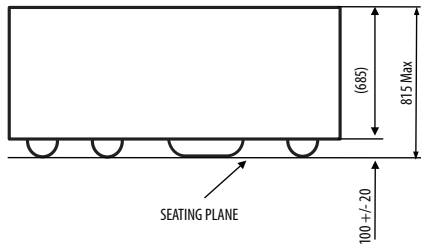
Solder Bar View



| Dim | Micrometers | | |
|-----|-------------|---------|------|
| | Min | Nominal | Max |
| A | 2020 | 2050 | 2080 |
| B | 820 | 850 | 880 |
| C | 555 | 580 | 605 |
| D | 400 | 400 | 400 |
| E | 600 | 600 | 600 |
| F | 200 | 225 | 250 |
| G | 175 | 200 | 225 |
| H | 425 | 450 | 475 |
| I | 175 | 200 | 225 |
| J | 400 | 400 | 400 |

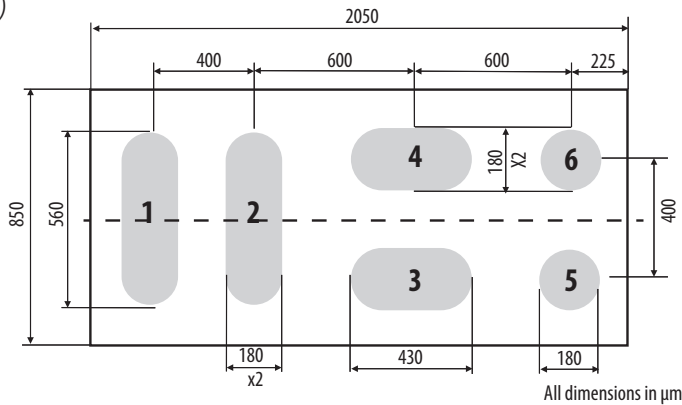
- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate

Side View



RECOMMENDED LAND PATTERN

(units in μm)



- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate

The land pattern is solder mask defined.
Solder mask opening is 10 μm smaller per side than bump.
Additional assembly resources available at:
<http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Information subject to change without notice.
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