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Development Board EPC9002

Quick Start Guide

100 V Half-Bridge with Gate Drive, Using EPC2001



DESCRIPTION

www.epc-co.com

The EPC9002 development board is a 100 V maximum device voltage, 10 A maximum output current, half bridge with onboard gate drives, featuring the EPC2001 enhancement mode (*eGaN*[®]) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2001 *eGaN FET* by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9002 development board is 2" x 1.5" and contains not only two EPC2001 *eGaN FET* in a half bridge configuration using

Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2001s *eGaN FET* please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V _{DD}	Gate Drive Input Supply Range		7	12	V
V _{IN}	Bus Input Voltage Range			70*	V
V _{OUT}	Switch Node Output Voltage			100	V
I _{OUT}	Switch Node Output Current			10*	A
V _{PWM}	PWM Logic Input Voltage Threshold	Input 'High'	3.5	6	V
		Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	60		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	200#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.

Limited by time needed to 'refresh' high side bootstrap supply voltage.

Quick Start Procedure

Development board EP9002 is easy to set up to evaluate the performance of the EP2001 eGAN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +VIN (J5, J6) and ground / return to -VIN (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive supply to +VDD (J1, Pin-1) and ground return to -VDD (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 100 V on VOUT).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE: When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EP9002 development board showcases the EP2001 eGAN FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EP9002 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE: The EP9002 development board does not have any current or thermal protection on board.

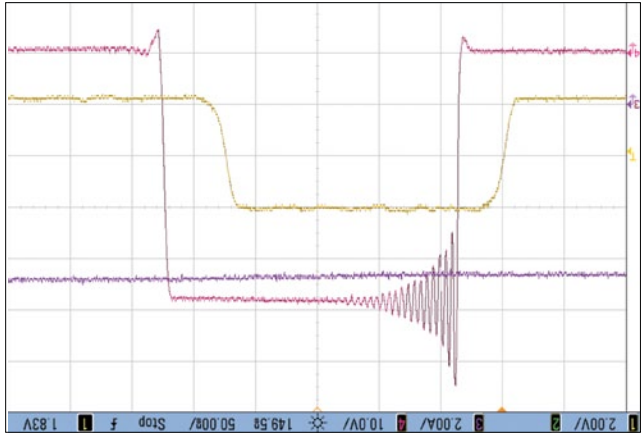


Figure 4: Typical Waveforms for $V_{in} = 48\text{ V}$ to 5 V / 7 A (500kHz) Buck converter
 CH1: V_{pwm} Input voltage – CH3: (I_{swt}) Switch node current – CH4: (V_{out}) Switch node voltage

Figure 1: Block Diagram of EP9002 Development Board

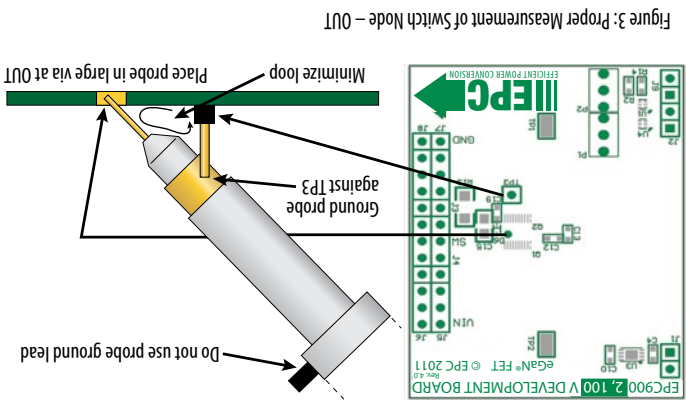
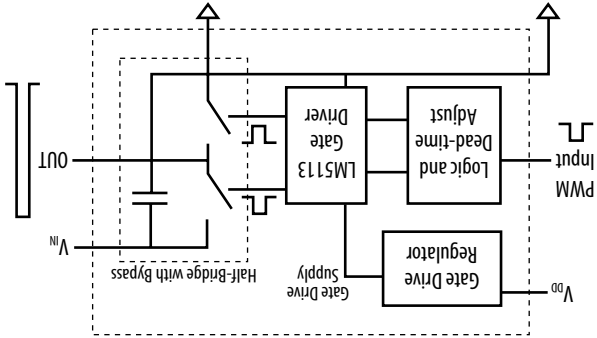


Figure 3: Proper Measurement of Switch Node – OUT

Figure 2: Proper Connection and Measurement Setup

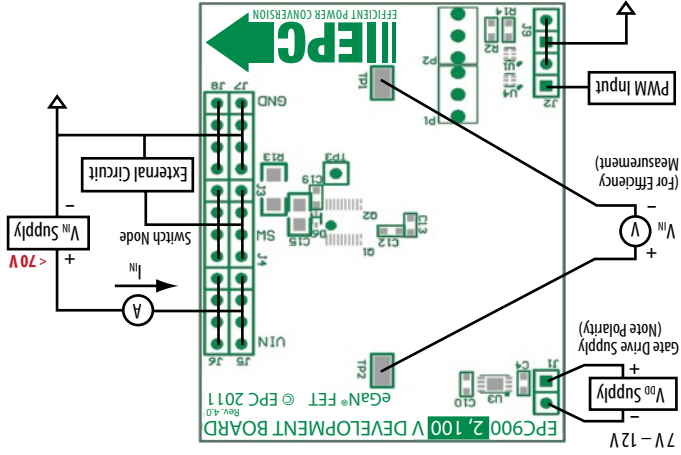
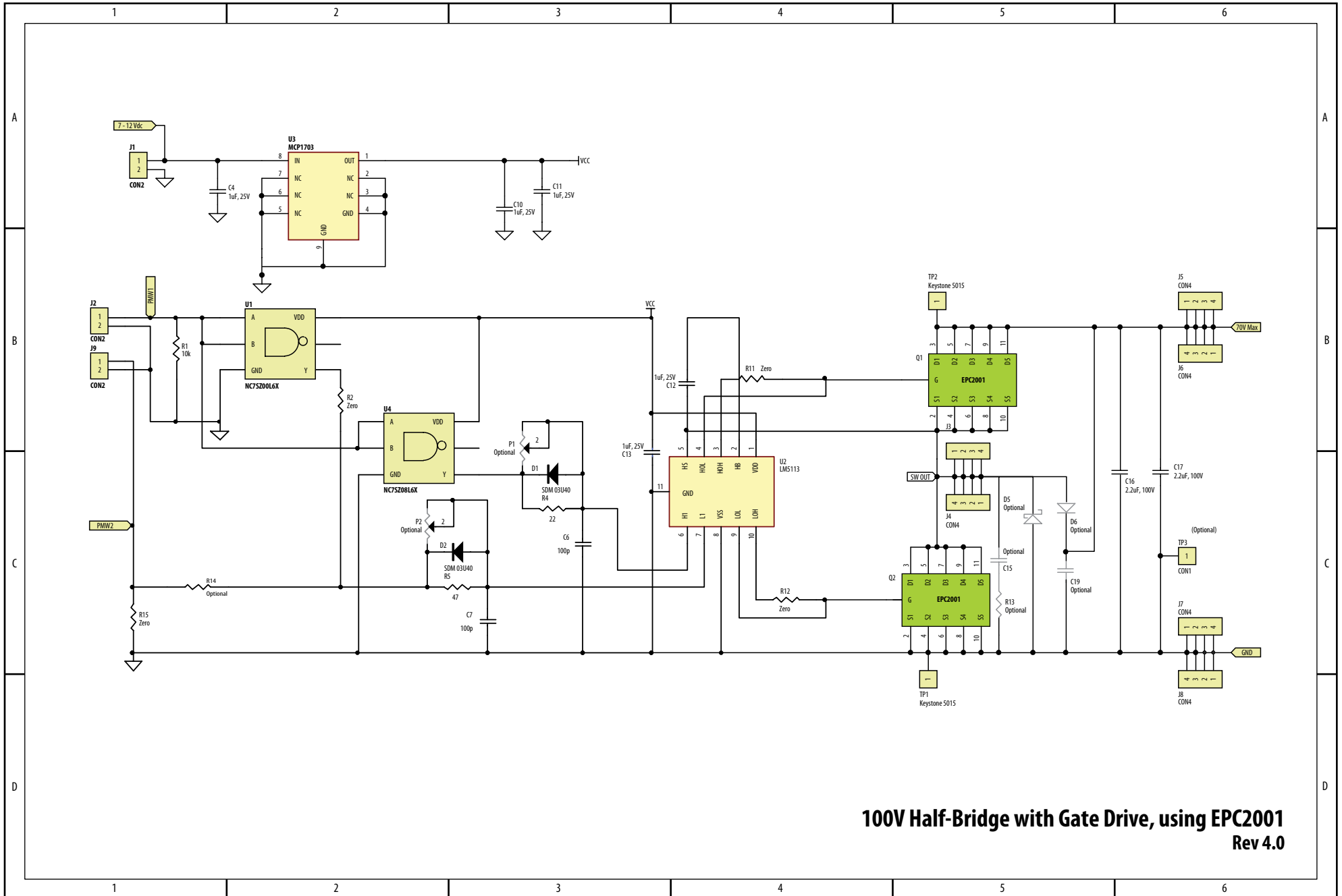


Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	4	C4, C10, C11, C13	Capacitor, 1uF, 10%, 25V, X5R	Murata, GRM188R61E105KA12D
2	2	C6, C7	Capacitor, 100pF, 5%, 50V, NP0	TDK, C1608C0G1H101J
3	1	C12	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1608X5R1E104K
4	2	C16, C17	Capacitor, 2.2uF, 10%, 100V, X5R	Taiyo Yuden, HMK325B7225K
5	2	D1, D2	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
6	3	J1, J2, J9	Connector	2pins of Tyco, 4-103185-0
7	1	J3, J4, J5, J6, J7, J8	Connector	FCI, 68602-224HLF
8	2	Q1, Q2	eGaN® FET	EPC, EPC2001
9	1	R1	Resistor, 10.0K, 5%, 1/8W	Stackpole, RMCF0603FT10K0
10	2	R2, R15	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603ZT0R00
11	1	R4	Resistor, 22 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT22R0
12	1	R5	Resistor, 47 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT47R0
13	2	R11, R12	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603ZT0R00
14	2	TP1, TP2	Test Point	Keystone Elect, 5015
15	1	TP3	Connector	1/40th of Tyco, 4-103185-0
16	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
17	1	U2	I.C., Gate driver	Texas Instruments, LM5113
18	1	U3	I.C., Regulator	Microchip, MCP1703T-5002E/MC
19	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
20	0	R13, R14	Optional Resistor	
21	0	C15, C19	Optional Capacitor	
22	0	D5, D6	Optional Diode	
23	0	P1, P2	Optional Potentiometer	



100V Half-Bridge with Gate Drive, using EPC2001
 Rev 4.0

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