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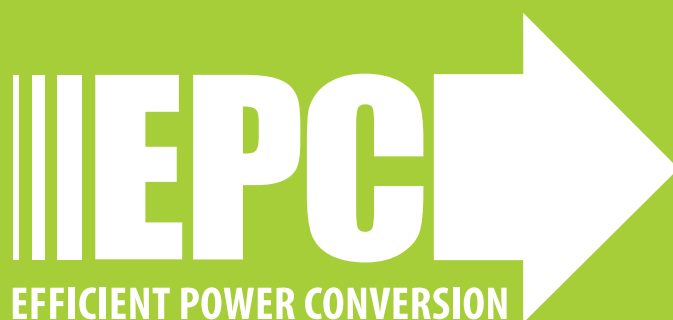


Demonstration System

EPC9059

Quick Start Guide

*EPC2100 - 30 V Half Bridge Parallel Evaluation
For High Current Applications*



DESCRIPTION

The EPC9059 development board features two 30 V EPC2100 eGaNiCs (Enhancement-mode Gallium Nitride Integrated Circuits) operating in parallel with a single onboard gate drive to achieve higher output currents. The purpose of this development board is to simplify the evaluation process of these monolithically integrated eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9059 development board is 2" x 2" and contains two EPC2100 eGaN monolithic half bridge ICs in a half bridge configuration using the Texas Instruments LM5113 gate driver. The board also contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2100 eGaNiC please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

QUICK START PROCEDURE

Development board EPC9059 is easy to set up to evaluate the performance of two EPC2100 eGaN monolithic half bridge ICs operated in parallel. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +V_{IN} (J1, J2) and ground / return to -V_{IN} (J5, J6).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required (half bridge configuration). The EPC9059 features an optional buck converter configuration, as shown in figure 2, with unpopulated footprints for an output inductor and output capacitors.
3. With power off, connect the gate drive input to +V_{DD} (J13, Pin-1) and ground return to -V_{DD} (J13, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J11, Pin-1) and ground return to any of the remaining J11 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the controller / PWM input source.
7. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage) and probe switching node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

Table 1: Performance Summary (T _A = 25°C)					
Symbol	Parameter	Conditions	Min	Max	Units
V _{DD}	Gate Drive Input Supply Range		7	12	V
V _{IN}	Bus Input Voltage Range ⁽¹⁾			20	V
I _{OUT}	Switch Node Output Current ⁽²⁾			50	A
V _{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V _{PWM} rise and fall time < 10 ns	50		ns
	Minimum 'Low' State Input Pulse Width ⁽³⁾	V _{PWM} rise and fall time < 10 ns	200		ns

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 30 V for EPC2100 eGaN monolithic half bridge IC.

(2) Maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermal cooling. EPC2100 eGaNiC intended for high step-down ratio applications.

(3) Limited by time needed to 'refresh' high side bootstrap supply voltage.

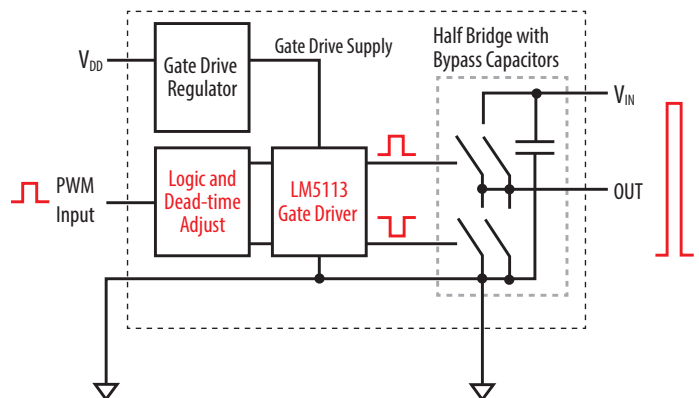


Figure 1: Block Diagram of EPC9059 Development Board

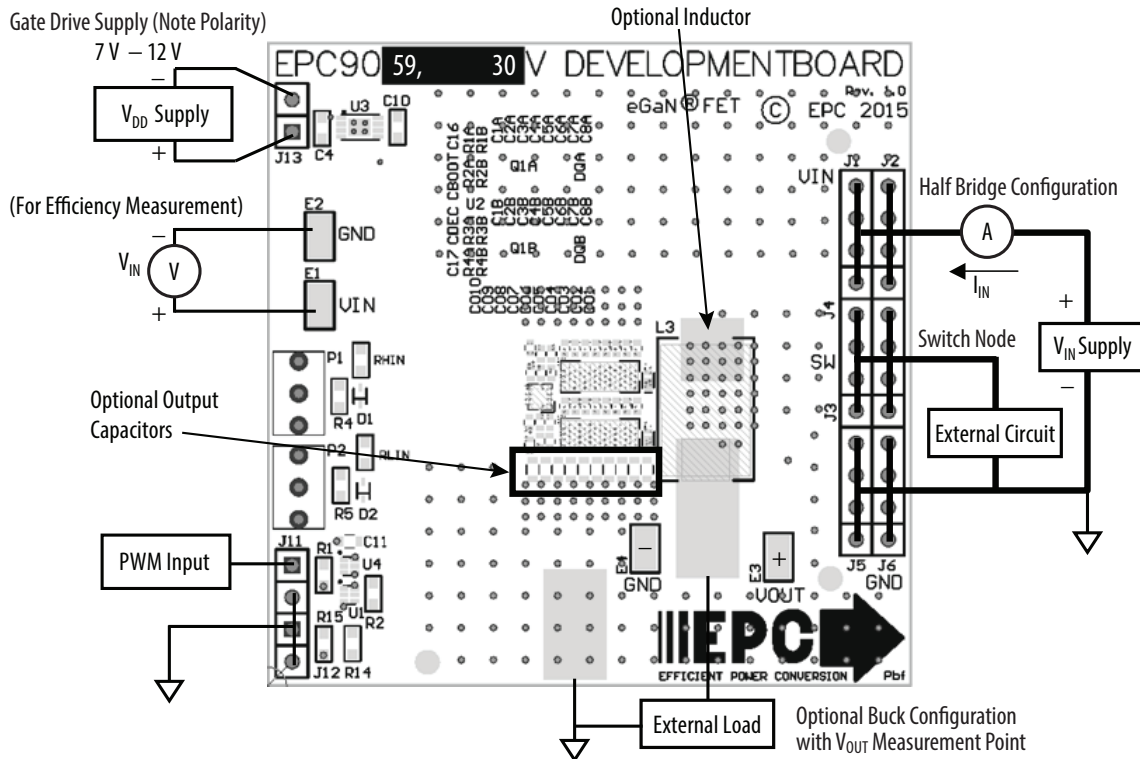


Figure 2: Proper Connection and Measurement Setup

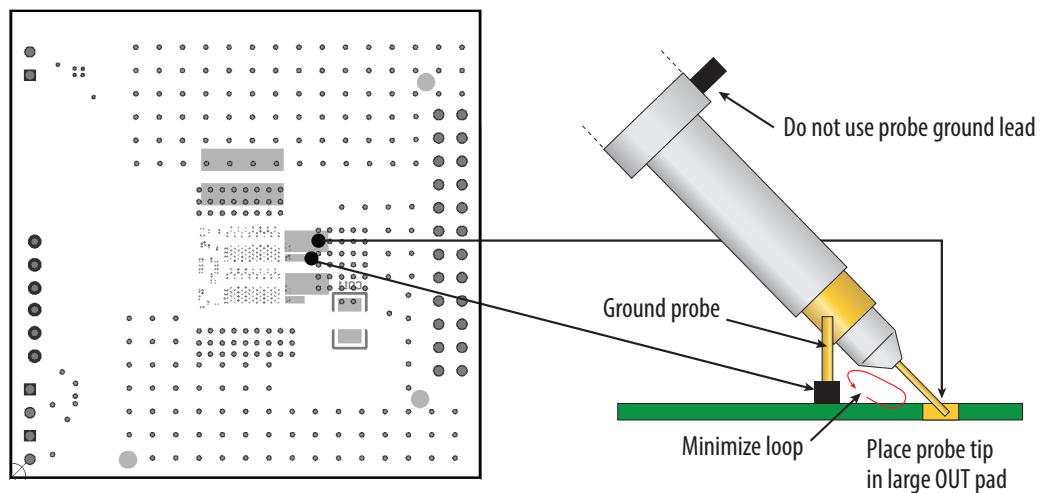


Figure 3: Proper Measurement of Switch Node – V_{SW}

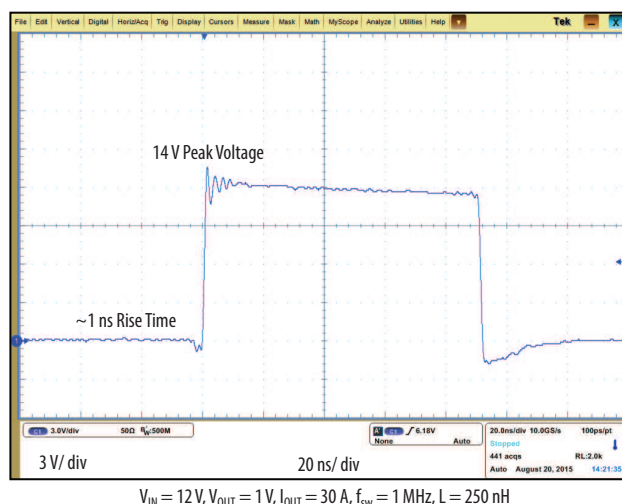


Figure 4: Typical Waveform for $V_{IN} = 12\text{ V}$ to 1 V_{OUT} , 30 A (1 MHz) Buck Converter

For more information regarding the in-circuit performance of EPC eGaN FETs, please consult: D. Reusch and J. Glaser, *DC-DC Converter Handbook*, a supplement to *GaN Transistors for Efficient Power Conversion*, First Edition, Power Conversion Publications, 2015.

THERMAL CONSIDERATIONS

The EPC9059 development board showcases the EPC2100 eGaNIC. The EPC9059 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C .

NOTE. The EPC9059 development board does not have any current or thermal protection on board.

For more information regarding the thermal performance of EPC eGaN FETs, please consult: D. Reusch and J. Glaser, *DC-DC Converter Handbook*, a supplement to *GaN Transistors for Efficient Power Conversion*, First Edition, Power Conversion Publications, 2015.

Table 2: Bill of Materials - Amplifier Board

Item	Qty	Reference	Part Description	Manufacturer/Part#
1	4	RLIN, RHIN, R2, R15	Jumper, Resistor, 0 Ohm, 0603	Stackpole, RMCF0603ZT0R00
2	Optional (10)	CO1, CO2, CO3, CO4, CO5, CO6, CO7, CO8, CO9, CO10	Output Capacitor 0603 Footprint	Optional
3	DNP	CO11	Output Capacitor 1206 Footprint	DNP
4	Optional (1)	L3	Output Inductor Coilcraft SLC1049 Footprint	Optional
5	2	DQA, DQB	30 V 2 A Schottky Diode	Diodes Incorporated, SDM2U30CSP-7
6	8	R1A, R2A, R3A, R4A, R1B, R2B, R3B, R4B	Gate Resistors 0 Ohm, 0402	Stackpole, RMCF0402ZT0R00
7	16	C1A, C2A, C3A, C4A, C5A, C6A, C7A, C8A, C1B, C2B, C3B, C4B, C5B, C6B, C7B, C8B	Input Capacitors 2.2 μF 25 V 20% X5R 0402	TDK Corporation, C1005X5R1E225M050BC
8	2	Q1A, Q2B	eGaNIC 30 V	EPC, EPC2100
9	3	J11, J12, J13	Connector	2 pins of Tyco, 4-103185-0
10	4	E1, E2, E3, E4	Test Point PC Miniature SMT	5015 Test Point PC Miniature SMT
11	1	CDEC	Decoupling Capacitor 1 μF , 10%, 25 V, X5R	TDK Corporation, C1005X5R1E105K050BC
12	1	CBOOT	Bootstrap Capacitor 0.1 μF , 10%, 25 V, X5R	TDK Corporation, C1005X5R1E104K050BC
13	2	C16, C17	Timing Capacitor 100 pF, 5%, 50 V, NP0	Kemet, C0402C101K5GACTU
14	DNP	P1, P2	Optional Potentiometer	DNP
15	DNP	R14	Optional Resistor	DNP
16	3	C4, C10, C11	Decoupling Capacitor 1 μF , 10%, 25 V, X5R	Murata, GRM188R61E105KA12D
17	2	D1, D2	Timing Schottky Diode	Diodes Inc., SDM03U40-7
18	6	J1, J2, J3, J4, J5, J6	Connector	FCI, 68602-224HLF
19	1	R1	Pull Down Resistor 10.0 K, 5%, 1/8 W	Stackpole, RMCF0603FT10K0
20	1	R4	Timing Resistor	Stackpole, RMCF0603FT51R0
21	1	R5	Timing Resistor	Stackpole, RMCF0603FT68R0
22	1	U3	I.C., Regulator	Microchip, MCP1703T-5002E/MC
23	1	U4	Logic Gate AND	Fairchild, NC7SZ08L6X
24	1	U1	Logic Gate NAND	Fairchild, NC7SZ00L6X
25	1	U2	Gate Driver	Texas Instruments, LM5113

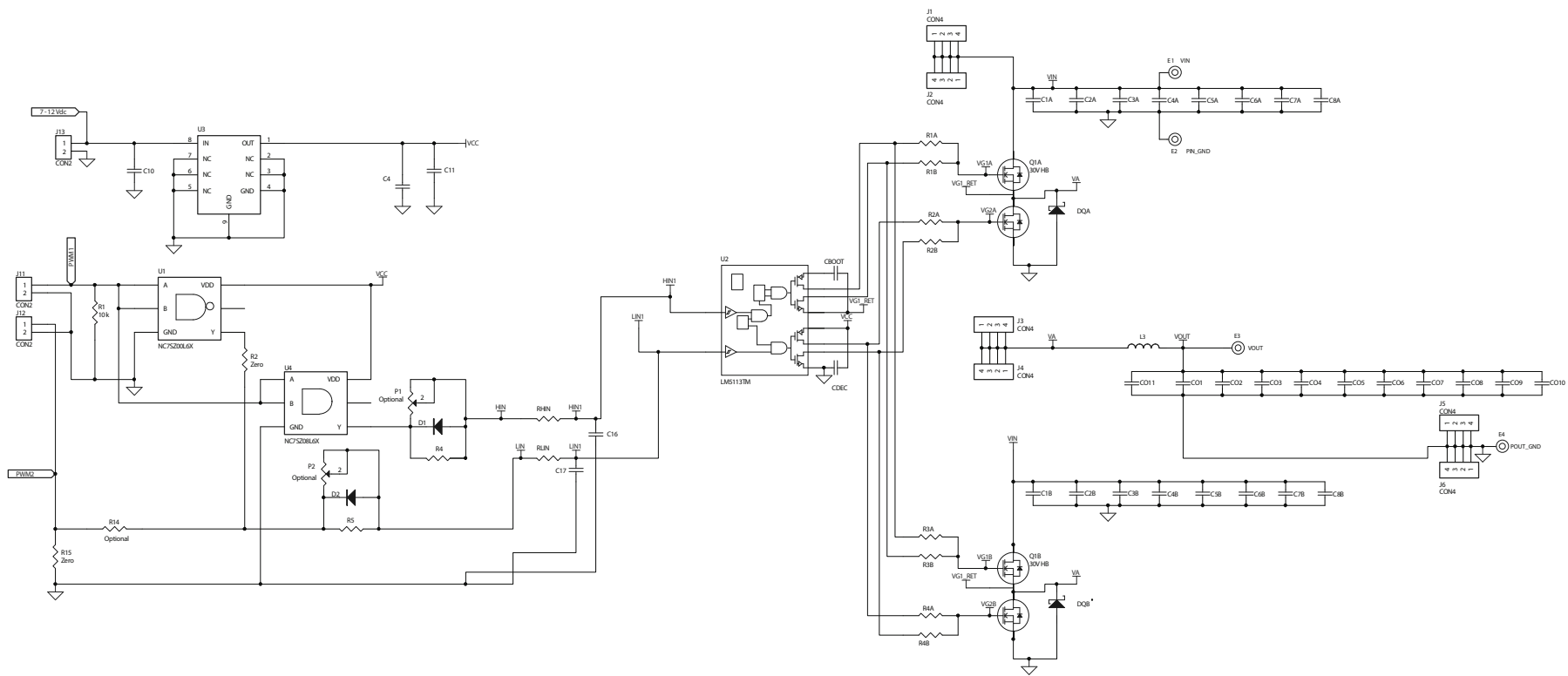


Figure 5: Development Board EPC9059 Schematic

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