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# Development Board EPC9126 Quick Start Guide

*EPC2016C*

*100 V High Current Pulsed Laser Diode Driver*

Revision 2.0



## DESCRIPTION

The EPC9126 development board is primarily intended to drive laser diodes with high current pulses with total pulse widths as low as 5 ns (10% of peak). The board is shipped with an EPC2016C enhancement mode (eGaN<sup>®</sup>) field effect transistor (FET), a 100 V maximum device voltage capable of current pulses up to 75 A. The board does not include a laser diode, which must be supplied by the user.

The EPC9126 is shipped with an EPC2016C ground-referenced eGaN FET driven by a Texas Instruments UCC27611 gate driver. It includes multiple options for mounting laser diodes and can drive these via a discharging capacitor (as shipped) or directly from a power bus. The printed circuit board is designed to minimize the power loop inductance while maintaining mounting flexibility for the laser diode. It includes multiple on-board passive probes for voltages and discharge capacitor current, and equipped with SMA connections for input and sensing designed for 50 ohm measurement systems. In addition, an optional precision narrow pulse generator can be enabled by the user. The main FET footprint can accommodate an EPC2001C 100V eGaN FET with a pulse current rating of up to 150 A for users needing higher current capability. Finally, the board can also be used for other applications requiring a ground-referenced eGaN FET, e.g. Class E amplifiers or similar. A complete block diagram of the circuit is given in figure 1, and a detailed schematic in figure 4.

For more information on the EPC2016C or EPC2001C eGaN FETs, please refer to the datasheets available from EPC at [www.epc-co.com](http://www.epc-co.com). The datasheet should be read in conjunction with this quick start guide.

## SETUP AND OPERATION

Development board EPC9126 is easy to set up to evaluate the performance of the EPC2016C eGaN FET as a laser driver. Refer to figure 2 for connection and measurement setup and follow the procedure below:

1. Review laser safety considerations. Observe all necessary laser safety requirements including the use of personal protection equipment (PPE) as required. Refer to qualified safety personnel as necessary.
2. With power off, install laser diode D3 with the correct polarity following diode manufacturer guidelines. See section Laser Diode Considerations for further information.
3. With power off, connect the input power supply bus to +VBUS (J2) and ground / return to -VBUS (J2).
4. With power off, connect the logic supply (7-12 V VDC) to +V7in (J1) and ground return to -V7in (J1).
5. With power off, connect the signal pulse generator to the input J5. J5 is terminated with 50 Ω on the EPC9126. The signal input can handle up to 0.25 W RMS.
6. Connect the remaining measurement SMA outputs to an oscilloscope, using 50 Ω cables and with the scope inputs set to 50 Ω impedance. See section Measurement Considerations for more information, including the attenuation values for each output.
7. Turn on the logic supply voltage to the required value.

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V <sub>7IN</sub>	Gate drive and logic supply		7		12	V
V <sub>BUS</sub>	Bus Input Voltage Range		0		80*	V
V <sub>COMP</sub>	Input comparator threshold	Input impedance of J5 is 50 Ω		2.5		V
V <sub>INPUT</sub>	Input pulse range		0		5	V
T <sub>Pin</sub>	Input pulse width		6			ns

\* Maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.

**SAFETY WARNING:** This board is capable of driving laser diodes to generate high peak power optical pulses. Such pulses are capable of creating permanent vision damage. User must follow proper laser safety procedures to prevent vision damage.

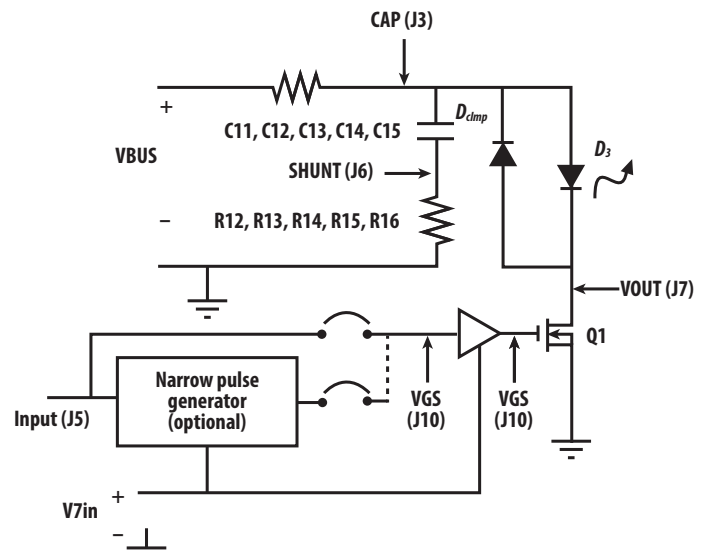


Figure 1: Block diagram of EPC9126 development board

8. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 80 V).
9. Turn on the pulse source and observe switching operation via the outputs and any additional desired probing. Laser diode output may be observed with an appropriate electro-optical receiver.
10. Once operational, adjust the bus voltage, input pulse width, and pulse repetition frequency (PRF) as desired within the operating range and observe the system behavior.
11. For shutdown, please follow steps in reverse.

**NOTE:** Many of the waveforms in the laser driver can have transition speeds well under 1 ns. It is recommended that the scope and probe bandwidth be at least 1 GHz, and for highest waveform fidelity, 2 GHz or higher is preferred. The use of standard scope probes with sub-GHz bandwidths can result in waveforms that appear substantially slower than the actual behavior of the circuit.

## OPERATING PRINCIPLE

The EPC9126 is shipped as a capacitive discharge laser diode driver. Please refer to the block diagram (figure 2) and the schematic (figure 4). It has several possible modifications (section MODIFICATIONS), but only the basic operation will be covered in this section. The EPC9126 basic operating principle is to discharge energy storage capacitance {C11, C12, C13, C14, C15} through the laser diode, and then recharge {C11, C12, C13, C14, C15} through the resistor bank {R2, R3, R5, R6}.

The discharge is controlled via an input pulse that is delivered to SMA connector J5, which is terminated in 50 Ω. As shipped, this pulse is delivered to gate driver U5. When the input goes high, the gate driver turns on Q1, allowing {C11, C12, C13, C14, C15} to discharge through the laser diode D3. When the input goes low, Q1 turns off. If there is current remaining in the power loop, diodes D1, D2 can conduct and help prevent overvoltage of the laser and FET.

Measurements of many of the main waveforms can be made through the SMA test points provided, and additional test points are provided. These test points can provide waveform measurements with equivalent bandwidths up to 3 GHz. As a result, they have requirements and properties that differ from most conventional oscilloscope probes. More details on the usage of these test points is provided in section Measurement Considerations.

## LASER DIODE CONSIDERATIONS

Laser diode D3 (supplied by the user) is mounted on the right-hand side of the EPC9126. The board is designed to accommodate both through-hole laser diodes and surface mount laser diodes. It is designed to allow mounting of laser diodes such that the laser beam can be emitted either perpendicular or parallel to the plane of the PCB. Figure 3 shows some example mounting configurations.

The power loop inductance, including that of the laser diode, is a primary factor that determines the shape of the laser pulse. Considerable effort

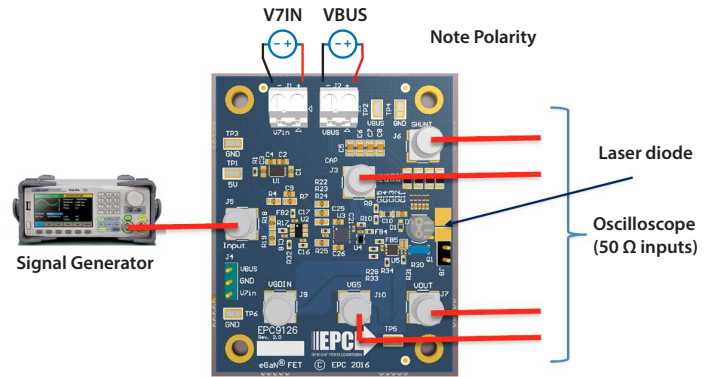


Figure 2: Connection and measurement setup

has been made to minimize power loop inductance while maximizing the choice of laser diode and its orientation. The discharge caps, current sense resistors, and the eGaN FET must all be mounted in close proximity to minimize inductance. As a result, the user must take care not to damage any components when mounting the laser or changing other components in the power loop.

Laser diode current pulses can result in peak powers of several hundred watts. Laser diodes for lidar applications are designed with this in mind, but thermal limitations of the laser package mean that pulse widths, duty cycles, and pulse repetition frequency limitations must be observed. Read laser diode data sheets carefully and follow any manufacturers' recommendations.

This board has been tested with the following laser diodes: SPL PL90 and SPL PL90\_3 from OSRAM Opto Semiconductor (<https://www.osram.com/os/>) and DPEGW1S09H and TPGAD1S09H from Excelitas (<http://www.excelitas.com>).

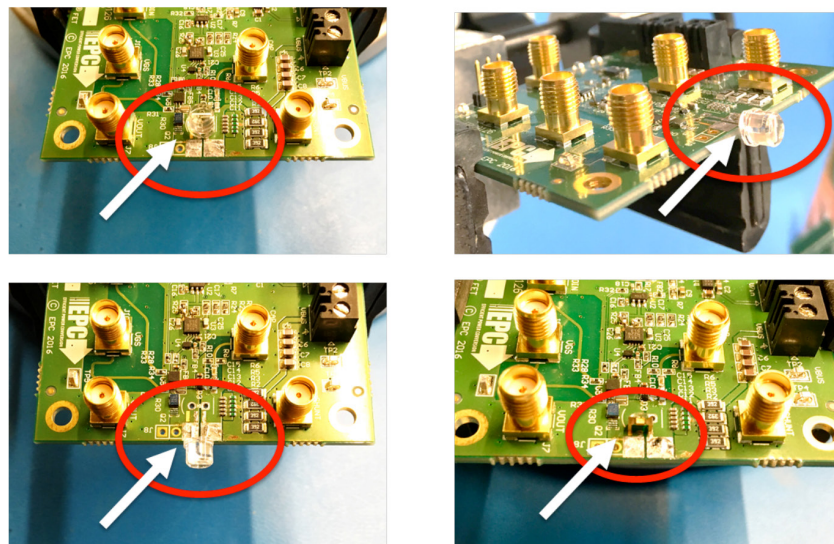


Figure 3: Laser diode mounting options: Leaded laser in standard through-hole position (upper left), edge-mounted leaded laser with both leads top-side (lower left), edge-mounted leaded laser with anode top-side and cathode bottom-side (upper right) and surface-mount laser (lower right).

## MEASUREMENT CONSIDERATIONS

SMA jacks are provided to measure several voltages in the circuit, including gate drive input, Q1 gate voltage, Q1 drain voltage, charge voltage of the energy storage cap, and the sense voltage of the discharge cap current measurement shunt. All measurement points are designed to be terminated in 50 Ω, hence when viewing waveforms, the oscilloscope inputs should be set to a 50 Ω input. Ideally, unused inputs should be also terminated with a 50 Ω load to prevent the probes from creating additional resonances. The Q1 drain voltage and the discharge cap sense voltage have on-board terminations to greatly reduce this effect, and in practice, the remaining resonances may be small or otherwise tolerable. It is recommended that the user verify this for their own requirements.

All sense measurement SMAs, except for the shunt measurement, use the transmission line probe principle to obtain waveform fidelity at sub-ns time scales. They have been verified to produce near-identical results to a Tektronix P9158 3 GHz transmission line probe. As a result of their design, they have a built-in attenuation factor. In addition, the impedance of the probes can be relatively small, and as a result, the test points for high voltage measurements include a DC blocking capacitor. If long pulse widths are used, these test points may yield erroneous results, and an external probe should be used.

The current shunt is designed to estimate the discharge capacitor current. Substantial effort has been made to reduce the inductive effects of the current shunt, but it should be used for estimation only, since the shunt inductance will distort the measured waveforms at the sub-ns time scale. If a more accurate shunt waveform measurement is desired, the shunt resistors may be replaced with ones that provide higher accuracy. This is likely to require higher resistor values, which can contribute to errors in the capacitor voltage measurement and in increased power dissipation. Finally, note that the capacitor current also includes the current due to D1, D2, and PCB capacitance.

Table 2 summarizes the properties of the SMA test points for ease of reference.

**Table 2: Properties of SMA test points**

Designator	PCB label	Description	Attenuation factor	DC blocking cap	LF time constant	Internal 50 Ω termination
J3	CAP	Discharge capacitor voltage (VCHARGE on schematic)	41 V/V	10 nF	10 μs	YES
J6	SHUNT	Discharge shunt voltage	22.7 A/V	NO	N/A	NO
J7	V <sub>OUT</sub>	Q1 drain voltage	41 V/V	10 nF	10 μs	YES
J9	VGDIN	Gate drive input	20	NO	N/A	NO
J10	VGS	Q1 gate voltage	20	NO	N/A	NO

## MODIFICATIONS

### Narrow pulse generator:

Many signal generators cannot produce an accurate, short pulse. The EPC9126 includes a narrow pulse generator based on the Linear Technologies LT1720 ultrafast dual comparator. This pulse generator requires an input pulse of at least 20 ns, and will produce a shorter pulse of fixed duration, independent of the length of the input pulse. To use the pulse generator instead of directly using the input pulse, remove 0 Ω resistors R32 and R33 (remove both to prevent unwanted reflections at either gate driver or input comparator), and add a 0 Ω resistor to the empty footprint for R28.

The internal pulse generator ships with a pulse width of ~8 ns. R22, R23, and R24 can be changed to change the pulse width. Increasing the combined value of R22, R23, and R24 will shorten the output pulse, and decreasing the combined value will lengthen it.

### Other modifications:

While diodes D1 and D2 can provide some protection to FET Q1 and laser D3, they have parasitic inductance and capacitance that can reduce performance at the very fastest speeds. If the protection is not needed, they can be removed.

The value of the shunt resistors can be increased up to a point to improve the discharge cap current sense accuracy. Note that accurate measurement of current while inserting extremely low inductance into the power loop is extremely challenging, and many factors must be considered. For the lowest possible inductance, the resistors can be mounted upside down or replaced with copper foil if no sensing is needed.

The footprint for Q1 can accommodate the EPC2001C eGaN FET if higher currents are desired. The higher gate charge of the larger FET will reduce the maximum speed, but will approximately double the current capability. For information on changing the FET, please see <http://epc-co.com/epc/DesignSupport/AssemblyResources.aspx>.

The value of the energy storage cap {C11, C12, C13, C14, C15} can be modified as desired, as well as the recharge resistor {R2, R3, R5, R6}. In the extreme case, the resistor may be reduced to 0 Ω for cases where a capacitive discharge pulse is not desired.

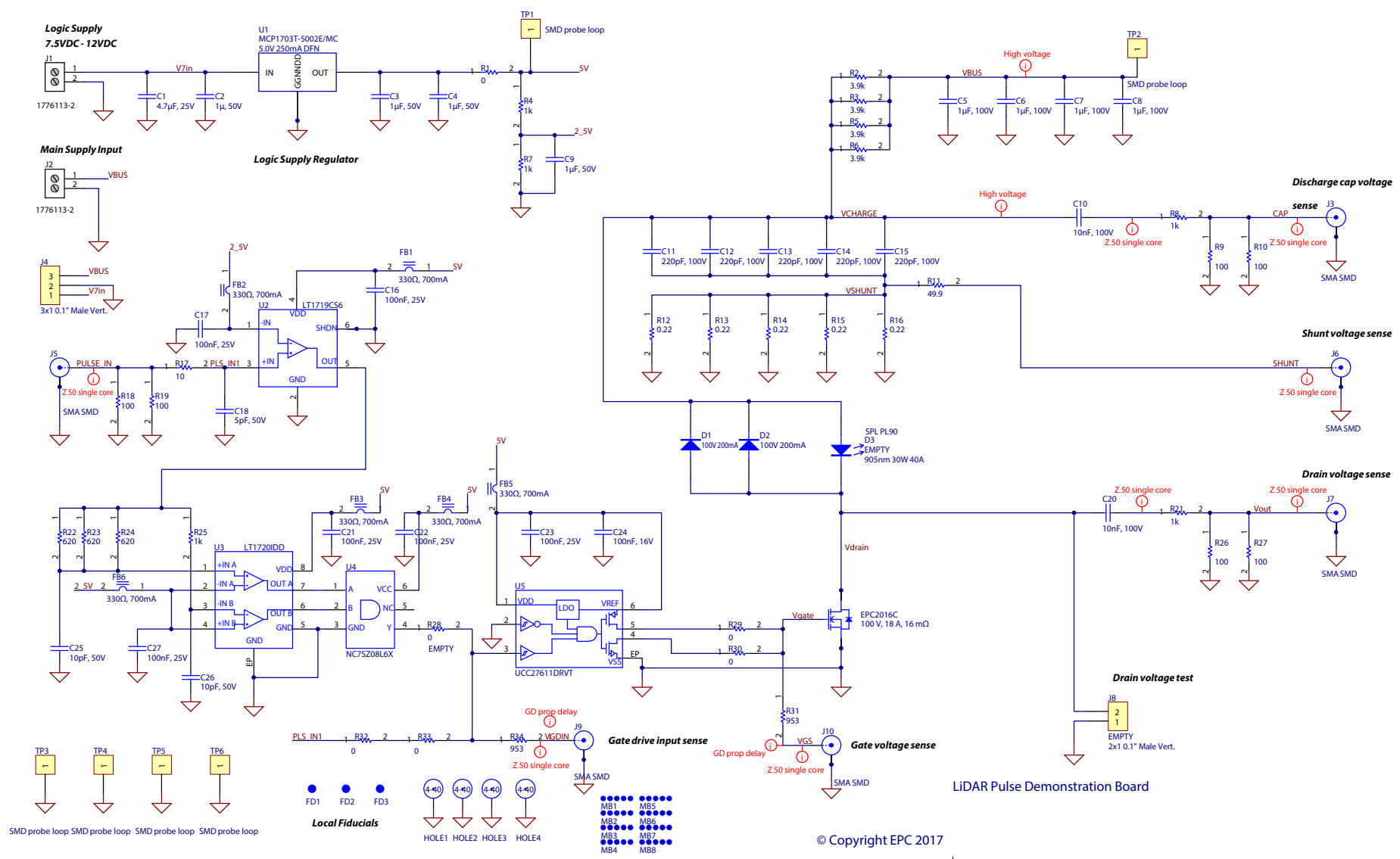


Figure 4: Full schematic EPC9126.

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LiDAR Pulse Demonstration Board

**Table 3: Bill of Materials - EPC9126**

Reference	Part Description	Q uantity	Man ufact urer Part #
C1	4.7 $\mu$ F, 25 V, X5R 0603	1	C1608X5R1E475K080AC
C2, C3, C4, C9	1 $\mu$ F, 25 V, X7R 0603	4	UMK107AB7105KA-T
C5, C6, C7, C8	1 $\mu$ F, 100 V, X7S 0805 TDK	4	CGA4J3X7S2A105K125AE
C10, C20	10 nF, 100 V, C0G 0603 TDK	2	C1608C0G2A103J080AC
C11, C12, C13, C14, C15	220 pF, 100 V, C0G 0402 TDK	5	C1005C0G2A221J050BA
C16, C17, C21, C22, C23, C27	100 nF, 25 V, X7R 0402	6	C1005X7R1E104K050BB
C18	5pF, 50 V, C0G 0402	1	C1005C0G1H050C050BA
C24	100 nF, 16 V, X7R 0306	1	C0816X7R1C104M050AC
C25, C26	100 nF, 25 V, X7R 0402	2	GCM1885C1H100JA16D
D1, D2	Schottky 100 V, 200 mA	2	BAT41KFILM
D3	Laser diode, 30 W, peak 905 nm	1	EMPTY
FB1, FB2, FB3, FB4, FB5, FB6	330 $\Omega$ , 700 mA, ferrite bead TDK 0402	6	MPZ1005S331ET000
J1, J2	Terminal block screw type THT 2-position 3.81 mm pitch	2	1776113-2
J3, J5, J6, J7, J9, J10	SMA jack straight SM	6	Molex 73251-1350
J4	.1 Male Vert."	1	68001-236HLF
J8	.1 Male Vert."	1	EMPTY
Q1	100 V, 18 A, 16 m $\Omega$	1	EPC2016C
R1, R32, R33	Size 0402	3	ERJ-2GE0R00X
R2, R3, R5, R6	3.9 k, 5%, 0.67 W, 1206 resistor	4	ERJ-P08J392V
R4, R7, R25	1 k resistor 0603 1%	3	RMCF0603FT1K00
R8, R21	Vishay PHP 0603 wide resistor	2	PHP00603E1001BST1
R9, R10, R26, R27	Size 0402	4	ERJ-2RKF1000X
R11	Size 0402	1	ERJ-2RKF49R9X
R12, R13, R14, R15, R16	Size 0402	5	RL0510S-R22-F
R17	Size 0402	1	ERJ-2RKF10R0X
R18, R19	100 $\Omega$ 0603	2	MCT0603MC1000FP500
R22, R23, R24	620 resistor 0603 1%	3	RMCF0603FT620R
R28	Size 0402	1	EMPTY
R29, R30	Size 0201	2	RC0603J000CS
R31, R34	Size 0402	2	ERJ-2RKF9530X
TP1, TP2, TP3, TP4, TP5, TP6	SMD probe loop	6	Keystone, 5015
$\mu$ 1	5 V, 250 mA, DFN	1	MCP1703T-5002E/MC
$\mu$ 2	Dual 4.5 ns comparator RRO	1	LT1719CS6
$\mu$ 3	Dual 4.5 ns comparator RRO	1	LT1720IDD
$\mu$ 4	TinyLogic UHS 2 input AND	1	NC7SZ08L6X
$\mu$ 5	eGaN gate driver with LDO	1	UCC27611DRVT

## For More Information:

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