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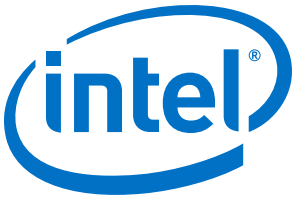

Quad-Serial Configuration (EPCQ) Devices Datasheet

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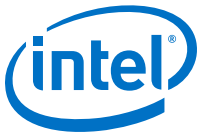


1. Quad-Serial Configuration (EPCQ) Devices Datasheet

This datasheet describes quad-serial configuration (EPCQ) devices. EPCQ is an in-system programmable NOR flash memory.

1.1. Supported Devices

Table 1. Supported Intel EPCQ Devices

Note: EPCQ devices are scheduled for product obsolescence and discontinued support as described in PDN1708 and PDN1802. Intel® recommends that you use the EPCQ-A configuration devices.

Device	Memory Size (bits)	On-Chip Decompression Support	ISP Support	Cascading Support	Reprogrammable	Recommended Operating Voltage (V)
EPCQ16	16,777,216	No	Yes	No	Yes	3.3
EPCQ32	33,554,432	No	Yes	No	Yes	3.3
EPCQ64	67,108,864	No	Yes	No	Yes	3.3
EPCQ128	134,217,728	No	Yes	No	Yes	3.3
EPCQ256	268,435,456	No	Yes	No	Yes	3.3
EPCQ512/A (1)	536,870,912	No	Yes	No	Yes	3.3

Related Information

- PDN1708
  Product discontinuance notification.
- PDN1802
  Product discontinuance notification.
- AN822: Intel Configuration Device Migration Guideline
  Provides more information about migrating EPCQ to EPCQ-A devices.
- Quad-Serial Configuration (EPCQ-A) Devices Datasheet

(1) EPCQ512/A is shown in the Intel Quartus® Prime software as EPCQ512.

1.2. Features

EPCQ devices offer the following features:

- Serial or quad-serial FPGA configuration in devices that support active serial (AS) x1 or AS x4 configuration schemes(2)
- Low cost, low pin count, and non-volatile memory
- 2.7-V to 3.6-V operation
- Available in 8- or 16- small-outline integrated circuit (SOIC) package
- Reprogrammable memory with up to 100,000 erase or program cycles
- Write protection support for memory sectors using status register bits
- Fast read, extended dual input fast read, and extended quad input fast read of the entire memory using a single operation code
- Write bytes, extended dual input fast write bytes, and extended quad input fast write bytes of the entire memory using a single operation code
- Reprogrammable with an external microprocessor using the SRunner software driver
- In-system programming (ISP) support with the SRunner software driver
- ISP support with Intel FPGA Download CableIntel FPGA Download Cable II, Intel FPGA Ethernet Cable
- By default, the memory array is erased and the bits are set to 1
- More than 20 years data retention

Related Information

Errata Sheet for EPCQ Devices

1.3. Operating Conditions

Tables in this section list information about the absolute maximum ratings, recommended operating conditions, DC operating conditions, I_{CC} supply current, and capacitance for EPCQ devices.

Note: The values of the tables in this section are finalized for EPCQ16, EPCQ32, EPCQ64, EPCQ128, EPCQ256, and EPCQ512/A devices. The operating conditions for all of these devices are the same unless indicated otherwise.

1.3.1. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–0.6	4	V
V_I (3)	DC input voltage	With respect to GND	–0.6	4	V
					continued...

(2) AS x4 is not supported in EPCQ512 devices. Refer to the *Errata Sheet for EPCQ Devices* for more information.

Symbol	Parameter	Condition	Min	Max	Unit
I_{MAX}	DC V_{CC} or GND current	—	—	20	mA
I_{OUT}	DC output current per pin	—	–25	25	mA
P_D	Power dissipation	—	—	72	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	Under bias	—	125	°C

1.3.2. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply voltage	(4)	2.7	3.6	V
V_I	Input voltage	With respect to GND	-0.5	0.4 + V_{CC}	V
V_O	Output voltage	—	0	V_{CC}	V
T_A (5)	Operating temperature	For industrial use	-40	85	°C
t_R	Input rise time for all devices except EPCQ512/A	—	—	5	ns
	Input rise time for EPCQ512/A	—	—	1.5	ns
t_F	Input fall time for all devices except EPCQ512/A	—	—	5	ns
	Input fall time for EPCQ512/A	—	—	1.5	ns

Related Information

EPCQ Package and Thermal Resistance
Provides more information about EPCQ thermal resistance.

1.3.3. DC Operating Conditions

Table 4. DC Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High-level input voltage	—	0.7 x VCC	VCC + 0.4	V
V_{IL}	Low-level input voltage	—	-0.5	0.3 x V_{CC}	V
V_{OH}	High-level output voltage	I_{OH} = -100 µA (6)	V_{CC} - 0.2	—	V

continued...

(3) For periods of less than 2 ns, V_{IL} can undershoot to –1.0 V and V_{IH} can overshoot to V_{CC} + 1.0 V.

(4) The maximum V_{CC} rise time is 100 ms.

(5) EPCQ devices can be paired with Intel FPGA industrial-grade FPGAs operating at junction temperatures up to 100°C as long as the ambient temperature does not exceed 85°C.

(6) The I_{OH} parameter refers to the high-level TTL or CMOS output current.

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA (7)	—	0.4	V
I_I	Input leakage current	V_I =V_{CC} or GND	-10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	-10	10	µA

1.3.4. ICC Supply Current

Table 5. I_{CC} Supply Current

Symbol	Parameter	Condition	Min	Max	Unit
I_{CC0}	V_{CC} supply current	Standby	—	100	µA
I_{CC1}	V_{CC} supply current for all devices except EPCQ512/A	During active power mode	5	20	mA
	V_{CC} supply current for EPCQ512/A		—	60	mA

1.3.5. Capacitance

Table 6. Capacitance

Capacitance is sample-tested only at T_A = 25 x C and at a 54 MHz frequency.

Symbol	Parameter	Condition	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} =0 V	—	6	pF
C_{OUT}	Output pin capacitance	V_{OUT} =0 V	—	8	pF

1.4. Memory Array Organization

Table 7. Supported Memory Array Organization in EPCQ Devices

Details	EPCQ16	EPCQ32	EPCQ64	EPCQ128	EPCQ256	EPCQ512/A
Bytes	2,097,152 bytes [16 megabits (Mb)]	4,194,304 bytes (32 Mb)	8,388,608 bytes (64 Mb)	16,777,216 bytes (128 Mb)	33,554,432 bytes (256 Mb)	67,108,864 bytes (512 Mb)
Number of sectors	32	64	128	256	512	1,024
Bytes per sector	65,536 bytes [512 kilobits (Kb)]					
Total numbers of subsectors (8)	512	1,024	2,048	4,096	8,192	16,384
Bytes per subsector	4,096 bytes (32 Kb)					

continued...

(7) The I_{OL} parameter refers to the low-level TTL or CMOS output current.

(8) Every sector is further divided into 16 subsectors with 4 KB of memory. Therefore, there are 512 (32 x 16) subsectors for the EPCQ16 device, 1,024 (64 x 16) subsectors for the EPCQ32 device, 2,048 (128 x 16) subsectors for the EPCQ64 device, 4,096 (256 x 16) subsectors for the EPCQ128 device, 8,192 (512 x 16) subsectors for the EPCQ256 device, and 16,384 (1,024 x 16) subsectors for the EPCQ512/A device.

Details	EPCQ16	EPCQ32	EPCQ64	EPCQ128	EPCQ256	EPCQ512/A
Pages per sector	256					
Total number of pages	8,192	16,384	32,768	65,536	131,072	262,144
Bytes per page	256 bytes					

1.4.1. Address Range for EPCQ16

Table 8. Address Range for Sectors 31..0 and Subsectors 511..0 in EPCQ16 Devices

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
31	511	1FF000	1FFFFF
	510	1FE000	1FEFFF
	.	.	.
	498	1F2000	1F2FFF
	497	1F1000	1F1FFF
	496	1F0000	1F0FFF
30	495	1EF000	1EFFFF
	494	1EE000	1EEFFF
	.	.	.
	482	1E2000	1E2FFF
	481	1E1000	1E1FFF
	480	1E0000	1E0FFF
1	31	1F000	1FFFF
	30	1E000	1EFFF
	.	.	.
	18	12000	12FFF
	17	11000	11FFF
	16	10000	10FFF
0	15	F000	FFFF
	14	E000	EFFF
	.	.	.
	2	2000	2FFF
	1	1000	1FFF
	0	H'0000000	H'0000FFF

1.4.2. Address Range for EPCQ32

Table 9. Address Range for Sectors 63..0 and Subsectors 1023..0 in EPCQ32 Devices

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
63	1023	3FF000	3FFFFF
	1022	3FE000	3FEFFF
	.	.	.
	1010	3F2000	3F2FFF
	1009	3F1000	3F1FFF
	1008	3F0000	3F0FFF
62	1007	3EF000	3EFFFF
	1006	3EE000	3EEFFF
	.	.	.
	994	3E2000	3E2FFF
	993	3E1000	3E1FFF
	992	3E0000	3E0FFF
1	31	1F000	1FFFF
	30	1E000	1EFFF
	.	.	.
	18	12000	12FFF
	17	11000	11FFF
	16	10000	10FFF
0	15	F000	FFFF
	14	E000	EFFF
	.	.	.
	2	2000	2FFF
	1	1000	1FFF
	0	H'0000000	H'0000FFF

1.4.3. Address Range for EPCQ64

Table 10. Address Range for Sectors 127..0 and Subsectors 2047..0 in EPCQ64 Devices

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
127	2047	7FF000	7FFFFF
	2046	7FE000	7FEFFF
	.	.	.

continued...

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
	2034	7F2000	7F2FFF
	2033	7F1000	7F1FFF
	2032	7F0000	7F0FFF
64	1039	40F000	40FFFF
	1038	40E000	40EFFF
	.	.	.
	1026	402000	402FFF
	1025	401000	401FFF
	1024	400000	400FFF
63	1023	3FF000	3FFFFF
	1022	3FE000	3FEFFF
	.	.	.
	1010	3F2000	3F2FFF
	1009	3F1000	3F1FFF
	1008	3F0000	3F0FFF
62	1007	3EF000	3EFFFF
	1006	3EE000	3EEFFF
	.	.	.
	994	3E2000	3E2FFF
	993	3E1000	3E1FFF
	992	3E0000	3E0FFF
1	31	1F000	1FFFF
	30	1E000	1EFFF
	.	.	.
	18	12000	12FFF
	17	11000	11FFF
	16	10000	10FFF
0	15	F000	FFFF
	14	E000	EFFF
	.	.	.
	2	2000	2FFF
	1	1000	1FFF
	0	H'0000000	H'0000FFF

1.4.4. Address Range for EPCQ128

Table 11. Address Range for Sectors 255..0 and Subsectors 4095..0 in EPCQ128 Devices

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
255	4095	FFF000	FFFFFF
	4094	FFE000	FFEFFF
	.	.	.
	4082	FF2000	FF2FFF
	4081	FF1000	FF1FFF
	4080	FF0000	FF0FFF
254	4079	FEF000	FEFFFF
	4078	FEE000	FEEFFF
	.	.	.
	4066	FE2000	FE2FFF
	4065	FE1000	FE1FFF
	4064	FE0000	FE0FFF
129	2079	81F000	81FFFF
	2078	81E000	81EFFF
	.	.	.
	2066	812000	812FFF
	2065	811000	811FFF
	2064	810000	810FFF
128	2063	80F000	80FFFF
	2062	80E000	80EFFF
	.	.	.
	2050	802000	802FFF
	2049	801000	801FFF
	2048	800000	800FFF
127	2047	7FF000	7FFFFF
	2046	7FE000	7FEFFF
	.	.	.
	2034	7F2000	7F2FFF
	2033	7F1000	7F1FFF
	2032	7F0000	7F0FFF

continued...

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
64	1039	40F000	40FFFF
	1038	40E000	40EFFF
	.	.	.
	1026	402000	402FFF
	1025	401000	401FFF
	1024	400000	400FFF
63	1023	3FF000	3FFFFF
	1022	3FE000	3FEFFF
	.	.	.
	1010	3F2000	3F2FFF
	1009	3F1000	3F1FFF
	1008	3F0000	3F0FFF
62	1007	3EF000	3EFFFF
	1006	3EE000	3EEFFF
	.	.	.
	994	3E2000	3E2FFF
	993	3E1000	3E1FFF
	992	3E0000	3E0FFF
1	31	1F000	1FFFF
	30	1E000	1EFFF
	.	.	.
	18	12000	12FFF
	17	11000	11FFF
	16	10000	10FFF
0	15	F000	FFFF
	14	E000	EFFF
	.	.	.
	2	2000	2FFF
	1	1000	1FFF
	0	H'0000000	H'0000FFF

1.4.5. Address Range for EPCQ256

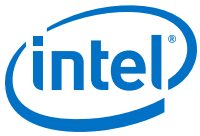
Table 12. Address Range for Sectors 511..0 and Subsectors 8191..0 in EPCQ256 Devices

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
511	8191	1FFF000	1FFFFFF
	8190	1FFE000	1FFEFFF
	.	.	.
	8178	1FF2000	1FF2FFF
	8177	1FF1000	1FF1FFF
	8176	1FF0000	1FF0FFF
510	8175	1FEF000	1FEFFFF
	8174	1FEE000	1FEEFFF
	.	.	.
	8162	1FE2000	1FE2FFF
	8161	1FE1000	1FE1FFF
	8160	1FE0000	1FE0FFF
257	4127	101F000	101FFFF
	4126	101E000	101EFFF
	.	.	.
	4114	1012000	1012FFF
	4113	1011000	1011FFF
	4112	1010000	1010FFF
256	4111	100F000	100FFFF
	4110	100E000	100EFFF
	.	.	.
	4098	1002000	1002FFF
	4097	1001000	1001FFF
	4096	1000000	1000FFF
255	4095	FFF000	FFFFFF
	4094	FFE000	FFEFFF
	.	.	.
	4082	FF2000	FF2FFF
	4081	FF1000	FF1FFF
	4080	FF0000	FF0FFF

continued...

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
254	4079	FEF000	FEFFFF
	4078	FEE000	FEEFFF
	.	.	.
	4066	FE2000	FE2FFF
	4065	FE1000	FE1FFF
	4064	FE0000	FE0FFF
129	2079	81F000	81FFFF
	2078	81E000	81EFFF
	.	.	.
	2066	812000	812FFF
	2065	811000	811FFF
	2064	810000	810FFF
128	2063	80F000	80FFFF
	2062	80E000	80EFFF
	.	.	.
	2050	802000	802FFF
	2049	801000	801FFF
	2048	800000	800FFF
127	2047	7FF000	7FFFFF
	2046	7FE000	7FEFFF
	.	.	.
	2034	7F2000	7F2FFF
	2033	7F1000	7F1FFF
	2032	7F0000	7F0FFF
64	1039	40F000	40FFFF
	1038	40E000	40EFFF
	.	.	.
	1026	402000	402FFF
	1025	401000	401FFF
	1024	400000	400FFF
63	1023	3FF000	3FFFFF
	1022	3FE000	3FEFFF
	.	.	.

continued...



Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
	1010	3F2000	3F2FFF
	1009	3F1000	3F1FFF
	1008	3F0000	3F0FFF
62	1007	3EF000	3EFFFF
	1006	3EE000	3EEFFF
	.	.	.
	994	3E2000	3E2FFF
	993	3E1000	3E1FFF
	992	3E0000	3E0FFF
1	31	1F000	1FFFF
	30	1E000	1EFFF
	.	.	.
	18	12000	12FFF
	17	11000	11FFF
	16	10000	10FFF
0	15	F000	FFFF
	14	E000	EFFF
	.	.	.
	2	2000	2FFF
	1	1000	1FFF
	0	H'0000000	H'0000FFF

1.4.6. Address Range for EPCQ512/A

Table 13. Address Range for Sectors 1023..0 and Subsectors 16383..0 in EPCQ512/A Devices

Sector	Subsector	Address Range (Byte Addresses in HEX)	
		Start	End
1023	16383	3FFF000	3FFFFFF
	.	.	.
	16368	3FF0000	3FF0FFF
.	.	.	.
511	8191	1FFF000	1FFFFFF
	.	.	.
	8176	FF0000	1FF0FFF
.	.	.	.
255	4095	FFF000	FFFFFF
	.	.	.
	4080	FF0000	FF0FFF
.	.	.	.
127	2047	7FF000	7FFFFF
	.	.	.
	2032	7F0000	7F0FFF
.	.	.	.
63	1023	3FF000	3FFFFF
	.	.	.
	1008	3F0000	3F0FFF
.	.	.	.
0	15	F000	FFFF
	.	.	.
	0	H'0000000	H'0000FFF

1.5. Memory Operations

This section describes the operations that you can use to access the memory in EPCQ devices. When performing the operation, addresses and data are shifted in and out of the device serially, with the MSB first.

1.5.1. Timing Requirements

When the active low chip select (nCS) signal is driven low, shift in the operation code into the EPCQ device using the serial data (DATA) pin. Each operation code bit is latched into the EPCQ device on the rising edge of the DCLK.

While executing an operation, shift in the desired operation code, followed by the address or data bytes. See related information for more information about the address and data bytes. The device must drive the nCS pin high after the last bit of the operation sequence is shifted in.

For read operations, the data read is shifted out on the DATA pin. You can drive the nCS pin high when any bit of the data is shifted out.

For write and erase operations, drive the nCS pin high at a byte boundary, that is in a multiple of eight clock pulses. Otherwise, the operation is rejected and not executed.

All attempts to access the memory contents while a write or erase cycle is in progress are rejected, and the write or erase cycle continues unaffected.

1.5.2. Addressing Mode

The 3-byte addressing mode is enabled by default. To access the EPCQ256 or EPCQ512/A memory, you must use the 4-byte addressing mode. In 4-byte addressing mode, the address width is 32-bit address. To enable the 4-byte addressing mode, you must execute the 4BYTEADDREN operation. This addressing mode takes effect immediately after you execute the 4BYTEADDREN operation and remains active in the subsequent power-ups. To disable the 4-byte addressing mode, you must execute the 4BYTEADDREX operation.

Note: If you are using the Intel Quartus Prime software or the SRunner software to program the EPCQ256 or EPCQ512/A device, you do not need to execute the 4BYTEADDREN operation. The Intel Quartus Prime software enables the 4-byte addressing mode when programming the device automatically.

1.6. Registers

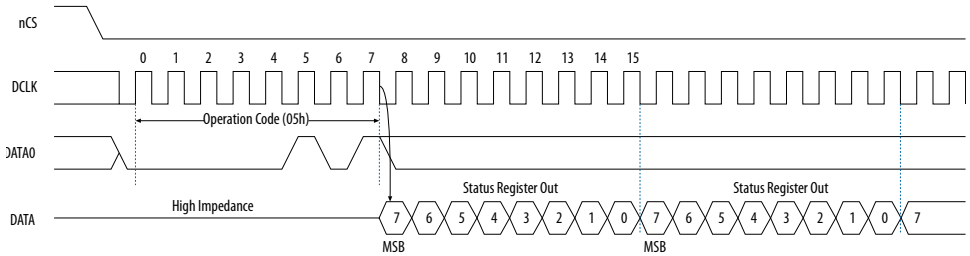
1.6.1. Status Register

Table 14. Status Register Bits

Bit	R/W	Default Value	Name	Value	Description
7	R/W	0	None		
6	R/W	0	BP3 (Block Protect Bit)[9] [10]	Table 15 on page 19 through Table 26 on page 24 list the protected area with reference to the block protect bits.	Determine the area of the memory protected from being written or erased unintentionally.
5	R/W	0	TB (Top/Bottom Bit)	• 1=Protected area starts from the bottom of the memory array. • 0=Protected area starts from the top of the memory array.	Determine that the protected area starts from the top or bottom of the memory array.
4	R/W	0	BP2[9]	Table 15 on page 19 through Table 26 on page 24 list the protected area with reference to the block protect bits.	Determine the area of the memory protected from being written or erased unintentionally.
3			BP1[9]		
2			BP0[9]		
1	R	0	WEL (Write Enable Latch Bit)	• 1=Allows the following operation to run: — Write Bytes — Write Status Register — Erase Bulk — Erase Die — Erase Sector • 0=Rejects the above mentioned operations.	Allows or rejects certain operation to run.
0	R	0	WIP (Write in Progress Bit)	• 1=One of the following operation is in progress: — Write Status Register — Write NVCR — Write Bytes — Erase • 0=no write or erase cycle in progress	Indicates if there is a command in progress.

1.6.1.1. Read Status Register Operation (05h)

Figure 1. Read Status Operation Timing Diagram



(9) The erase bulk and erase die operation is only available when all the block protect bits are set to 0. When any of the block protect bits are set to 1, the relevant area is protected from being written by a write bytes operation or erased by an erase sector operation.

(10) Applicable for EPCQ64, EPCQ128, EPCQ256, and EPCQ512/A devices only.

1.6.1.1.1. Block Protection Bits in EPCQ16 when TB Bit is Set to 0

Table 15. Block Protection Bits in EPCQ16 when TB Bit is Set to 0

Status Register Content				Memory Content	
TB Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	0	None	All sectors
0	0	0	1	Sector 31	Sectors (0 to 30)
0	0	1	0	Sectors (30 to 31)	Sectors (0 to 29)
0	0	1	1	Sectors (28 to 31)	Sectors (0 to 27)
0	1	0	0	Sectors (24 to 31)	Sectors (0 to 23)
0	1	0	1	Sectors (16 to 31)	Sectors (0 to 15)
0	1	1	0	All sectors	None
0	1	1	1	All sectors	None

1.6.1.1.2. Block Protection Bits in EPCQ16 when TB Bit is Set to 1

Table 16. Block Protection Bits in EPCQ16 when TB Bit is Set to 1

Status Register Content				Memory Content	
TB Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
1	0	0	0	None	All sectors
1	0	0	1	Sector 0	Sectors (1 to 31)
1	0	1	0	Sectors (0 to 1)	Sectors (2 to 31)
1	0	1	1	Sectors (0 to 3)	Sectors (4 to 31)
1	1	0	0	Sectors (0 to 7)	Sectors (8 to 31)
1	1	0	1	Sectors (0 to 15)	Sectors (16 to 31)
1	1	1	0	All sectors	None
1	1	1	1	All sectors	None

1.6.1.1.3. Block Protection Bits in EPCQ32 when TB Bit is Set to 0

Table 17. Block Protection Bits in EPCQ32 when TB Bit is Set to 0

Status Register Content				Memory Content	
TB Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	0	None	All sectors
0	0	0	1	Sector 63	Sectors (0 to 62)
0	0	1	0	Sectors (62 to 63)	Sectors (0 to 61)
0	0	1	1	Sectors (60 to 63)	Sectors (0 to 59)
0	1	0	0	Sectors (56 to 63)	Sectors (0 to 55)

continued...

Status Register Content				Memory Content	
TB Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	1	0	1	Sectors (48 to 63)	Sectors (0 to 47)
0	1	1	0	Sectors (32 to 63)	Sectors (0 to 31)
0	1	1	1	All sectors	None

1.6.1.1.4. Block Protection Bits in EPCQ32 when TB Bit is Set to 1

Table 18. Block Protection Bits in EPCQ32 when TB Bit is Set to 1

Status Register Content				Memory Content	
TB Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
1	0	0	0	None	All sectors
1	0	0	1	Sector 0	Sectors (1 to 63)
1	0	1	0	Sectors (0 to 1)	Sectors (2 to 63)
1	0	1	1	Sectors (0 to 3)	Sectors (4 to 63)
1	1	0	0	Sectors (0 to 7)	Sectors (8 to 63)
1	1	0	1	Sectors (0 to 15)	Sectors (16 to 63)
1	1	1	0	Sectors (0 to 31)	Sectors (32 to 63)
1	1	1	1	All sectors	None

1.6.1.1.5. Block Protection Bits in EPCQ64 when TB Bit is Set to 0

Table 19. Block Protection Bits in EPCQ64 when TB Bit is Set to 0

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	0	0	None	All sectors
0	0	0	0	1	Sector 127	Sectors (0 to 126)
0	0	0	1	0	Sectors (126 to 127)	Sectors (0 to 125)
0	0	0	1	1	Sectors (124 to 127)	Sectors (0 to 123)
0	0	1	0	0	Sectors (120 to 127)	Sectors (0 to 119)
0	0	1	0	1	Sectors (112 to 127)	Sectors (0 to 111)
0	0	1	1	0	Sectors (96 to 127)	Sectors (0 to 95)
0	0	1	1	1	Sectors (64 to 127)	Sectors (0 to 63)
0	1	0	0	0	All sectors	None
0	1	0	0	1	All sectors	None
0	1	0	1	0	All sectors	None
0	1	0	1	1	All sectors	None
0	1	1	0	0	All sectors	None

continued...

Status Register Content					Memory Content	
TB Bit	**BP3 Bit**	**BP2 Bit**	**BP1 Bit**	**BP0 Bit**	**Protected Area**	**Unprotected Area**
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

1.6.1.1.6. Block Protection Bits in EPCQ64 when TB Bit is Set to 1

Table 20. Block Protection Bits in EPCQ64 when TB Bit is Set to 1

Status Register Content					Memory Content	
TB Bit	**BP3 Bit**	**BP2 Bit**	**BP1 Bit**	**BP0 Bit**	**Protected Area**	**Unprotected Area**
1	0	0	0	0	None	All sectors
1	0	0	0	1	Sector 0	Sectors (1 to 127)
1	0	0	1	0	Sectors (0 to 1)	Sectors (2 to 127)
1	0	0	1	1	Sectors (0 to 3)	Sectors (4 to 127)
1	0	1	0	0	Sectors (0 to 7)	Sectors (8 to 127)
1	0	1	0	1	Sectors (0 to 15)	Sectors (16 to 127)
1	0	1	1	0	Sectors (0 to 31)	Sectors (32 to 127)
1	0	1	1	1	Sectors (0 to 63)	Sectors (64 to 127)
1	1	0	0	0	All sectors	None
1	1	0	0	1	All sectors	None
1	1	0	1	0	All sectors	None
1	1	0	1	1	All sectors	None
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None

1.6.1.1.7. Block Protection Bits in EPCQ128 when TB Bit is Set to 0

Table 21. Block Protection Bits in EPCQ128 when TB Bit is Set to 0

Status Register Content					Memory Content	
TB Bit	**BP3 Bit**	**BP2 Bit**	**BP1 Bit**	**BP0 Bit**	**Protected Area**	**Unprotected Area**
0	0	0	0	0	None	All sectors
0	0	0	0	1	Sector 255	Sectors (0 to 254)
0	0	0	1	0	Sectors (254 to 255)	Sectors (0 to 253)
0	0	0	1	1	Sectors (252 to 255)	Sectors (0 to 251)
0	0	1	0	0	Sectors (248 to 255)	Sectors (0 to 247)
0	0	1	0	1	Sectors (240 to 255)	Sectors (0 to 239)

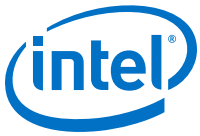
continued...

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	1	1	0	Sectors (224 to 255)	Sectors (0 to 223)
0	0	1	1	1	Sectors (192 to 255)	Sectors (0 to 191)
0	1	0	0	0	Sectors (128 to 255)	Sectors (0 to 127)
0	1	0	0	1	All sectors	None
0	1	0	1	0	All sectors	None
0	1	0	1	1	All sectors	None
0	1	1	0	0	All sectors	None
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

1.6.1.1.8. Block Protection Bits in EPCQ128 when TB Bit is Set to 1

Table 22. Block Protection Bits in EPCQ128 when TB Bit is Set to 1

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
1	0	0	0	0	None	All sectors
1	0	0	0	1	Sector 0	Sectors (1 to 255)
1	0	0	1	0	Sectors (0 to 1)	Sectors (2 to 255)
1	0	0	1	1	Sectors (0 to 3)	Sectors (4 to 255)
1	0	1	0	0	Sectors (0 to 7)	Sectors (8 to 255)
1	0	1	0	1	Sectors (0 to 15)	Sectors (16 to 255)
1	0	1	1	0	Sectors (0 to 31)	Sectors (32 to 255)
1	0	1	1	1	Sectors (0 to 63)	Sectors (64 to 255)
1	1	0	0	0	Sectors (0 to 127)	Sectors (128 to 255)
1	1	0	0	1	All sectors	None
1	1	0	1	0	All sectors	None
1	1	0	1	1	All sectors	None
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None



1.6.1.1.9. Block Protection Bits in EPCQ256 when TB Bit is Set to 0

Table 23. Block Protection Bits in EPCQ256 when TB Bit is Set to 0

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	0	0	None	All sectors
0	0	0	0	1	Sector 511	Sectors (0 to 510)
0	0	0	1	0	Sectors (510 to 511)	Sectors (0 to 509)
0	0	0	1	1	Sectors (508 to 511)	Sectors (0 to 507)
0	0	1	0	0	Sectors (504 to 511)	Sectors (0 to 503)
0	0	1	0	1	Sectors (496 to 511)	Sectors (0 to 495)
0	0	1	1	0	Sectors (480 to 511)	Sectors (0 to 479)
0	0	1	1	1	Sectors (448 to 511)	Sectors (0 to 447)
0	1	0	0	0	Sectors (384 to 511)	Sectors (0 to 383)
0	1	0	0	1	Sectors (256 to 511)	Sectors (0 to 255)
0	1	0	1	0	All sectors	None
0	1	0	1	1	All sectors	None
0	1	1	0	0	All sectors	None
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

1.6.1.1.10. Block Protection Bits in EPCQ256 when TB Bit is Set to 1

Table 24. Block Protection Bits in EPCQ256 when TB Bit is Set to 1

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
1	0	0	0	0	None	All sectors
1	0	0	0	1	Sector 0	Sectors (1 to 511)
1	0	0	1	0	Sectors (0 to 1)	Sectors (2 to 511)
1	0	0	1	1	Sectors (0 to 3)	Sectors (4 to 511)
1	0	1	0	0	Sectors (0 to 7)	Sectors (8 to 511)
1	0	1	0	1	Sectors (0 to 15)	Sectors (16 to 511)
1	0	1	1	0	Sectors (0 to 31)	Sectors (32 to 511)
1	0	1	1	1	Sectors (0 to 63)	Sectors (64 to 511)
1	1	0	0	0	Sectors (0 to 127)	Sectors (128 to 511)
1	1	0	0	1	Sectors (0 to 255)	Sectors (256 to 511)
1	1	0	1	0	All sectors	None
1	1	0	1	1	All sectors	None

continued...

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None

1.6.1.1.11. Block Protection Bits in EPCQ512/A when TB is Set to 0

Table 25. Block Protection Bits in EPCQ512/A when TB Bit is Set to 0

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	0	0	None	All sectors
0	0	0	0	1	Sector 1023	Sectors (0 to 1022)
0	0	0	1	0	Sectors (1022 to 1023)	Sectors (0 to 1021)
0	0	0	1	1	Sectors (1020 to 1023)	Sectors (0 to 1019)
0	0	1	0	0	Sectors (1016 to 1023)	Sectors (0 to 1015)
0	0	1	0	1	Sectors (1008 to 1023)	Sectors (0 to 1007)
0	0	1	1	0	Sectors (992 to 1023)	Sectors (0 to 991)
0	0	1	1	1	Sectors (960 to 1023)	Sectors (0 to 959)
0	1	0	0	0	Sectors (896 to 1023)	Sectors (0 to 895)
0	1	0	0	1	Sectors (768 to 1023)	Sectors (0 to 767)
0	1	0	1	0	Sectors (512 to 1023)	Sectors (0 to 511)
0	1	0	1	1	All sectors	None
0	1	1	0	0	All sectors	None
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

1.6.1.1.12. Block Protection Bits in EPCQ512/A when TB is Set to 1

Table 26. Block Protection Bits in EPCQ512/A when TB Bit is Set to 1

Status Register Content					Memory Content	
TB Bit	BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
1	0	0	0	0	None	All sectors
1	0	0	0	1	Sector 0	Sectors (1 to 1023)
1	0	0	1	0	Sectors (0 to 1)	Sectors (2 to 1023)
1	0	0	1	1	Sectors (0 to 3)	Sectors (4 to 1023)
1	0	1	0	0	Sectors (0 to 7)	Sectors (8 to 1023)

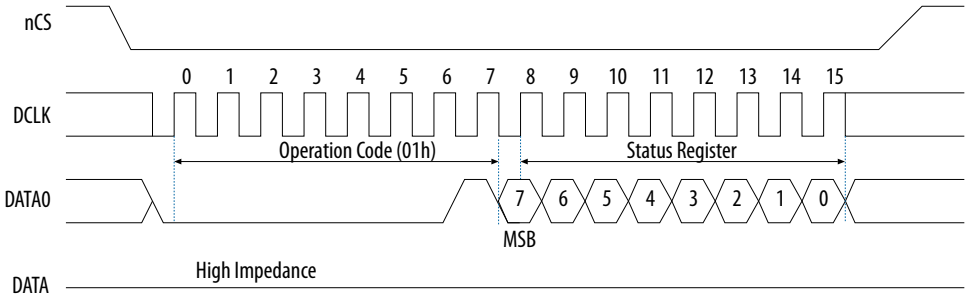
continued...

Status Register Content					Memory Content	
TB Bit	**BP3 Bit**	**BP2 Bit**	**BP1 Bit**	**BP0 Bit**	**Protected Area**	**Unprotected Area**
1	0	1	0	1	Sectors (0 to 15)	Sectors (16 to 1023)
1	0	1	1	0	Sectors (0 to 31)	Sectors (32 to 1023)
1	0	1	1	1	Sectors (0 to 63)	Sectors (64 to 1023)
1	1	0	0	0	Sectors (0 to 127)	Sectors (128 to 1023)
1	1	0	0	1	Sectors (0 to 255)	Sectors (256 to 1023)
1	1	0	1	0	Sectors (0 to 511)	Sectors (512 to 1023)
1	1	0	1	1	All sectors	None
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None

1.6.1.2. Write Status Register Operation (01h)

The write status operation does not affect the write enable latch and write in progress bits. You can use the write status operation to set the status register block protection and top or bottom bits. Therefore, you can implement this operation to protect certain memory sectors. After setting the block protect bits, the protected memory sectors are treated as read-only memory. You must execute the write enable operation before the write status operation.

Figure 2. Write Status Operation Timing Diagram



Immediately after the `nCS` signal drives high, the device initiates the self-timed write status cycle. The self-timed write status cycle usually takes 5 ms for all EPCQ devices and is guaranteed to be less than 8 ms. For details about t_{WS}, refer to the related information below. You must account for this delay to ensure that the status register is written with the desired block protect bits. Alternatively, you can check the write in progress bit in the status register by executing the read status operation while the self-timed write status cycle is in progress. Set the write in progress bit to `1` during the self-timed write status cycle and `0` when it is complete.

Related Information

Write Operation Timing on page 40
The Write Operation Parameters provides more information about t_{WS}, t_{ES} and t_{WB}.