



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MAX 7000A Programmable Logic Device

September 2003, ver. 4.5

Data Sheet

Features...

- High-performance 3.3-V EEPROM-based programmable logic devices (PLDs) built on second-generation Multiple Array MatriX (MAX[®]) architecture (see [Table 1](#))
- 3.3-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface with advanced pin-locking capability
 - MAX 7000AE device in-system programmability (ISP) circuitry compliant with IEEE Std. 1532
 - EPM7128A and EPM7256A device ISP circuitry compatible with IEEE Std. 1532
- Built-in boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1
- Supports JEDEC Jam Standard Test and Programming Language (STAPL) JESD-71
- Enhanced ISP features
 - Enhanced ISP algorithm for faster programming (excluding EPM7128A and EPM7256A devices)
 - ISP_Done bit to ensure complete programming (excluding EPM7128A and EPM7256A devices)
 - Pull-up resistor on I/O pins during in-system programming
- Pin-compatible with the popular 5.0-V MAX 7000S devices
- High-density PLDs ranging from 600 to 10,000 usable gates
- Extended temperature range



For information on in-system programmable 5.0-V MAX 7000 or 2.5-V MAX 7000B devices, see the [MAX 7000 Programmable Logic Device Family Data Sheet](#) or the [MAX 7000B Programmable Logic Device Family Data Sheet](#).

Table 1. MAX 7000A Device Features

| Feature | EPM7032AE | EPM7064AE | EPM7128AE | EPM7256AE | EPM7512AE |
|-----------------------|-----------|-----------|-----------|-----------|-----------|
| Usable gates | 600 | 1,250 | 2,500 | 5,000 | 10,000 |
| Macrocells | 32 | 64 | 128 | 256 | 512 |
| Logic array blocks | 2 | 4 | 8 | 16 | 32 |
| Maximum user I/O pins | 36 | 68 | 100 | 164 | 212 |
| t_{PD} (ns) | 4.5 | 4.5 | 5.0 | 5.5 | 7.5 |
| t_{SU} (ns) | 2.9 | 2.8 | 3.3 | 3.9 | 5.6 |
| t_{FSU} (ns) | 2.5 | 2.5 | 2.5 | 2.5 | 3.0 |
| t_{CO1} (ns) | 3.0 | 3.1 | 3.4 | 3.5 | 4.7 |
| f_{CNT} (MHz) | 227.3 | 222.2 | 192.3 | 172.4 | 116.3 |

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, ByteBlasterMV™ parallel port download cable, and BitBlaster™ serial download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File- (.svf) capable in-circuit tester

General Description

MAX 7000A (including MAX 7000AE) devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 7000A devices in the -4, -5, -6, -7, and some -10 speed grades are compatible with the timing requirements for 33 MHz operation of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 2](#).

Table 2. MAX 7000A Speed Grades

| Device | Speed Grade | | | | | |
|-----------|-------------|----|----|----|-----|-----|
| | -4 | -5 | -6 | -7 | -10 | -12 |
| EPM7032AE | ✓ | | | ✓ | ✓ | |
| EPM7064AE | ✓ | | | ✓ | ✓ | |
| EPM7128A | | | ✓ | ✓ | ✓ | ✓ |
| EPM7128AE | | ✓ | | ✓ | ✓ | |
| EPM7256A | | | ✓ | ✓ | ✓ | ✓ |
| EPM7256AE | | ✓ | | ✓ | ✓ | |
| EPM7512AE | | | | ✓ | ✓ | ✓ |

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See [Table 3](#) and [Table 4](#).

Table 3. MAX 7000A Maximum User I/O Pins *Note (1)*

| Device | 44-Pin PLCC | 44-Pin TQFP | 49-Pin Ultra FineLine BGA (2) | 84-Pin PLCC | 100-Pin TQFP | 100-Pin FineLine BGA (3) |
|-----------|-------------|-------------|-------------------------------|-------------|--------------|--------------------------|
| EPM7032AE | 36 | 36 | | | | |
| EPM7064AE | 36 | 36 | 41 | | 68 | 68 |
| EPM7128A | | | | 68 | 84 | 84 |
| EPM7128AE | | | | 68 | 84 | 84 |
| EPM7256A | | | | | 84 | |
| EPM7256AE | | | | | 84 | 84 |
| EPM7512AE | | | | | | |

Table 4. MAX 7000A Maximum User I/O Pins *Note (1)*

| Device | 144-Pin TQFP | 169-Pin Ultra FineLine BGA (2) | 208-Pin PQFP | 256-Pin BGA | 256-Pin FineLine BGA (3) |
|-----------|--------------|--------------------------------|--------------|-------------|--------------------------|
| EPM7032AE | | | | | |
| EPM7064AE | | | | | |
| EPM7128A | 100 | | | | 100 |
| EPM7128AE | 100 | 100 | | | 100 |
| EPM7256A | 120 | | 164 | | 164 |
| EPM7256AE | 120 | | 164 | | 164 |
| EPM7512AE | 120 | | 176 | 212 | 212 |

Notes to tables:

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs”](#) on [page 15](#) for more details.
- (3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs”](#) on [page 15](#) for more details.

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0 and 3.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the [MAX+PLUS II Programmable Logic Development System & Software Data Sheet](#) and the [Quartus Programmable Logic Development System & Software Data Sheet](#).

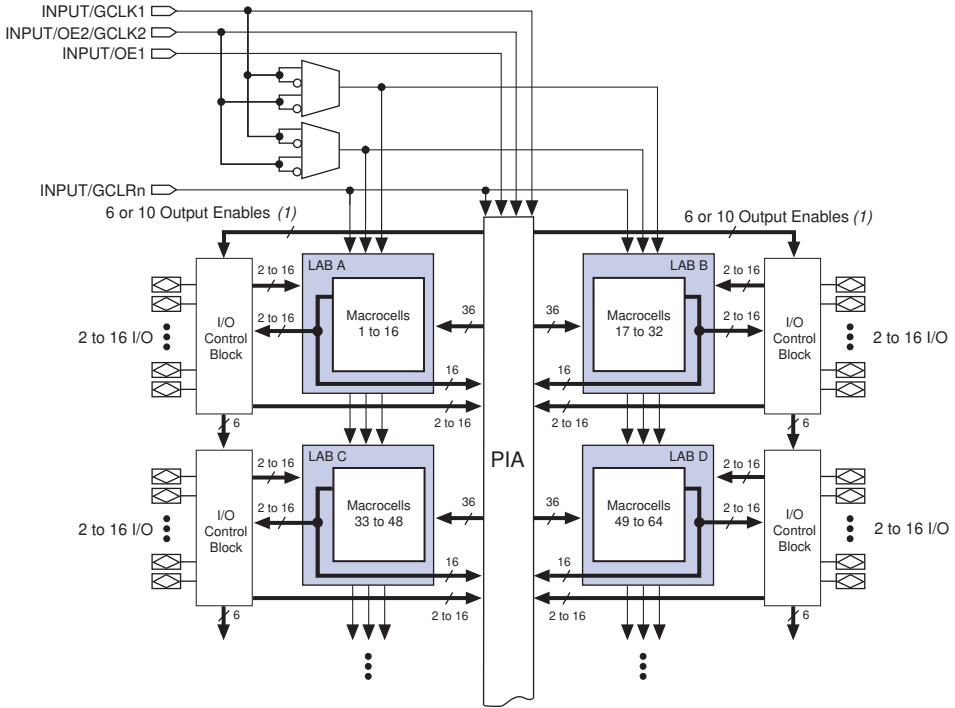
Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000A devices.

Figure 1. MAX 7000A Device Block Diagram



Note:

- (1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

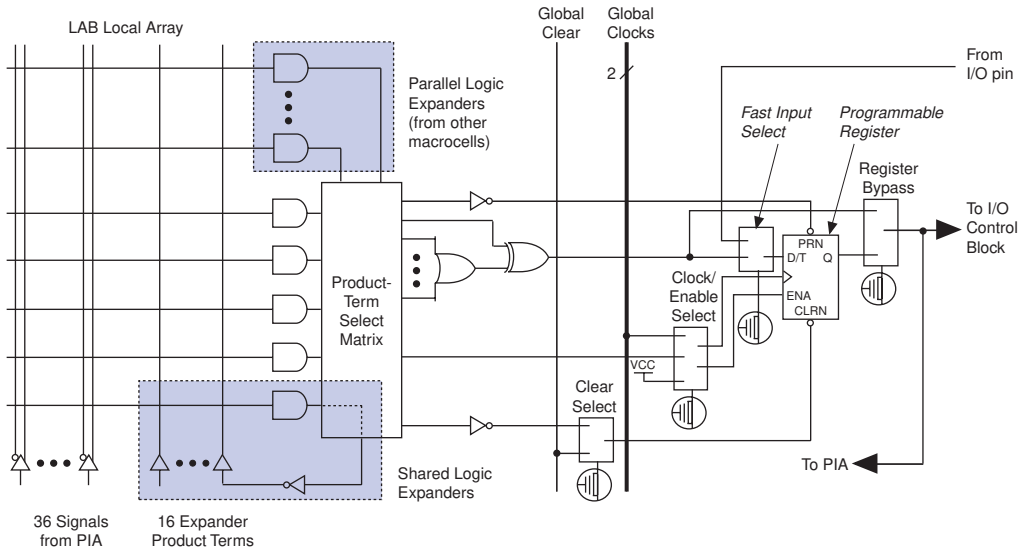
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.

Figure 2. MAX 7000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in [Figure 1](#), these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in [Figure 2](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

Expander Product Terms

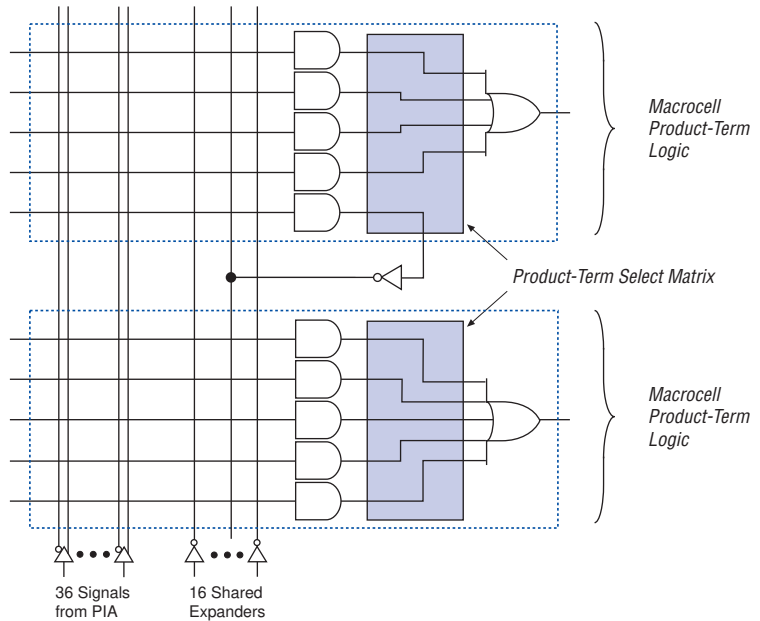
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. **Figure 3** shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

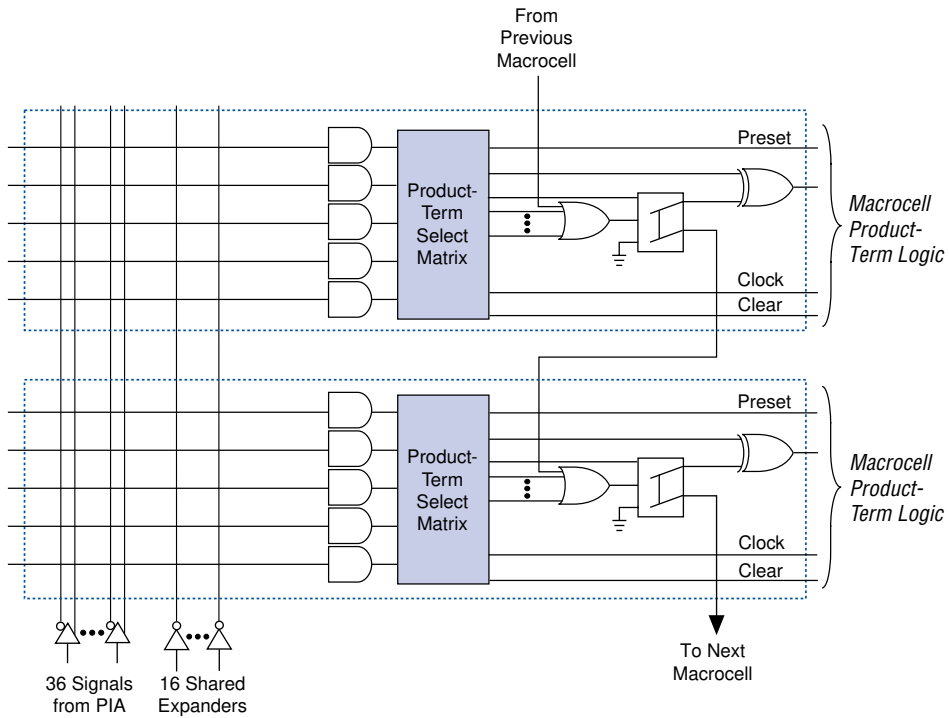
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

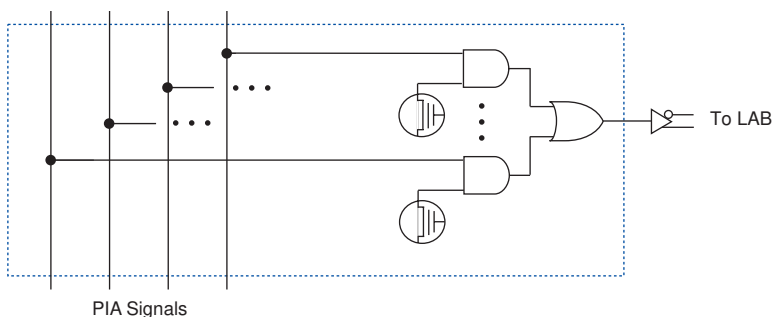
Figure 4. MAX 7000A Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

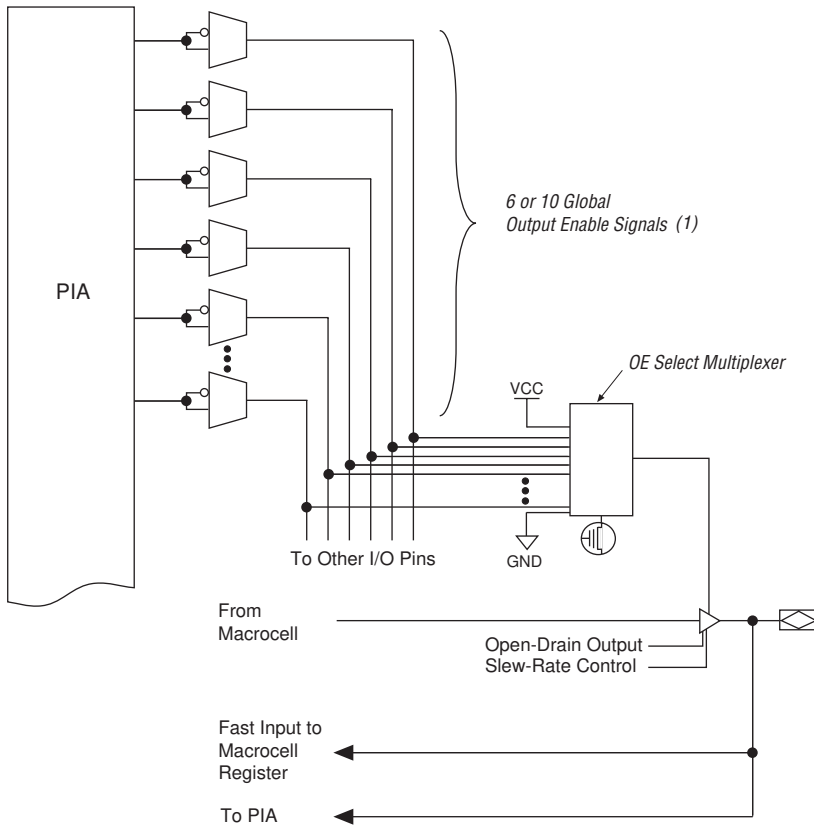
Figure 5. MAX 7000A PIA Routing

While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000A Devices



Note:

- (1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enable signals. EPM7512AE devices have 10 output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

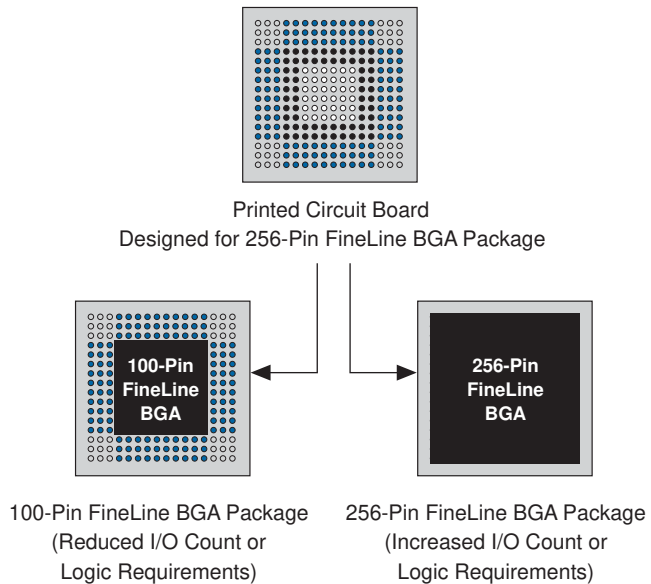
The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 7](#)).

Figure 7. SameFrame Pin-Out Example



In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The programming times described in Tables 5 through 7 are associated with the worst-case method using the enhanced ISP algorithm.

Table 5. MAX 7000A t_{PULSE} & $Cycle_{TCK}$ Values

| Device | Programming | | Stand-Alone Verification | |
|--------------|------------------|----------------|--------------------------|----------------|
| | t_{PPULSE} (s) | $Cycle_{PTCK}$ | t_{VPULSE} (s) | $Cycle_{VTCK}$ |
| EPM7032AE | 2.00 | 55,000 | 0.002 | 18,000 |
| EPM7064AE | 2.00 | 105,000 | 0.002 | 35,000 |
| EPM7128AE | 2.00 | 205,000 | 0.002 | 68,000 |
| EPM7256AE | 2.00 | 447,000 | 0.002 | 149,000 |
| EPM7512AE | 2.00 | 890,000 | 0.002 | 297,000 |
| EPM7128A (1) | 5.11 | 832,000 | 0.03 | 528,000 |
| EPM7256A (1) | 6.43 | 1,603,000 | 0.03 | 1,024,000 |

Tables 6 and 7 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 6. MAX 7000A In-System Programming Times for Different Test Clock Frequencies

| Device | f_{TCK} | | | | | | | | Units |
|--------------|-----------|-------|-------|-------|---------|---------|---------|--------|-------|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM7032AE | 2.01 | 2.01 | 2.03 | 2.06 | 2.11 | 2.28 | 2.55 | 3.10 | s |
| EPM7064AE | 2.01 | 2.02 | 2.05 | 2.11 | 2.21 | 2.53 | 3.05 | 4.10 | s |
| EPM7128AE | 2.02 | 2.04 | 2.10 | 2.21 | 2.41 | 3.03 | 4.05 | 6.10 | s |
| EPM7256AE | 2.05 | 2.09 | 2.23 | 2.45 | 2.90 | 4.24 | 6.47 | 10.94 | s |
| EPM7512AE | 2.09 | 2.18 | 2.45 | 2.89 | 3.78 | 6.45 | 10.90 | 19.80 | s |
| EPM7128A (1) | 5.19 | 5.27 | 5.52 | 5.94 | 6.77 | 9.27 | 13.43 | 21.75 | s |
| EPM7256A (1) | 6.59 | 6.75 | 7.23 | 8.03 | 9.64 | 14.45 | 22.46 | 38.49 | s |

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies

| Device | f_{TCK} | | | | | | | | Units |
|--------------|-----------|-------|-------|-------|---------|---------|---------|--------|-------|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM7032AE | 0.00 | 0.01 | 0.01 | 0.02 | 0.04 | 0.09 | 0.18 | 0.36 | s |
| EPM7064AE | 0.01 | 0.01 | 0.02 | 0.04 | 0.07 | 0.18 | 0.35 | 0.70 | s |
| EPM7128AE | 0.01 | 0.02 | 0.04 | 0.07 | 0.14 | 0.34 | 0.68 | 1.36 | s |
| EPM7256AE | 0.02 | 0.03 | 0.08 | 0.15 | 0.30 | 0.75 | 1.49 | 2.98 | s |
| EPM7512AE | 0.03 | 0.06 | 0.15 | 0.30 | 0.60 | 1.49 | 2.97 | 5.94 | s |
| EPM7128A (1) | 0.08 | 0.14 | 0.29 | 0.56 | 1.09 | 2.67 | 5.31 | 10.59 | s |
| EPM7256A (1) | 0.13 | 0.24 | 0.54 | 1.06 | 2.08 | 5.15 | 10.27 | 20.51 | s |

Note to tables:

- (1) EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware



MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.

For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.



For more information, see [Programming Hardware Manufacturers](#).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. [Table 8](#) describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (<http://www.altera.com>), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 8. MAX 7000A JTAG Instructions

| JTAG Instruction | Description |
|------------------|--|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins |
| BYPASS | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation |
| IDCODE | Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO |
| USERCODE | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. The USERCODE instruction is available for MAX 7000AE devices only |
| UESCODE | These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only. |
| ISP Instructions | These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment. |

The instruction register length of MAX 7000A devices is 10 bits. The user electronic signature (UES) register length in MAX 7000A devices is 16 bits. The MAX 7000AE USERCODE register length is 32 bits. Tables 9 and 10 show the boundary-scan register length and device IDCODE information for MAX 7000A devices.

Table 9. MAX 7000A Boundary-Scan Register Length

| Device | Boundary-Scan Register Length |
|-----------|-------------------------------|
| EPM7032AE | 96 |
| EPM7064AE | 192 |
| EPM7128A | 288 |
| EPM7128AE | 288 |
| EPM7256A | 480 |
| EPM7256AE | 480 |
| EPM7512AE | 624 |

Table 10. 32-Bit MAX 7000A Device IDCODE *Note (1)*

| Device | IDCODE (32 Bits) | | | |
|-----------|------------------|-----------------------|-----------------------------------|---------------|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | 1 (1 Bit) (2) |
| EPM7032AE | 0001 | 0111 0000 0011 0010 | 00001101110 | 1 |
| EPM7064AE | 0001 | 0111 0000 0110 0100 | 00001101110 | 1 |
| EPM7128A | 0000 | 0111 0001 0010 1000 | 00001101110 | 1 |
| EPM7128AE | 0001 | 0111 0001 0010 1000 | 00001101110 | 1 |
| EPM7256A | 0000 | 0111 0010 0101 0110 | 00001101110 | 1 |
| EPM7256AE | 0001 | 0111 0010 0101 0110 | 00001101110 | 1 |
| EPM7512AE | 0001 | 0111 0101 0001 0010 | 00001101110 | 1 |

Notes:

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 8 shows timing information for the JTAG signals.

Figure 8. MAX 7000A JTAG Waveforms

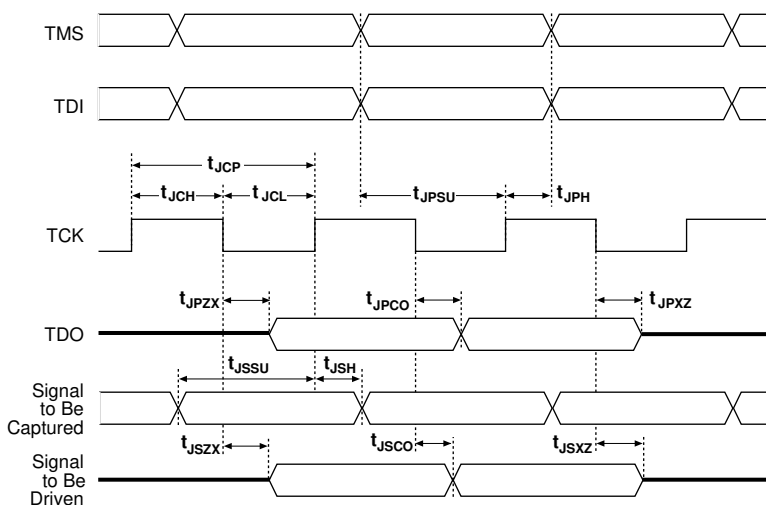


Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices *Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|------------|--|-----|-----|------|
| t_{JCP} | TCK clock period | 100 | | ns |
| t_{JCH} | TCK clock high time | 50 | | ns |
| t_{JCL} | TCK clock low time | 50 | | ns |
| t_{JPSU} | JTAG port setup time | 20 | | ns |
| t_{JPH} | JTAG port hold time | 45 | | ns |
| t_{JPCO} | JTAG port clock to output | | 25 | ns |
| t_{JPZX} | JTAG port high impedance to valid output | | 25 | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | | 25 | ns |
| t_{JSSU} | Capture register setup time | 20 | | ns |
| t_{JSH} | Capture register hold time | 45 | | ns |
| t_{JSCO} | Update register clock to output | | 25 | ns |
| t_{JSZX} | Update register high impedance to valid output | | 25 | ns |
| t_{JSXZ} | Update register valid output to high impedance | | 25 | ns |

Note:

(1) Timing parameters shown in this table apply for all specified VCCIO levels.

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1} . Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

| Table 12. MAX 7000A MultiVolt I/O Support | | | | | | |
|--|-------------------------|------------|------------|--------------------------|------------|------------|
| V_{CCIO} Voltage | Input Signal (V) | | | Output Signal (V) | | |
| | 2.5 | 3.3 | 5.0 | 2.5 | 3.3 | 5.0 |
| 2.5 | ✓ | ✓ | ✓ | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | | ✓ | ✓ |

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high V_{IH} . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS V_{OH} requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.