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The Altera Enpirion ES1021QI is an integrated 4-channel controlled-on/controlled-off power-supply sequencer with supply monitoring, fault protection and a "sequence completed" signal ($\overline{\text{RESET}}$). ES1021QI uses a patented, micropower 7x charge pump to drive four external low-cost NFET switch gates above the supply rail by 5.3V. These ICs can be biased from 5V down to 1.5V by any supply.

ES1021QI has two groups of two channels, each with its independent I/O. It is ideal for voltage sequencing into redundant capability loads. All four inputs must be satisfied before turn-on, but a single group fault is ignored by the other group.

External resistors provide flexible voltage threshold programming of monitored rail voltages. Delay and sequencing are provided by external capacitors for ramp-up and ramp-down.

Additional I/O is provided for indicating and driving the $\overline{\text{RESET}}$ state in various configurations.

For volume applications, other programmable options and features are available.

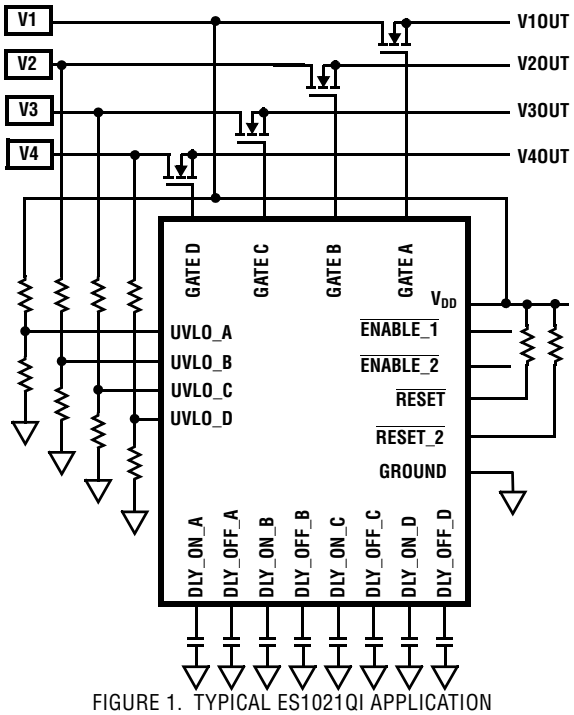


FIGURE 1. TYPICAL ES1021QI APPLICATION

Features

- Enables Arbitrary Turn-on and Turn-off Sequencing of Up to Four Power Supplies (0.7V to 5V)
- Operates From 1.5V to 5V Supply Voltage
- Supplies V_{DD} +5.3V of Charge Pumped Gate Drive
- Adjustable Voltage Slew Rate for Each Rail
- Multiple Sequencers Can be Daisy-Chained to Sequence an Infinite Number of Independent Supplies
- Glitch Immunity
- Undervoltage Lockout for Each Supply
- Active Low $\overline{\text{ENABLE}}$ Input
- Dual Channel Groupings
- QFN Package
- Pb-free (RoHS-compliant)

Applications

- Graphics Cards
- FPGA/ASIC/Microprocessor/PowerPC Supply Sequencing
- Network Routers
- Telecommunications Systems

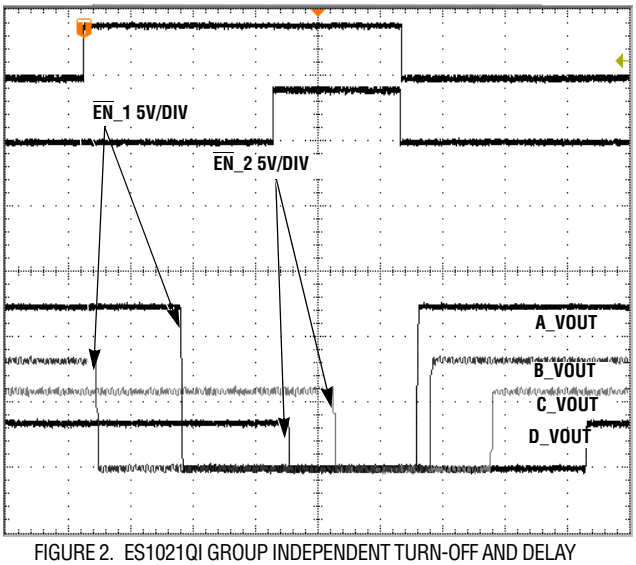


FIGURE 2. ES1021QI GROUP INDEPENDENT TURN-OFF AND DELAY ADJUSTABLE PRE-PROGRAMMED TURN-ON

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ES1021QI	S1021	-40 to +85	24 Ld 4x4 QFN	L24.4x4

NOTES:

1. Add "T" suffix for Tape and Reel. Please refer to Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html
2. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram

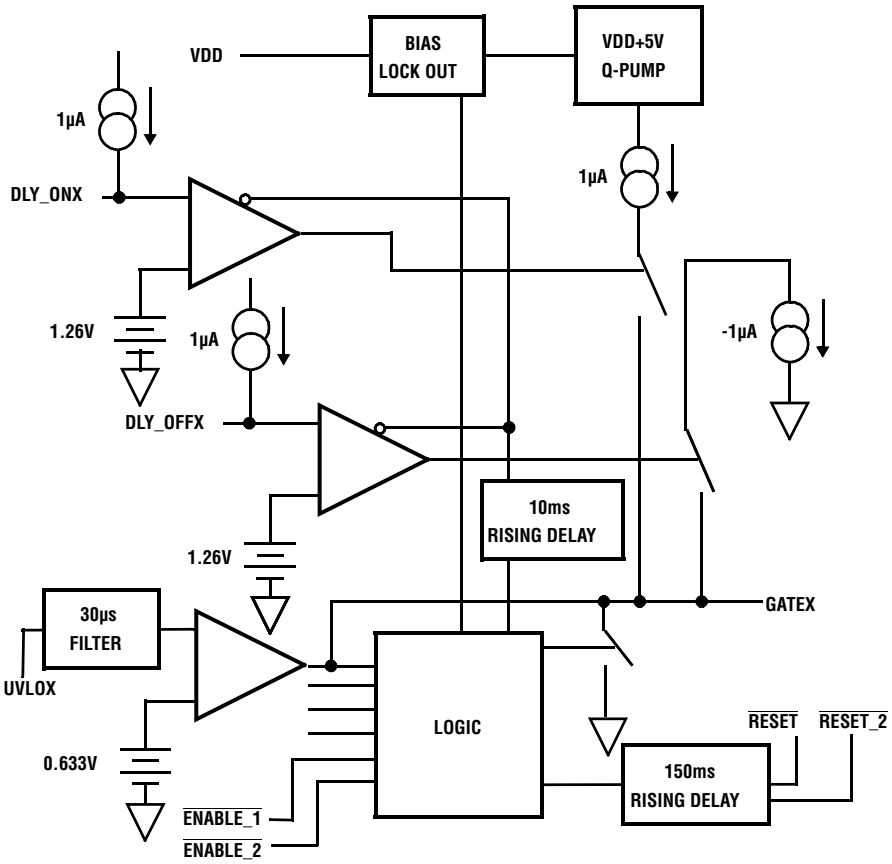
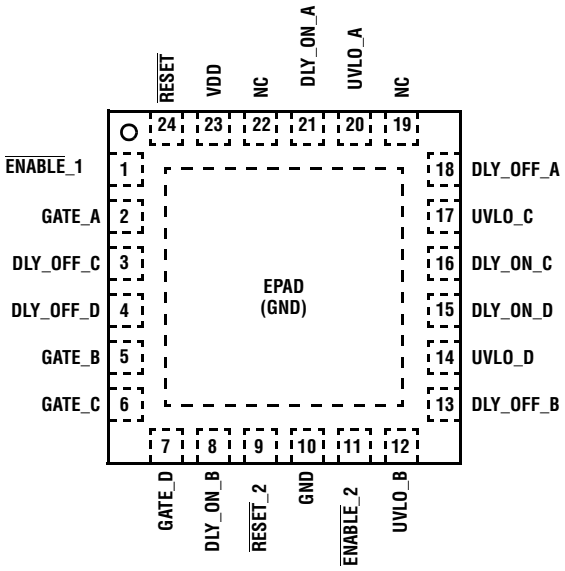


FIGURE 3. ES1021QI BLOCK DIAGRAM

Pin Configurations

ES1021QI
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	23	Chip Bias. Bias IC from nominal 1.5V to 5V.
GND	10	Bias Return. IC ground.
$\overline{\text{ENABLE}}$_1	1	Input to start on/off sequencing. Input to initiate start of programmed sequencing of supplies on or off. Enable functionality disabled for 10ms after UVLO is satisfied. ES1021QI has two $\overline{\text{ENABLE}}$ inputs; one for each 2-channel grouping. $\overline{\text{ENABLE}}$_1 is for (A, B), and $\overline{\text{ENABLE}}$_2 is for (C, D).
$\overline{\text{ENABLE}}$_2	11	
$\overline{\text{RESET}}$	24	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ provides low signal 150ms after all GATEs are fully enhanced. Delay is for stabilization of output voltages. $\overline{\text{RESET}}$ asserts low upon UVLO not being satisfied or $\overline{\text{ENABLE}}$ being deasserted. $\overline{\text{RESET}}$ outputs are open-drain, N-channel FET and are guaranteed to be in correct state for VDD down to 1V and are filtered to ignore fast transients on VDD and UVLO_X. $\overline{\text{RESET}}$_2 only exists for (C, D) group I/O.
$\overline{\text{RESET}}$_2	9	
UVLO_A	20	Undervoltage Lockout/Monitoring Input. Provides a programmable UV lockout referenced to an internal 0.633V reference. Filtered to ignore short (<30µs) transients below programmed UVLO level.
UVLO_B	12	
UVLO_C	17	
UVLO_D	14	
DLY_ON_A	21	Gate On Delay Timer Output. Allows programming of delay and sequence for VOUT turn-on using a capacitor to ground. Each capacitor charged with 1µA 10ms after turn-on initiated by ENABLE/$\overline{\text{ENABLE}}$. Internal current source provides delay to associated FET GATE turn-on.
DLY_ON_B	8	
DLY_ON_C	16	
DLY_ON_D	15	
DLY_OFF_A	18	Gate Off Delay Timer Output. Allows programming of delay and sequence for VOUT turn-off through ENABLE/$\overline{\text{ENABLE}}$ via a capacitor to ground. Each capacitor charged with 1µA internal current source to an internal reference voltage, causing corresponding gate to be pulled down, thus turning off FET.
DLY_OFF_B	13	
DLY_OFF_C	3	
DLY_OFF_D	4	
GATE_A	2	FET Gate Drive Output. Drives external FETs with 1µA current source to soft-start ramp into load.
GATE_B	5	
GATE_C	6	
GATE_D	7	
GND	EPAD	Ground. Die Substrate. Can be left floating.
NC	19, 22	No Connect

ES1021QI Feature Matrix

PART NAME	EN/$\overline{\text{EN}}$	CMOS/ TTL	GATE DRIVE OR OPEN DRAIN OUTPUTS	REQUIRED CONDITIONS FOR INITIAL START-UP	NUMBER OF UVLO INPUTS MONITORED BY EACH $\overline{\text{RESET}}$	NUMBER OF CHANNELS THAT TURN OFF WHEN ONE UVLO FAULTS	PRESET OR ADJUSTABLE SEQUENCE	NUMBER OF UVLO AND PAIRS OF I/O	FEATURES
ES1021QI	$\overline{\text{EN}}$	CMOS	Gate Drive	4 UVLO 2 EN	2 UVLO	2 Gates	Preset	2 Monitors with 2 I/O	Dual Redundant Operation

Absolute Maximum Ratings (Note 5)

V_{DD} . . . . . +6.0V
GATE . . . . . -0.3V to V_{DD}+6V
UVLO, $\overline{ENABLE}$. . . . . .-0.3V to V_{DD} + 0.3V
$\overline{RESET}$, DLY_ON, DLYOFF. . . . . .-0.3V to V_{DD} + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package (Notes 3, 4)	46	8

Maximum Junction Temperature . . . . . +125°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C

Operating Conditions

V_{DD} Supply Voltage Range . . . . . .+1.5V to +5.5V
Temperature Range (T_A) . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 1.5V to +5V, T_A = T_J = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
UVLO						
Falling Undervoltage Lockout Threshold	$V_{UVLOvth}$	T_J = +25°C	619	633	647	mV
Undervoltage Lockout Threshold Tempco	$TC_{UVLOvth}$			40		µV/°C
Undervoltage Lockout Hysteresis	$V_{UVLOhys}$			10		mV
Undervoltage Lockout Threshold Range	RUVLOvth	Max $V_{UVLOvth}$- Min $V_{UVLOvth}$		7		mV
Undervoltage Lockout Delay	TUVLOdel	$\overline{ENABLE}$ satisfied		10		ms
Transient Filter Duration	t_{FIL}	V_{DD}, UVLO, $\overline{ENABLE}$ glitch filter		30		µs
DELAY ON/OFF						
Delay Charging Current	DLY_ichg	V_{DLY} = 0V	**0.92**	1	**1.08**	µA
Delay Charging Current Range	DLY_ichg_r	DLY_ichg(max) - DLY_ichg(min)		0.08		µA
Delay Charging Current Temperature Coefficient	TC_DLY_ichg			0.2		nA/°C
Delay Threshold Voltage	DLY_Vth		**1.238**	1.266	**1.294**	V
Delay Threshold Voltage Temperature Coefficient	TC_DLY_Vth			0.2		mV/°C
$\overline{ENABLE}$, $\overline{RESET}$						
$\overline{ENABLE}$ Threshold	V_{ENh}			0.5 V_{DD}		V
$\overline{ENABLE}$ Hysteresis	V_{ENh} .V_{ENl}	Measured at V_{DD} = 1.5V		0.2		V
$\overline{ENABLE}$ Lockout Delay	t_{delEN_LO}	UVLO satisfied		10		ms
$\overline{ENABLE}$ Input Capacitance	Cin_en			5		pF
$\overline{RESET}$ Pull-up Voltage	Vpu_rst			V_{DD}		V
$\overline{RESET}$ Pull-Down Current	$I_{\overline{RST}pd1}$	V_{DD} = 1.5V, $\overline{RST}$ = 0.1V		5		mA
	$I_{\overline{RST}pd3}$	V_{DD} = 3.3V, $\overline{RST}$ = 0.1V		13		mA
	$I_{\overline{RST}pd5}$	V_{DD} = 5V, $\overline{RST}$ = 0.1V		17		mA
$\overline{RESET}$ Delay after GATE High	$T_{\overline{RST}del}$	GATE = V_{DD}+5V		160		ms

Electrical Specifications V_{DD} = 1.5V to +5V, $T_A = T_J$ = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$\overline{\text{RESET}}$ Output Low	$V_{\overline{RSTI}}$	Measured at V_{DD} = 5V with 5k pull-up resistors			**0.1**	V
RESET Output Capacitance	C_{OUT_RST}			10		pF
GATE						
GATE Turn-On Current	I_{GATEon}	GATE = 0V	**0.8**	1.1	**1.4**	µA
GATE Turn-Off Current	$I_{GATEoff\_I}$	GATE = V_{DD}, Disabled	**-1.4**	-1.05	**-0.8**	µA
GATE Current Range	I_{GATE_range}	Within IC I_{GATE} max-min			**0.35**	µA
GATE Turn-On/Off Current Temperature Coefficient	TC_I_{GATE}			0.2		nA/°C
GATE Pull-Down High Current	$I_{GATEoff\_h}$	GATE = V_{DD}, UVLO = 0V		88		mA
GATE High Voltage	V_{GATEh}	V_{DD} < 2V, T_J = +25°C		V_{DD} + 4.9V		V
	V_{GATEh}	V_{DD} > 2V	**V_{DD} + 5V**	V_{DD} + 5.3V		V
GATE Low Voltage	V_{GATEl}	Gate Low Voltage, V_{DD} = 1V		0	**0.1**	V
BIAS						
IC Supply Current	I_{VDD_5V}	V_{DD} = 5V		0.20	**0.5**	mA
	$I_{VDD\_3.3V}$	V_{DD} = 3.3V		0.14		mA
	$I_{VDD\_1.5V}$	V_{DD} = 1.5V		0.10		mA
V_{DD} Power-on Reset	V_{DD}_POR				**1**	V

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Descriptions and Operation

The ES1021QI sequencer is a 4-channel voltage sequencing controller, and is designed for use in multiple-voltage systems requiring power sequencing of various supply voltages. Individual voltage rails are gated on and off by external N-Channel MOSFETs, the gates of which are driven by an internal charge pump to V_{DD} + 5.3V (VQP) in a user-programmed sequence.

The ES1021QI is a 4-channel device that groups the four channels into two groups of two channels each. Each group of A, B and C, D, has its own $\overline{\text{ENABLE}}$ and RESET I/O pins. All four UVLO and both $\overline{\text{ENABLE}}$s must be satisfied for sequencing to start. The A, B group turns on first, 10ms after the second $\overline{\text{ENABLE}}$ is pulled low, with A then B turning on, followed by C then D.

Once the preceding GATE = VQP, the next DLY_ON pin starts to charge its capacitor; thus, all four GATEs turn on. Approximately 160ms after D GATE = VQP, the $\overline{\text{RESET}}$ output is released to go high. Once any UVLO is unsatisfied, only the related group's $\overline{\text{RESET}}$ and two GATEs are pulled low. The related EN input must be cycled for the faulted group to be turned on again.

Normal shutdown is invoked by signaling both $\overline{\text{ENABLE}}$ inputs high, which causes the two related GATEs to shut down in reverse order from turn-on. DLY_X capacitors adjust the delay between GATES during turn-on and turn-off, but not the order.

During bias up, the $\overline{\text{RESET}}$ output is guaranteed to be in the correct state, with V_{DD} lower than 1V.

ES1021QI requires that the related $\overline{\text{ENABLE}}$ be cycled for restart of its associated group GATEs. If no capacitors are connected between DLY_ON or DLY_OFF pins and ground, then all such related GATEs start to turn on immediately after the 10ms (TUVLOdel) ENABLE stabilization timeout has expired. The GATEs start to turn off immediately when ENABLE is asserted.

If some of the rails are sequenced together to reduce cost and eliminate the effect of capacitor variance on the timing, a common capacitor can be connected to two or more DLY_ON or DLY_OFF pins. In this case, multiply the capacitor value by the number of common DLY_X pins to obtain the desired timing.

Table 1 shows the nominal time delay on the DLY_X pins for various capacitor values, from the start of charging to the 1.27V reference. This table does not include the 10ms of ENABLE lockout delay during a start-up sequence, but it does represent the time from the end of the ENABLE lockout delay to the start of GATE transition. There is no ENABLE lockout delay for a sequence-off, so this table illustrates the delay to GATE transition from a disable signal.

TABLE 1. NOMINAL DELAY TO SEQUENCING THRESHOLD

DLY PIN CAPACITANCE	TIME(s)
Open	0.00006
100pF	0.00013
1000pF	0.0013
0.01µF	0.013
0.1µF	0.13
1µF	1.3
10µF	13

NOTE: Nom. T_{DEL_SEQ} = Capacitor (µF)*1.3MW.

Typical Performance Curves

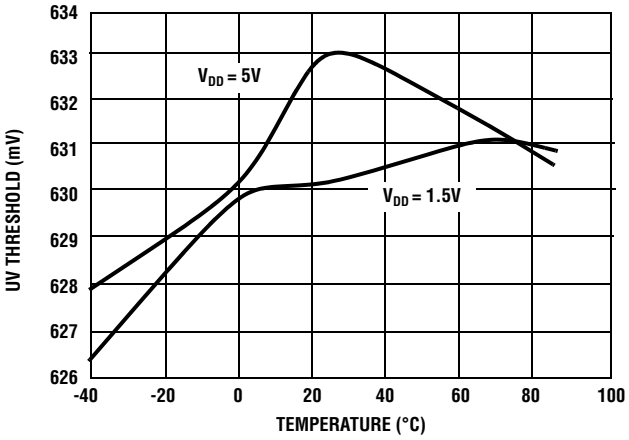


FIGURE 4. UVLO THRESHOLD VOLTAGE

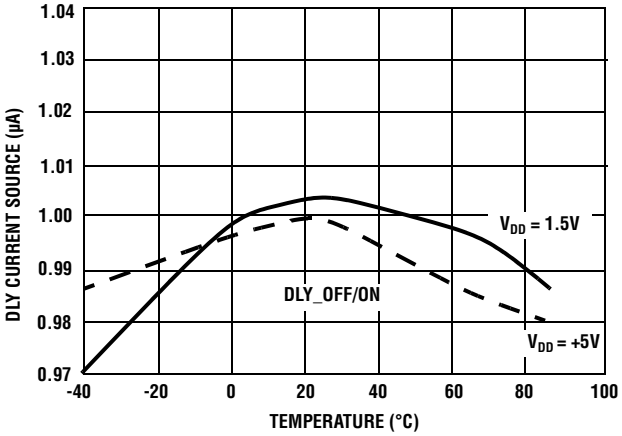


FIGURE 5. DLY CHARGE CURRENT

Figure 6 demonstrates the independence of the ES1021QI, the redundant 2-rail sequencer. It shows that either one of the two groups can be turned off, and the ABCD order of restart with capacitor programmable delay, once both EN inputs are pulled low.

Typical Performance Waveforms

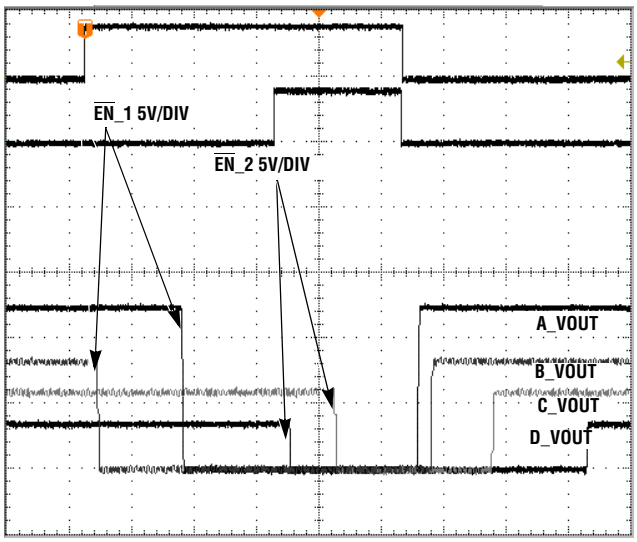


FIGURE 6. ES1021QI GROUP INDEPENDENT TURN-OFF AND DELAY ADJUSTABLE PRE-PROGRAMMED TURN-ON

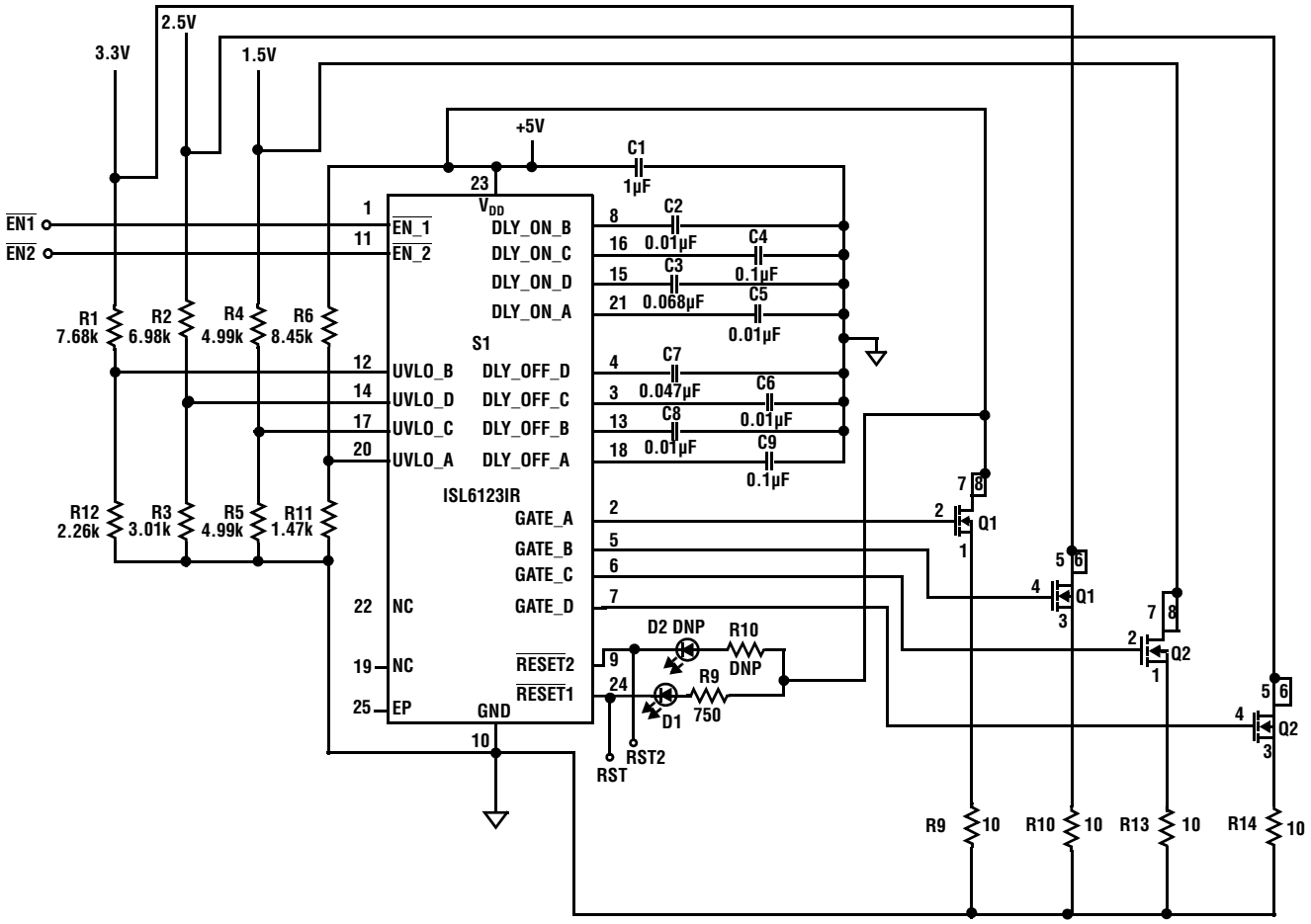


FIGURE 7. ES1021QI SCHEMATIC

Application Considerations

Timing Error Sources

In any system there are variance contributors. For ES1021QI, timing errors are mainly contributed by three sources.

Capacitor Timing Mismatch Error

Obviously, the absolute capacitor value is an error source; thus, lower-percentage tolerance capacitors help to reduce this error source. Figure 8 illustrates a difference of 0.57ms between two DLY_X outputs ramping to DLY_X threshold voltage. These 5% capacitors were from a common source. In applications where two or more GATEs or LOGIC outputs must have concurrent transitions, it is recommended that a common GATE drive be used to eliminate this timing error.

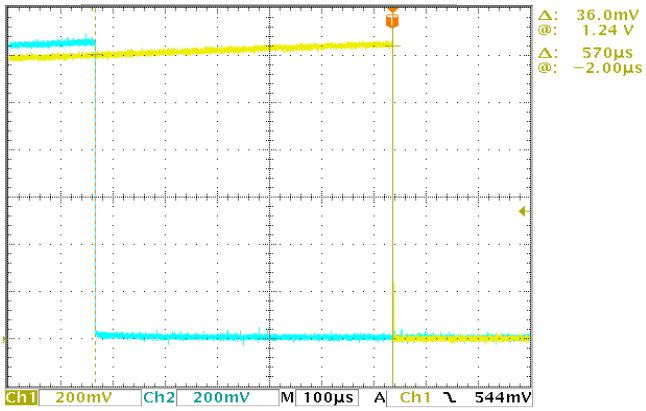


FIGURE 8. CAPACITOR TIMING MISMATCH

DLY_X Threshold Voltage and Charging Current Mismatch

The two other error sources come from the IC itself and are found across the four DLY_X outputs. These errors are the DLY_X threshold voltage (DLY_Vth) variance when the GATE_X charging and discharging current latches are set, and the DLY_X charging current (DLY_ichg) variances to determine the time to next sequencing event. Both of these parameters are bounded by specification. Figure 9 shows that, with a common capacitor, the typical error contributed by these factors is insignificant, since both DLY_X traces overlay each other.

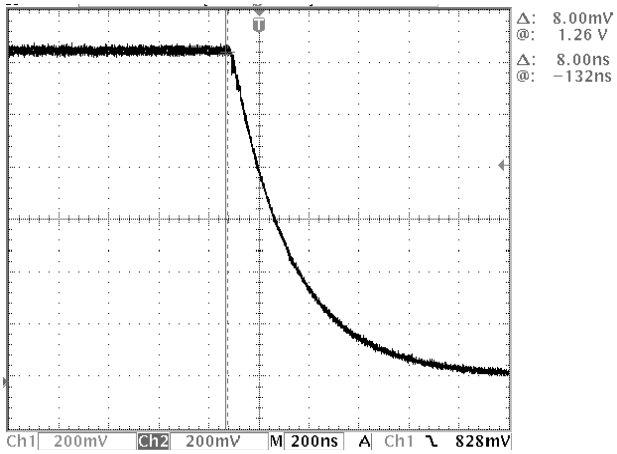


FIGURE 9. DLY_VTH AND DLY_ICHG TIMING MISMATCH

Revision History

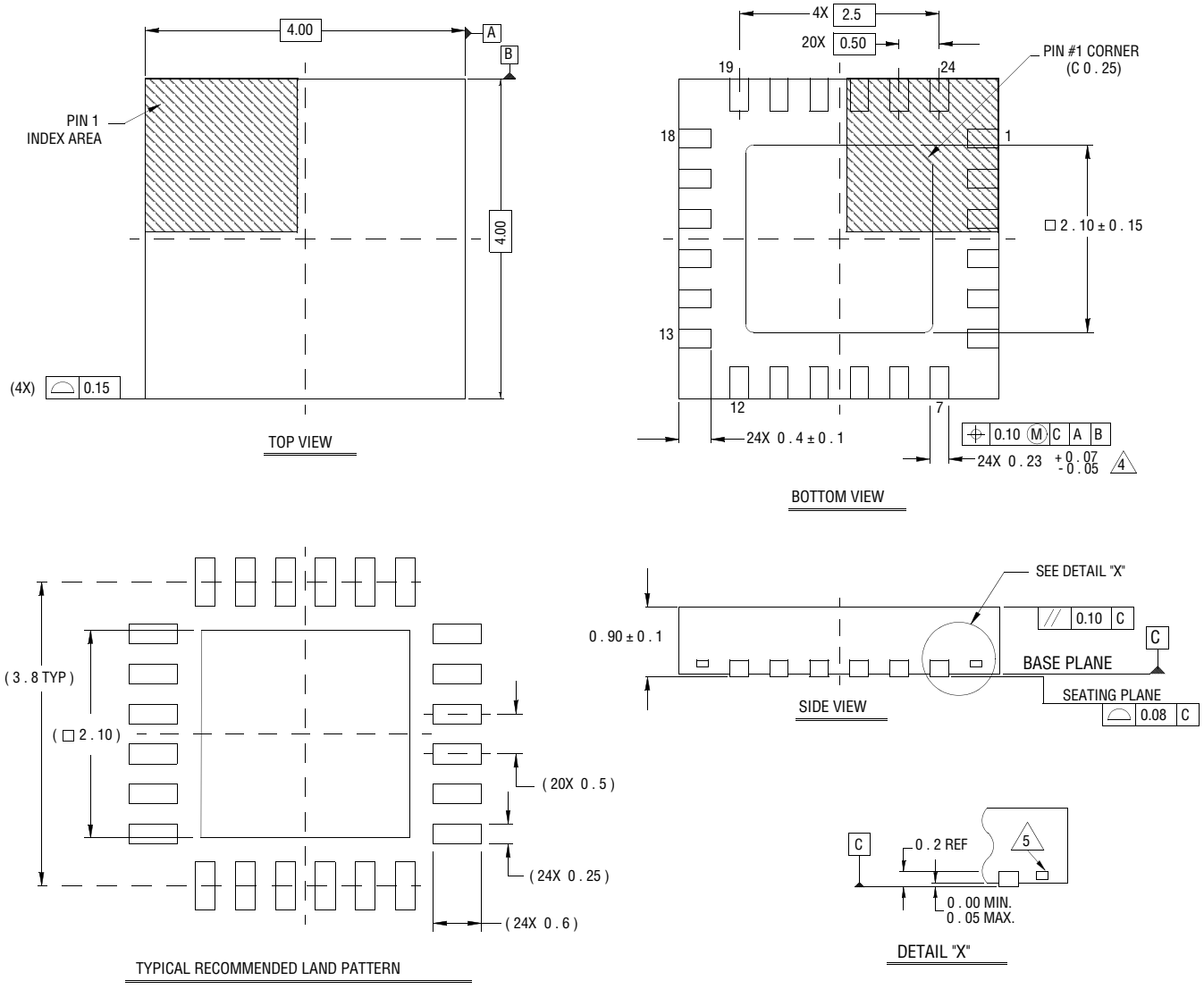
The table lists the revision history for this document.

DATE	REVISION	CHANGE
July, 2014	1.0	Initial Release.

Package Outline Drawing

L24.4x4

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.