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# TVS Diodes

Transient Voltage Suppressor Diodes

## ESD102-U2-099EL

2-Line Ultra-low Capacitance ESD / Transient Protection Diodes

ESD102-U2-099EL

## Data Sheet

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Final

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**Revision History: Revision 1.0, 2013-03-21**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.1, 2013-05-15</b>	

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Last Trademarks Update 2010-06-09

# 1 2-Line Ultra-low Capacitance ESD / Transient Protection Diodes

## 1.1 Features

- ESD / transient protection of high speed data lines exceeding:
  - IEC61000-4-2 (ESD):  $\pm 20$  kV (air / contact)
  - IEC61000-4-4 (EFT):  $\pm 2.5$  kV / 50 A (5/50ns)
  - IEC61000-4-5 (Surge):  $\pm 3$  A (8/20 $\mu$ s)
- Maximum working voltage:  $V_{RWM} = 3.3$  V
- Ultra low capacitance  $C_L = 0.4$  pF (typ.) I/O to GND,  $0.2$  pF (typ.) I/O to I/O
- Very low clamping voltage:  $V_{CL} = 8$  V (typ.) at  $I_{PP} = 16$  A
- Very low dynamic resistance:  $R_{DYN} = 0.19$   $\Omega$  (typ.)
- TSLP-4-10 package with pad pitch 0.4 mm, smallest 2 line package
- Pb-free and halogen free package (RoHS compliant)



## 1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, etc.

## 1.3 Product Description

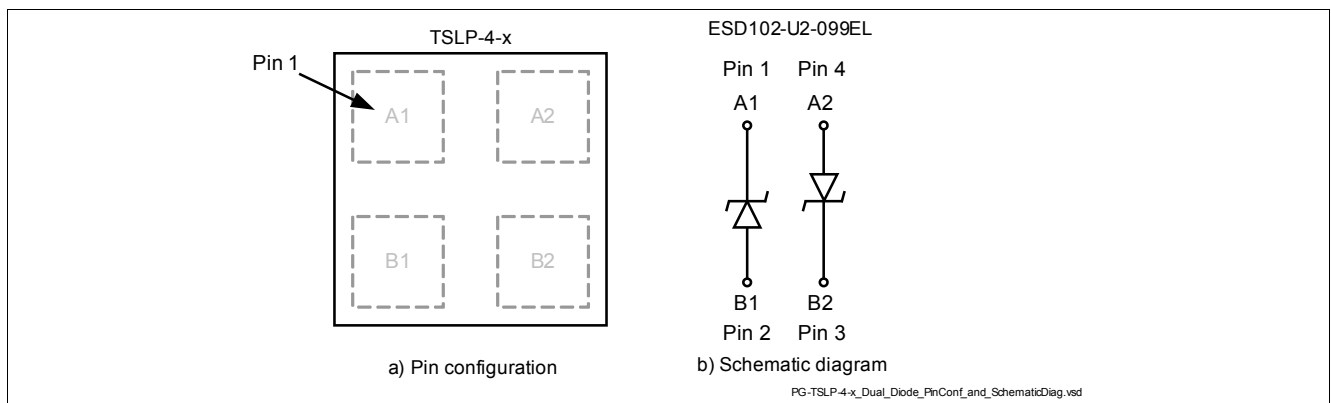


Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD102-U2-099EL	TSLP-4-10	2 Lines anti-parallel, uni-directional	B

## 2 Characteristics

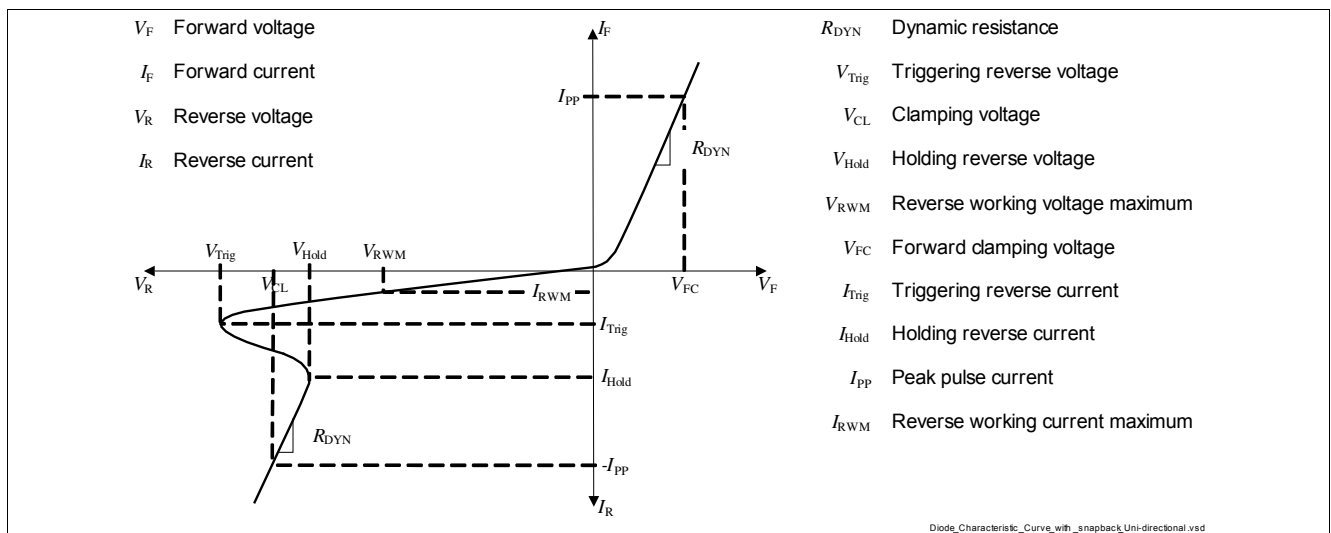
**Table 2 Maximum Rating at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD air / contact discharge <sup>1)</sup>	$V_{ESD}$	-20	–	20	kV
Peak pulse current ( $t_p = 8/20\ \mu\text{s}$ ) <sup>2)</sup>	$I_{PP}$	-3	–	3	A
Operating temperature	$T_{OP}$	-40	–	125	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65	–	150	$^\circ\text{C}$

1)  $V_{ESD}$  according to IEC61000-4-2

2)  $I_{PP}$  according to IEC61000-4-5

### 2.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified



**Figure 2 Definitions of electrical characteristics[1]**

**Table 3 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	–	–	3.3	V	I/O to GND
Reverse current	$I_R$	–	1	50	nA	$V_R = 3.3\text{ V}$ , I/O to GND

## Characteristics

**Table 4 RF Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance <sup>1)</sup>	$C_L$	–	0.4	0.65	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to GND
		–	0.2	0.35	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to I/O
Channel capacitance matching between I/O to GND	$\Delta C_{i/o-GND}$	–	0.01	–	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to GND
Channel capacitance matching between I/O to I/O	$\Delta C_{i/o-i/o}$	–	0.005	–	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to I/O

1) Total capacitance line to ground

**Table 5 ESD Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>1)</sup> [2]	$V_{CL}$	–	8	–	V	$I_{TLP} = 16\text{ A}$ , from I/O to GND
		–	11	–	V	$I_{TLP} = 30\text{ A}$ , from I/O to GND
Forward clamping voltage <sup>1)</sup> [2]	$V_{FC}$	–	6	–	V	$I_{TLP} = 16\text{ A}$ , from GND to I/O
		–	9	–	V	$I_{TLP} = 30\text{ A}$ , from GND to I/O
Dynamic resistance <sup>1)</sup> [2]	$R_{DYN}$	–	0.19	–	$\Omega$	I/O to GND
		–	0.23	–	$\Omega$	GND to I/O

 1) Please refer to Application Note AN210. TLP parameter:  $Z_0 = 50\text{ }\Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{TLP1} = 10\text{ A}$  and  $I_{TLP2} = 40\text{ A}$ .

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

### 3 Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

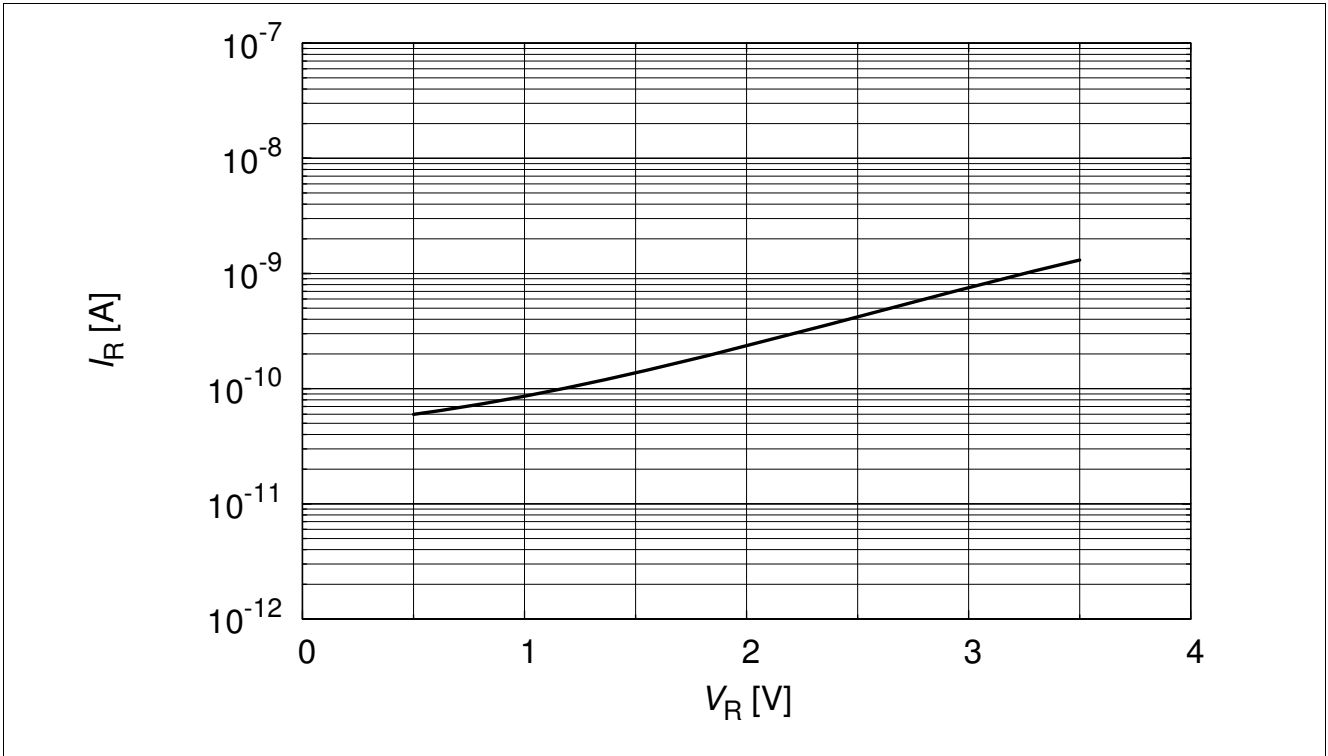


Figure 3 Reverse current,  $I_R = (V_R)$

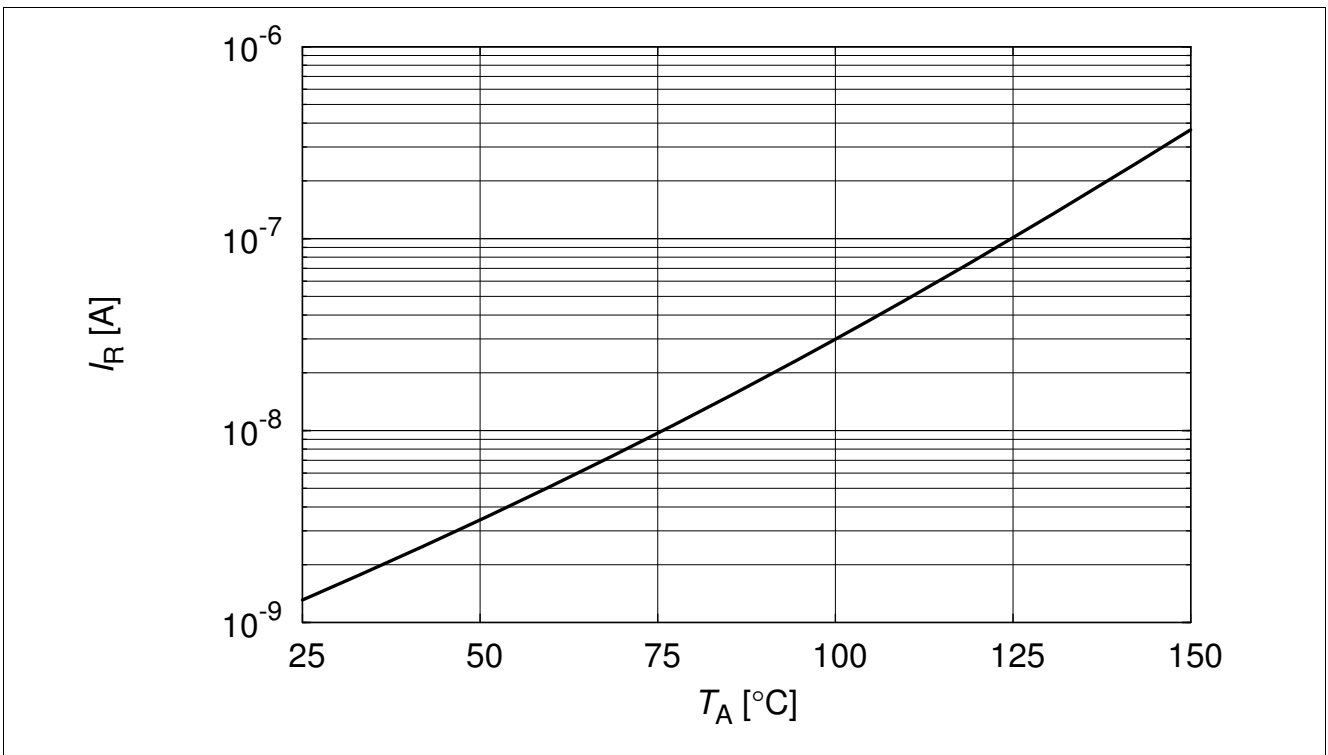


Figure 4 Reverse current:  $I_R = f(T_A)$ ,  $V_R = 3.3\text{ V}$



Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

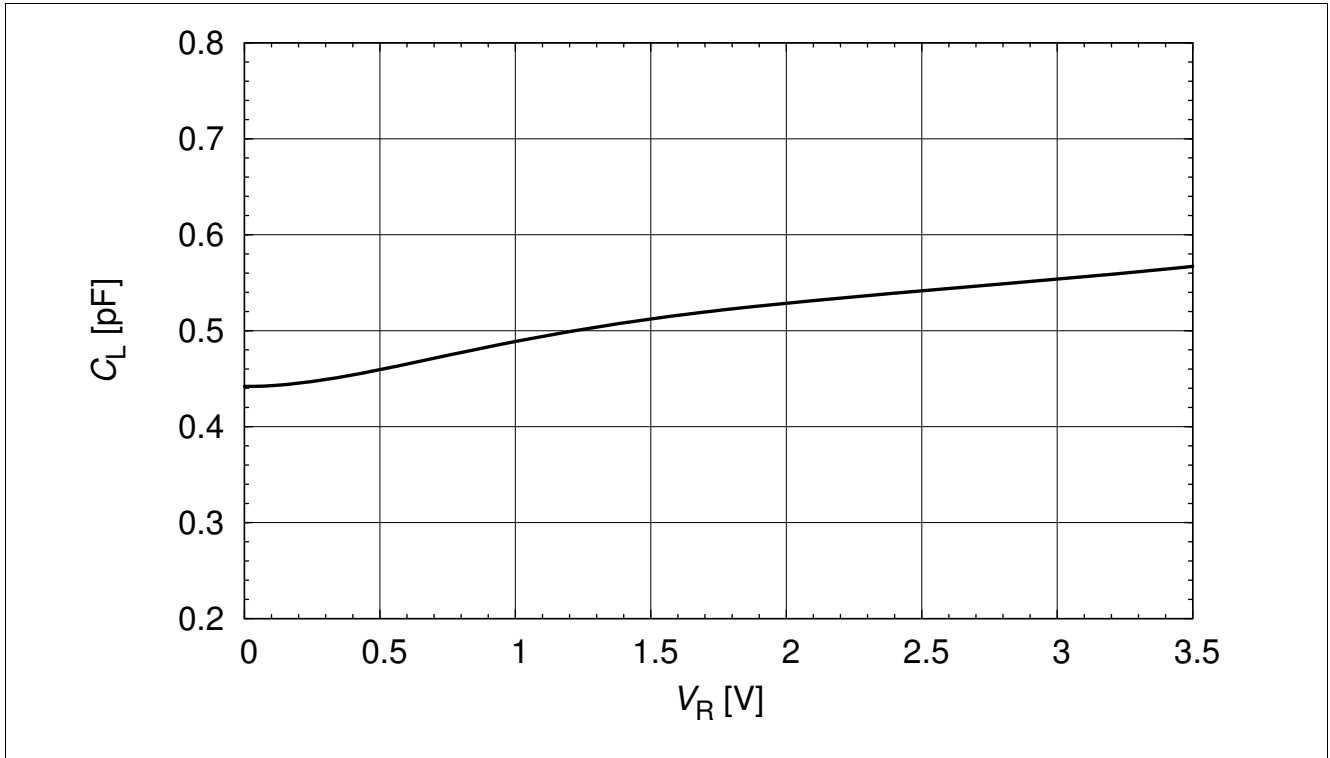
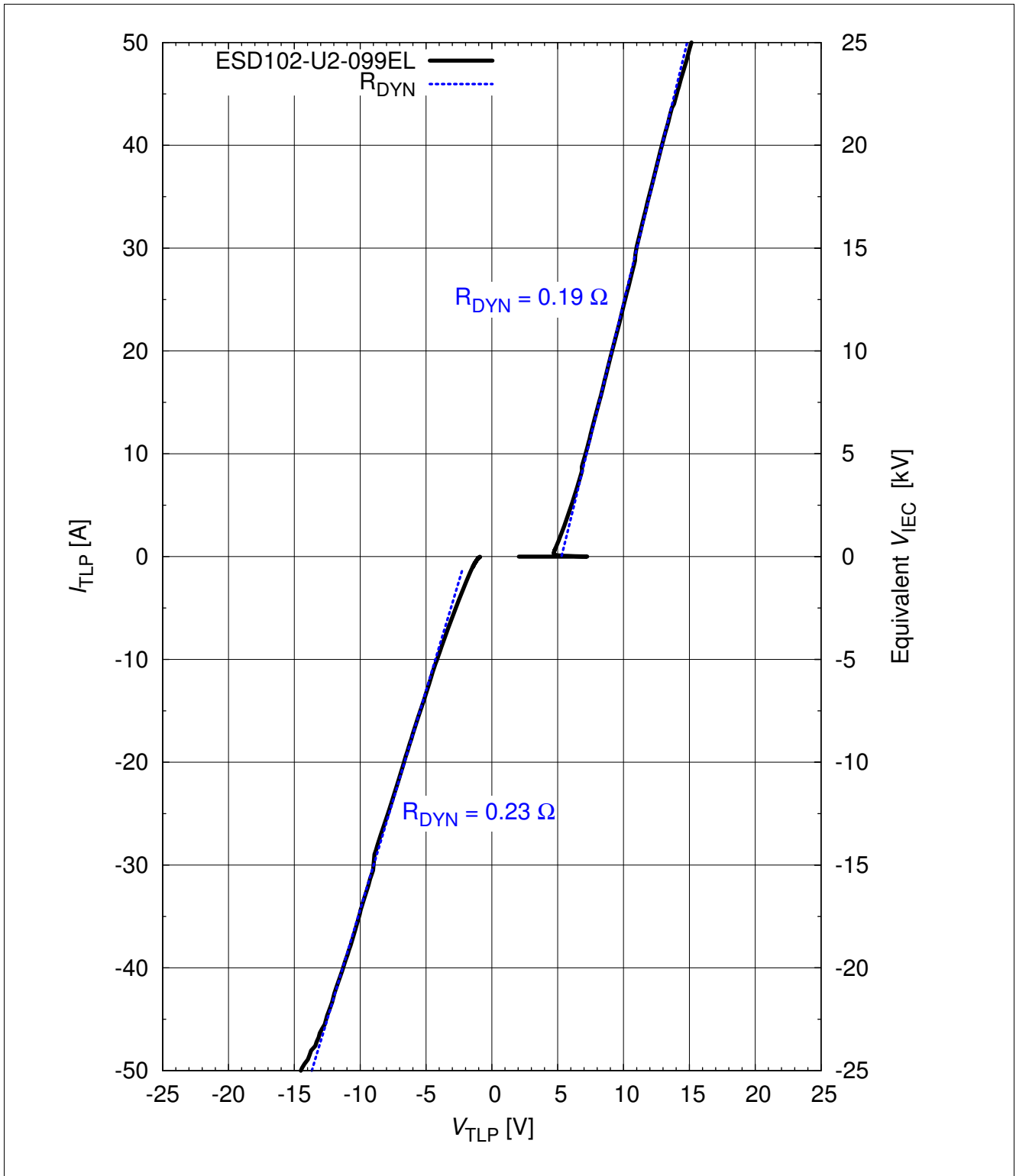


Figure 5 Line capacitance:  $C_L = f(V_R)$ ,  $f = 1\text{MHz}$ , from I/O to GND

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified



**Figure 6 Clamping voltage  $V_{TLP} = f(I_{TLP})$ [2]**

Note: TLP parameter:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{TLP1} = 10\text{ A}$  and  $I_{TLP2} = 40\text{ A}$ . The equivalent stress level  $V_{IEC}$  according IEC 61000-4-2 ( $R = 330\ \Omega$ ,  $C = 150\text{ pF}$ ) is calculated at the broad peak of the IEC waveform at  $t = 30\text{ ns}$  with  $2\text{ A/kV}$

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

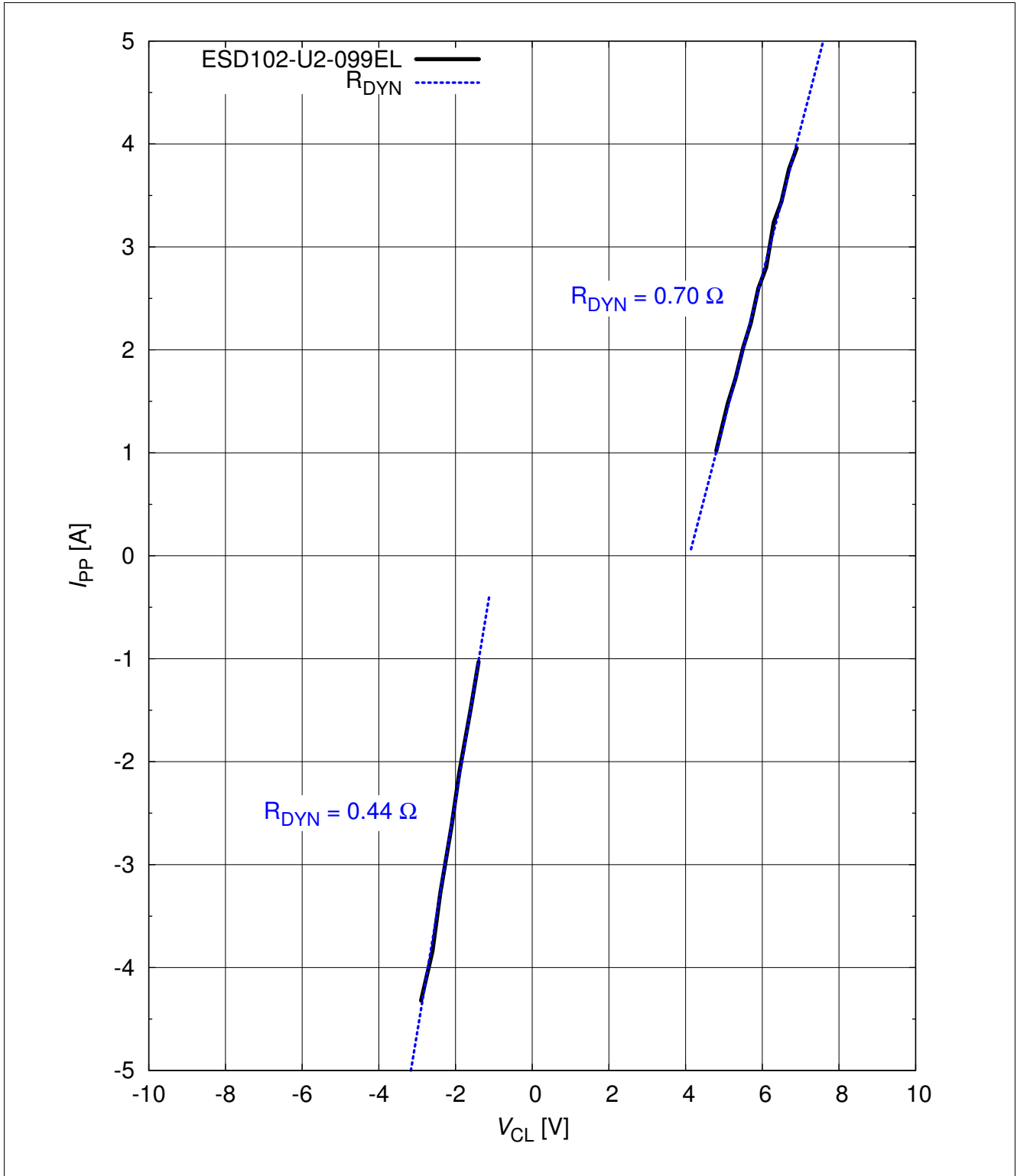


Figure 7 Pulse current (IEC61000-4-5) versus clamping voltage:  $I_{PP} = f(V_{CL})$

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

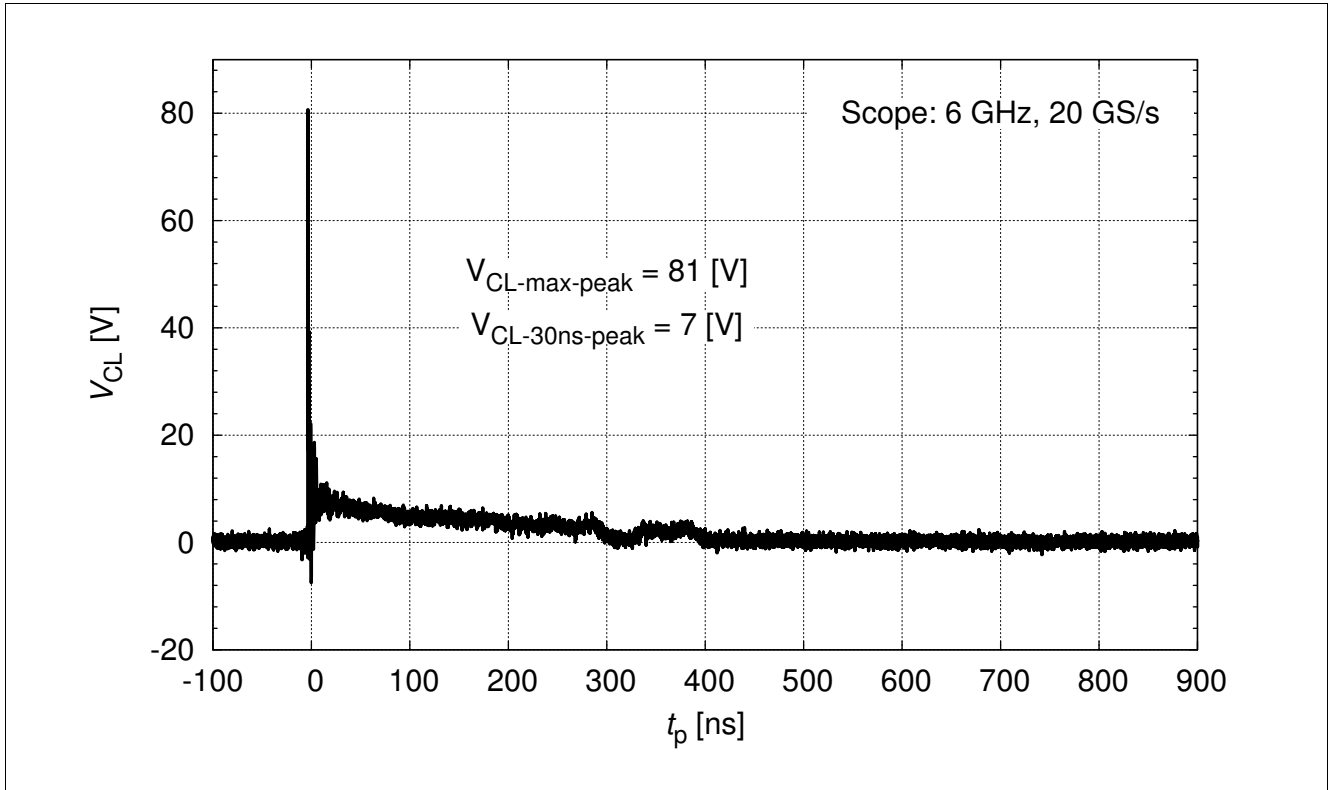


Figure 8 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV positive pulse from pin 1 to pin 2

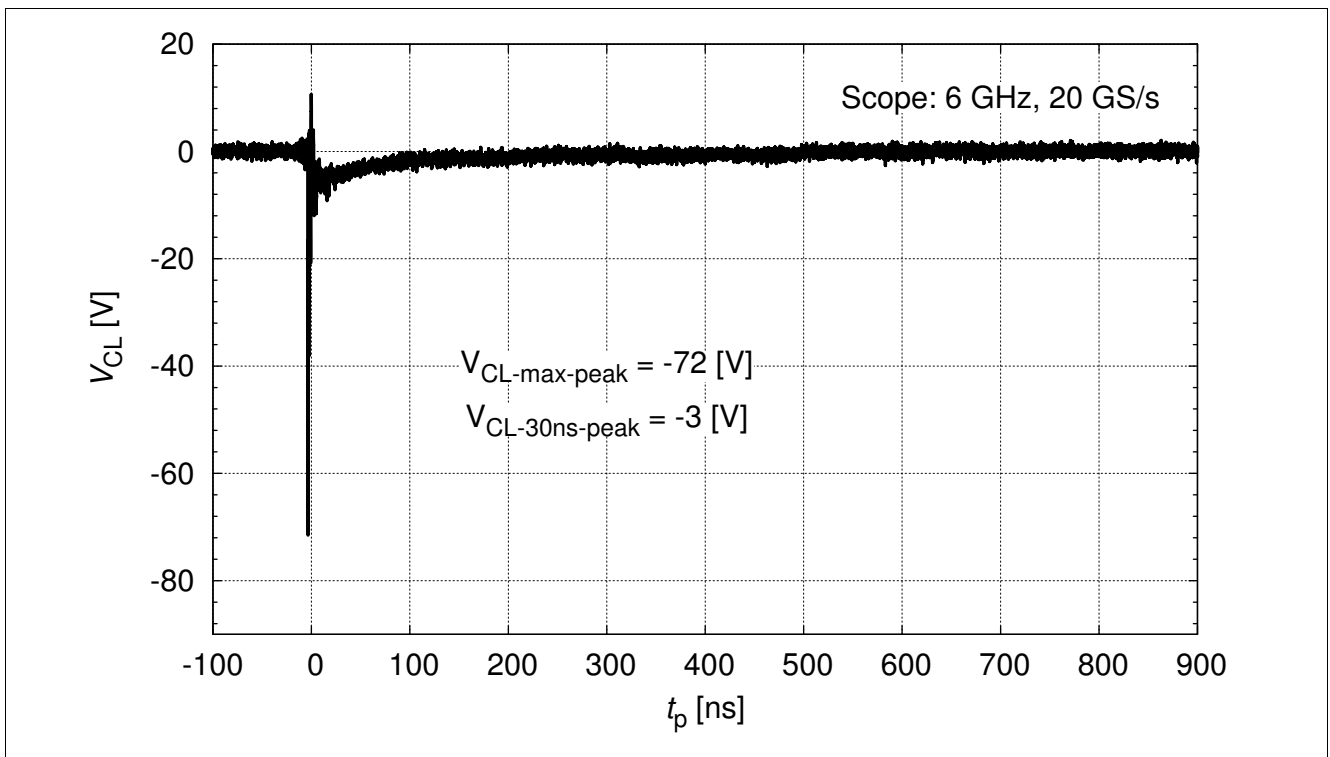


Figure 9 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV negative pulse from pin 1 to pin 2

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

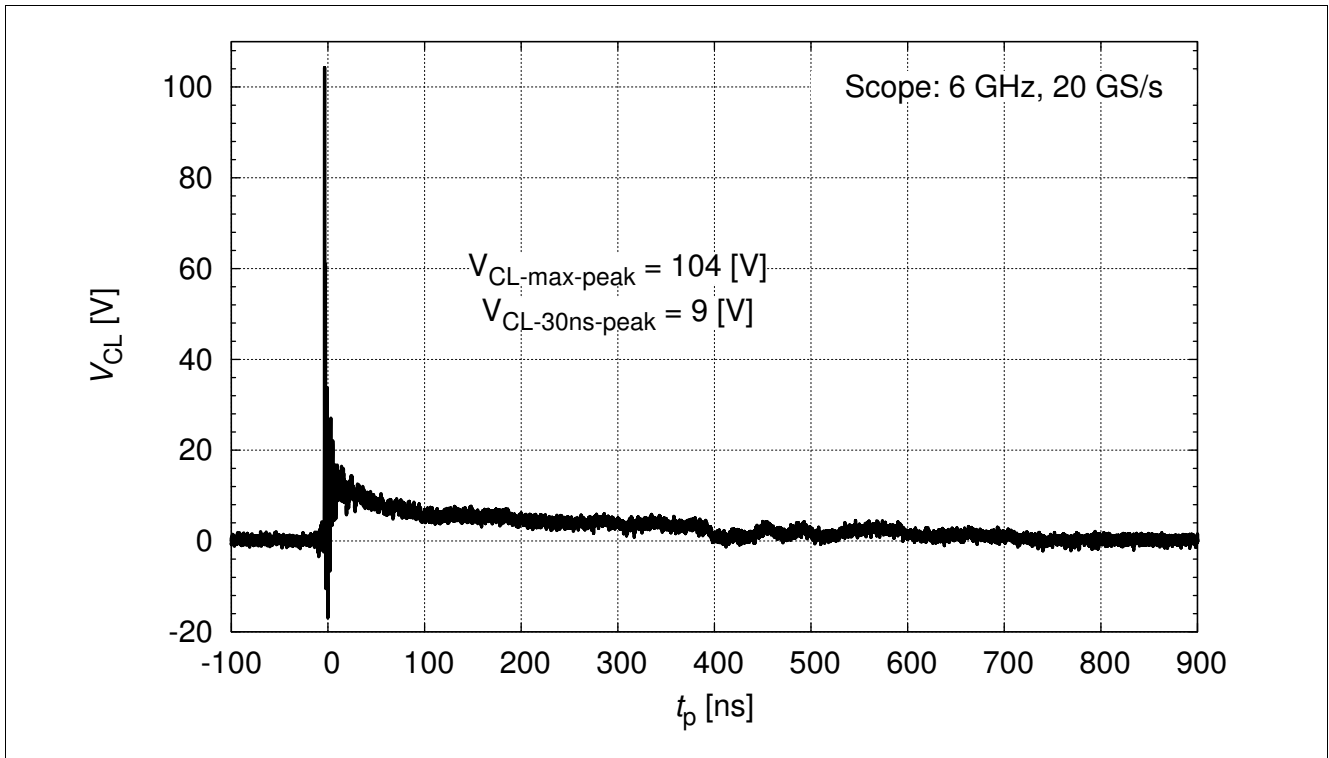


Figure 10 IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV positive pulse from pin 1 to pin 2

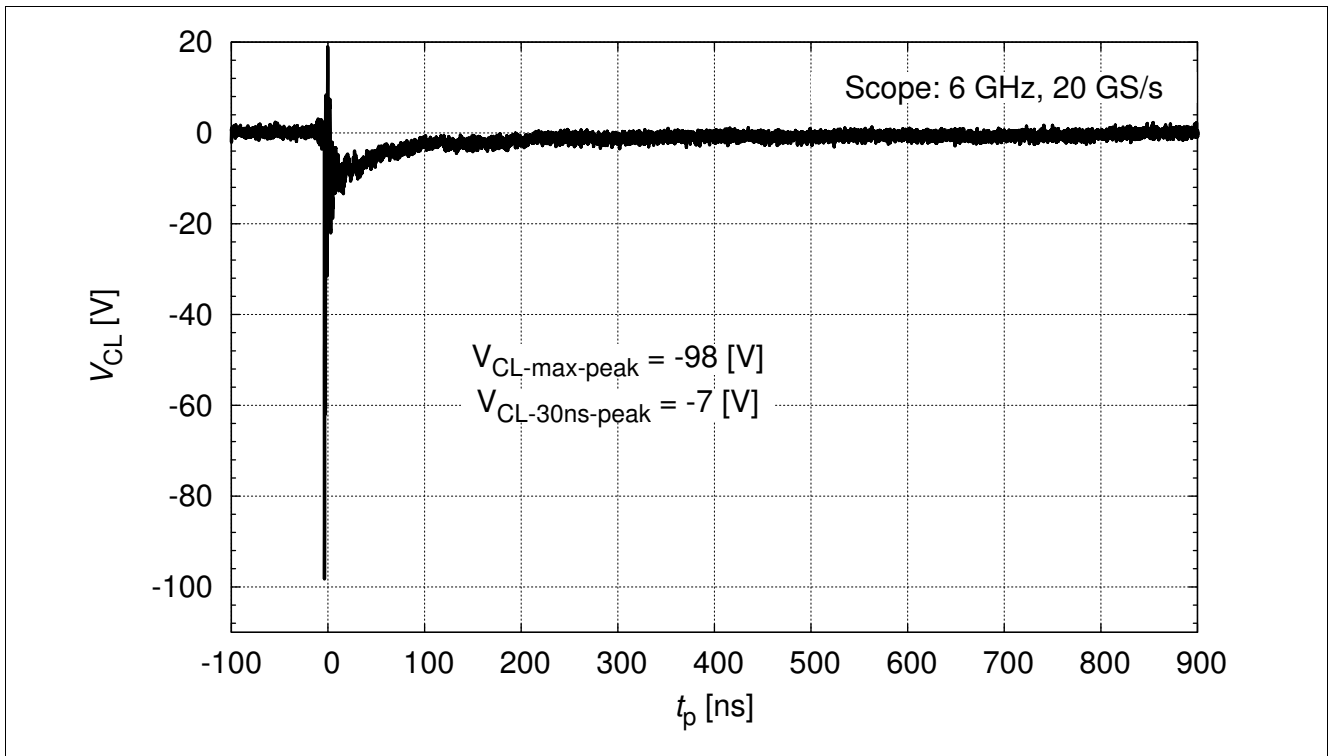


Figure 11 IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV negative pulse from pin 1 to pin 2

## 4 Package Information

### 4.1 TSLP-4-10 (mm)

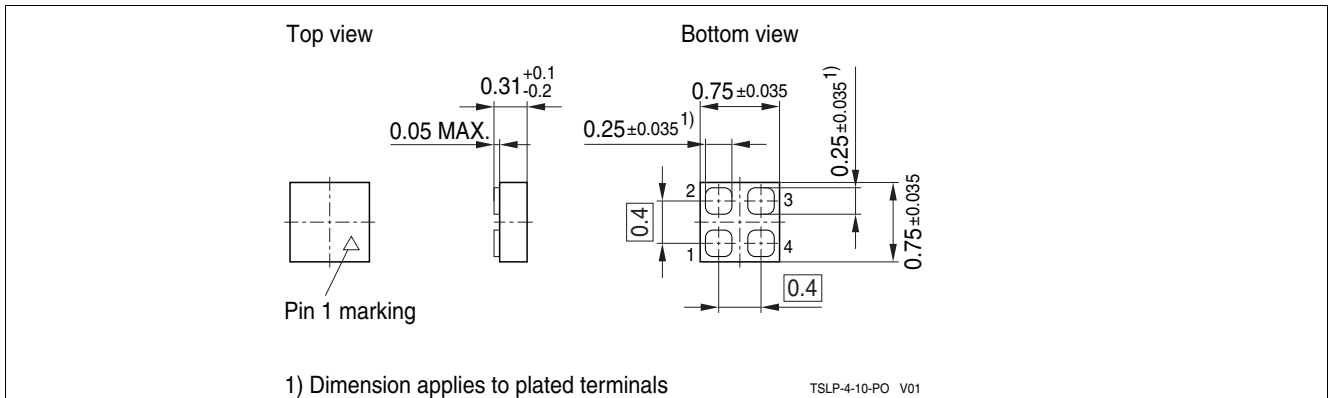


Figure 12 TSLP-4-10: Package outline (dimension in mm)

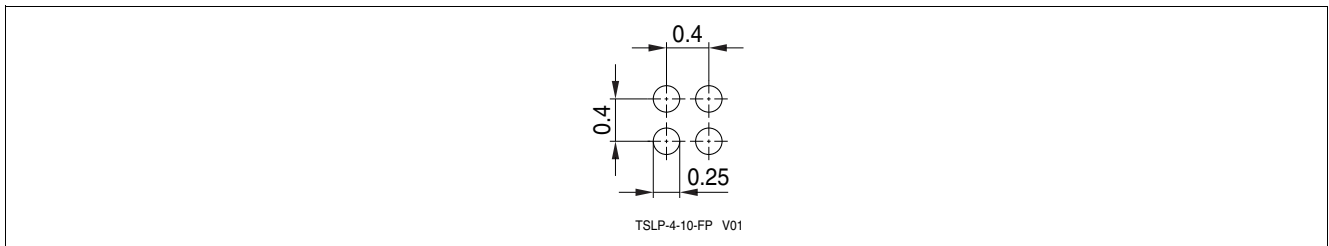


Figure 13 TSLP-4-10: Footprint (dimension in mm)

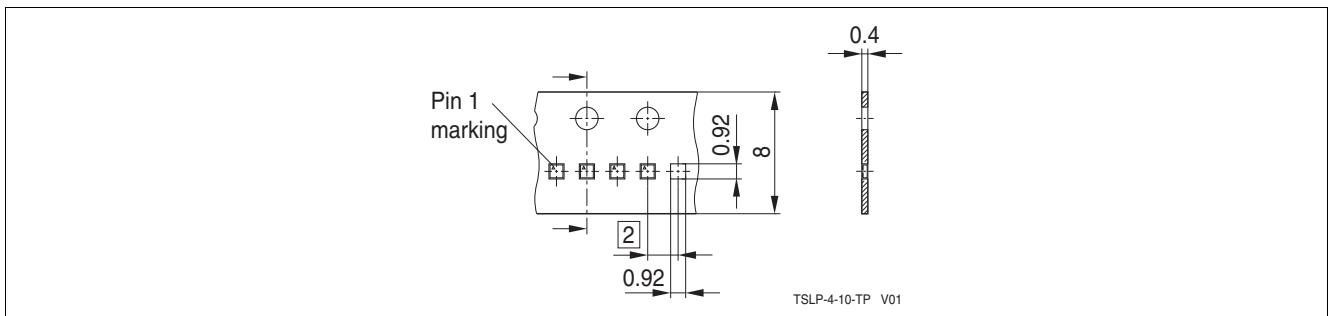


Figure 14 TSLP-4-10: Packing dimension in mm)

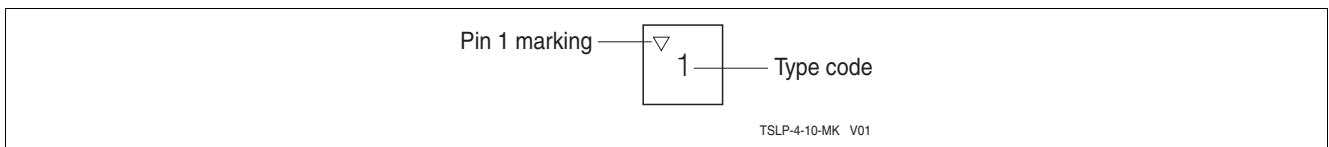


Figure 15 TSLP-4-10: Marking (example)

**References**

- [1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1
- [2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology
- [3] Infineon Technologie AG - **Application Note AN240**: Effective ESD Protection for USB3.0, combined with perfect Signal Integrity.

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